

# HD74LS194A

## 4-bit Bidirectional Universal Shift Register

REJ03D0456-0300  
Rev.3.00  
Jul.15.2005

The bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs. Operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely;

- Parallel (broadside) load
- Shift right (in the direction  $Q_A$  toward  $Q_D$ )
- Shift left (in the direction  $Q_D$  toward  $Q_A$ )
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is high and  $S_1$  is low. Serial data for this mode is entered at the shift-right data input. When  $S_0$  is low and  $S_1$  is high, data shifts left synchronously and new data is entered at the shift-left serial input.

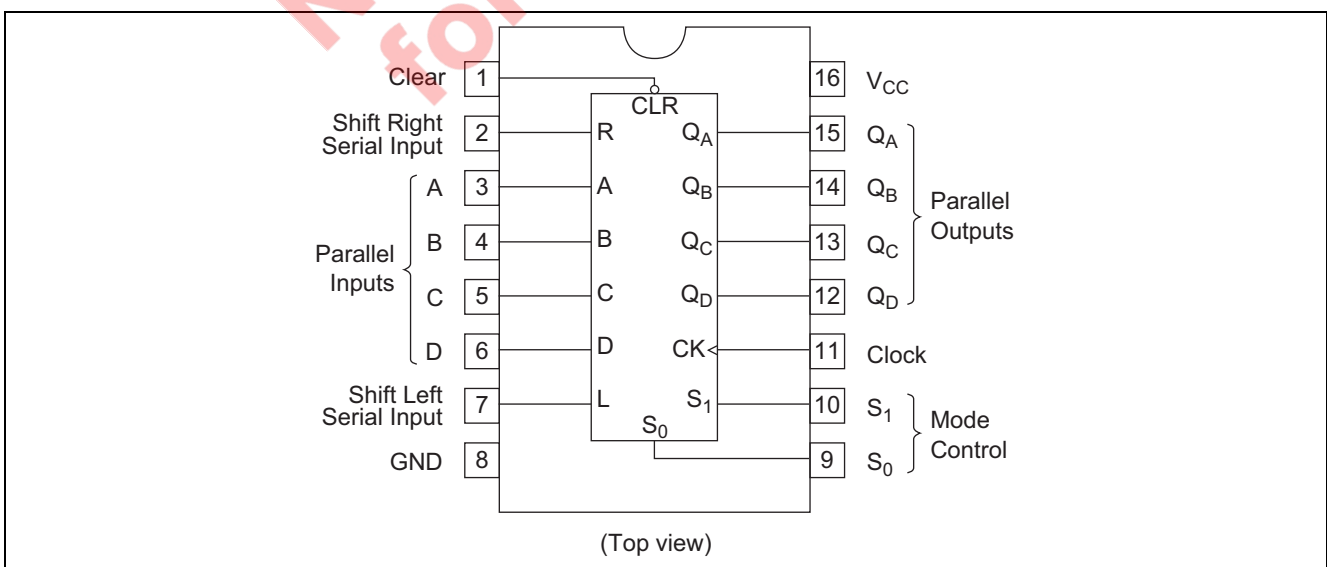
Clocking of the flip-flop is inhibited when both mode control inputs are low.

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS194AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS194AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement

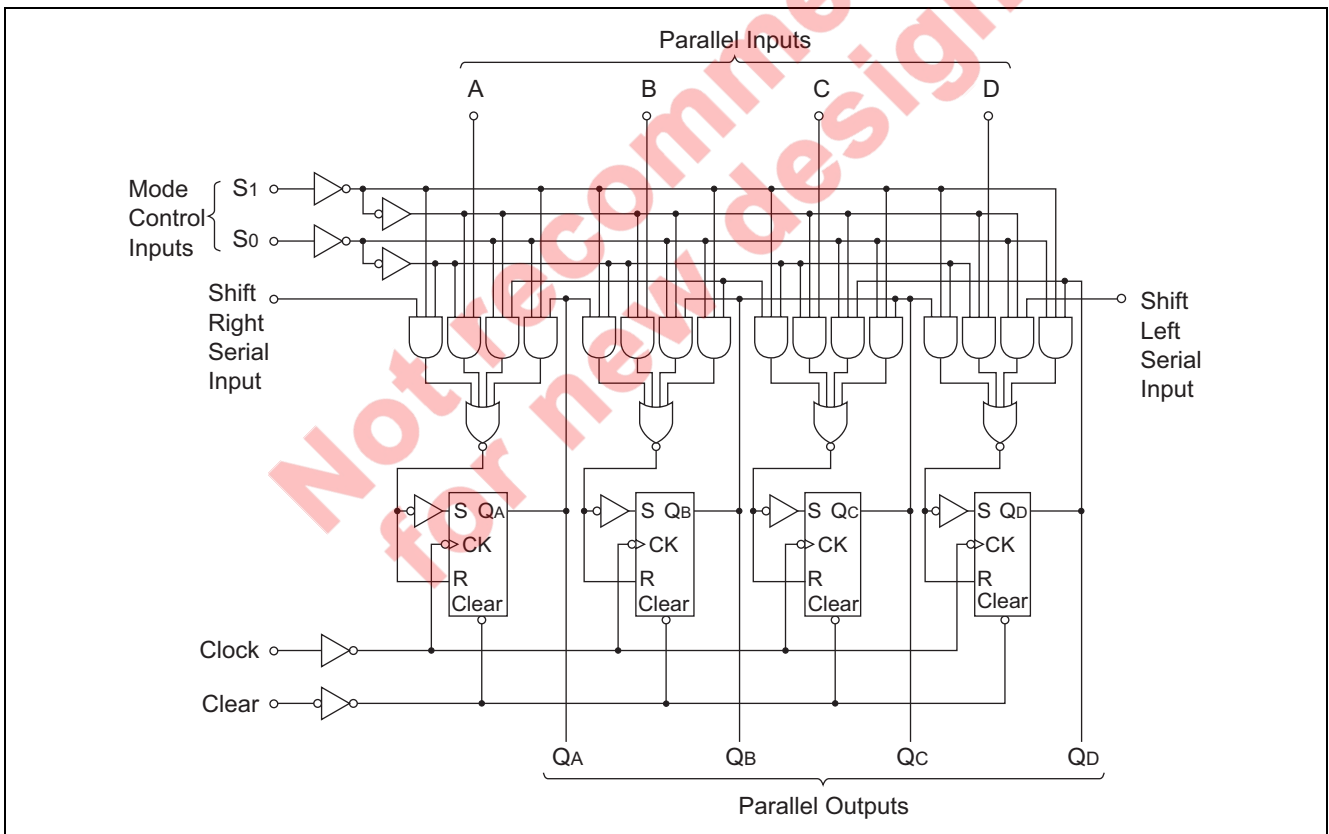


Function Table

Clear	Mode		Clock	Inputs						Outputs			
	S <sub>1</sub>	S <sub>0</sub>		Serial		Parallel				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
				Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	L	H	↑	X	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	H	L	↑	H	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	H
H	H	L	↑	L	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	L
H	L	L	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

- Notes:
1. H; high level, L; low level, X; irrelevant
  2. ↑; transition from low to high level
  3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively
  4. Q<sub>A0</sub> to Q<sub>D0</sub>; the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively before the indicated steady-state input conditions were established.
  5. Q<sub>An</sub> to Q<sub>Dn</sub>; the level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively before the most-recent ↑ transition of the clock.

Block Diagram



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	$\mu A$
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Clock frequency	$f_{clock}$	0	—	25	MHz
Clock pulse width	$t_w(CK)$	20	—	—	ns
Clear pulse width	$t_w(CLR)$	20	—	—	ns
Setup time	Mode Control	30	—	—	ns
	A, B, C, D, R, L	20	—	—	ns
	CLR (inactive state)	25	—	—	ns
Hold time	$t_h$	0	—	—	ns

## Electrical Characteristics

( $T_a = -20$  to  $+75$  °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	$V_{IH}$	2.0	—	—	V	
	$V_{IL}$	—	—	0.8	V	
Output voltage	$V_{OH}$	2.7	—	—	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ $\mu A$
	$V_{OL}$	—	—	0.4	V	$I_{OL} = 4$ mA
		—	—	0.5	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OL} = 8$ mA
Input current	$I_{IH}$	—	—	20	$\mu A$	$V_{CC} = 5.25$ V, $V_I = 2.7$ V
	$I_{IL}$	—	—	-0.4	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V
	$I_I$	—	—	0.1	mA	$V_{CC} = 5.25$ V, $V_I = 7$ V
Short-circuit output current	$I_{OS}$	-20	—	-100	mA	$V_{CC} = 5.25$ V
Supply current**	$I_{CC}$	—	15	23	mA	$V_{CC} = 5.25$ V
Input clamp voltage	$V_{IK}$	—	—	-1.5	V	$V_{CC} = 4.75$ V, $I_{IN} = -18$ mA

Notes: \*  $V_{CC} = 5$  V,  $T_a = 25$  °C

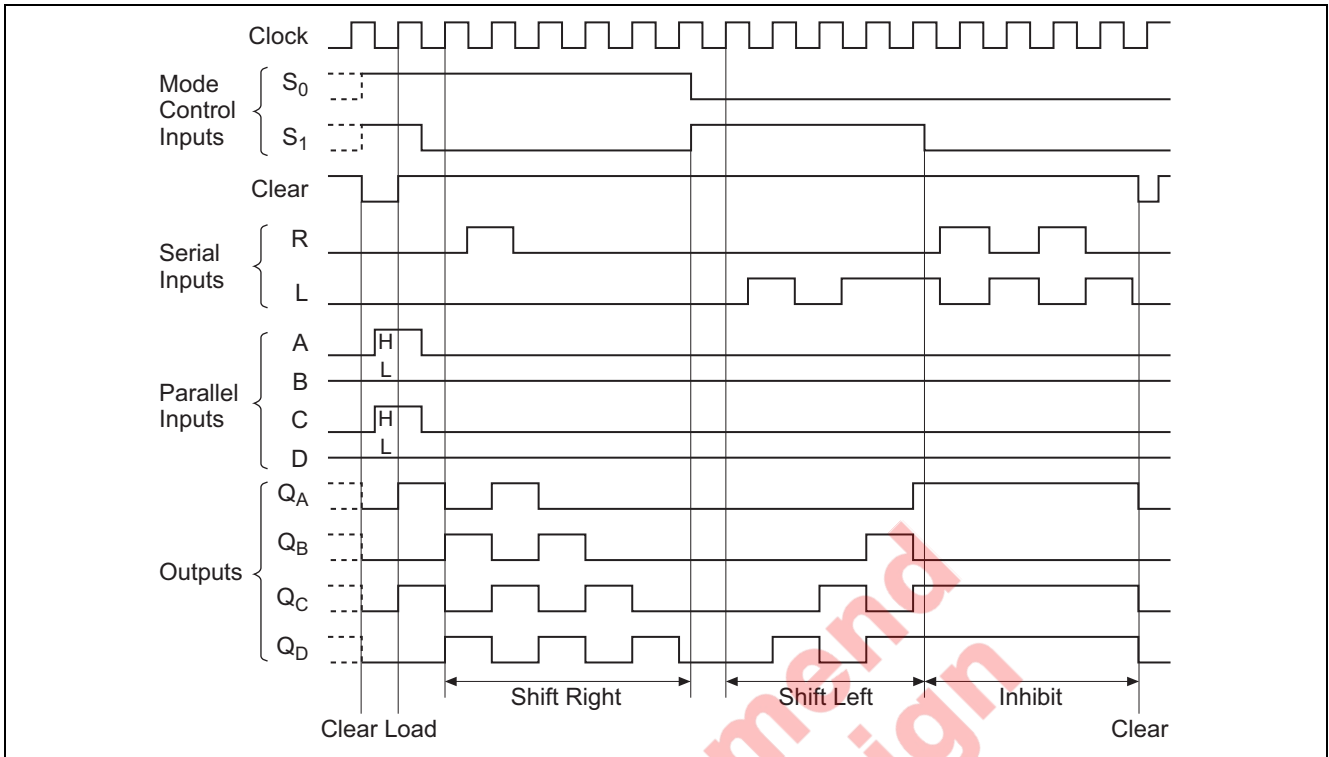
\*\* With all outputs open, inputs A through D grounded, and 4.5 V applied to  $S_0$ ,  $S_1$ , clear and the serial inputs,  $I_{CC}$  is tested with a momentary GND, then 4.5 V, applied to clock.

## Switching Characteristics

( $V_{CC} = 5$  V,  $T_a = 25$  °C)

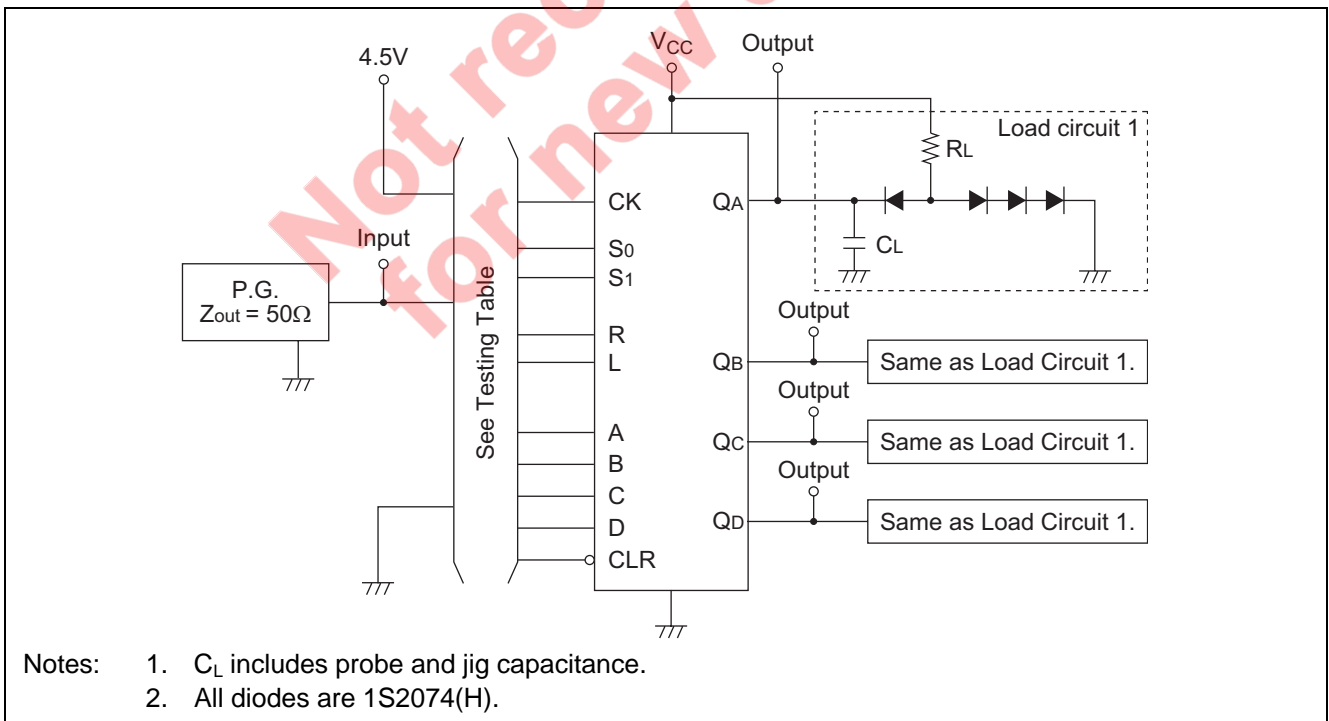
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{max}$			25	36	—	MHz	$C_L = 15$ pF, $R_L = 2$ k $\Omega$
Propagation delay time	$t_{PHL}$	Clear	Q	—	19	30	ns	
	$t_{PLH}$	Clock		—	14	22	ns	
	$t_{PHL}$	Clock		—	17	26	ns	

### Count Sequences



### Testing Method

#### Test Circuit



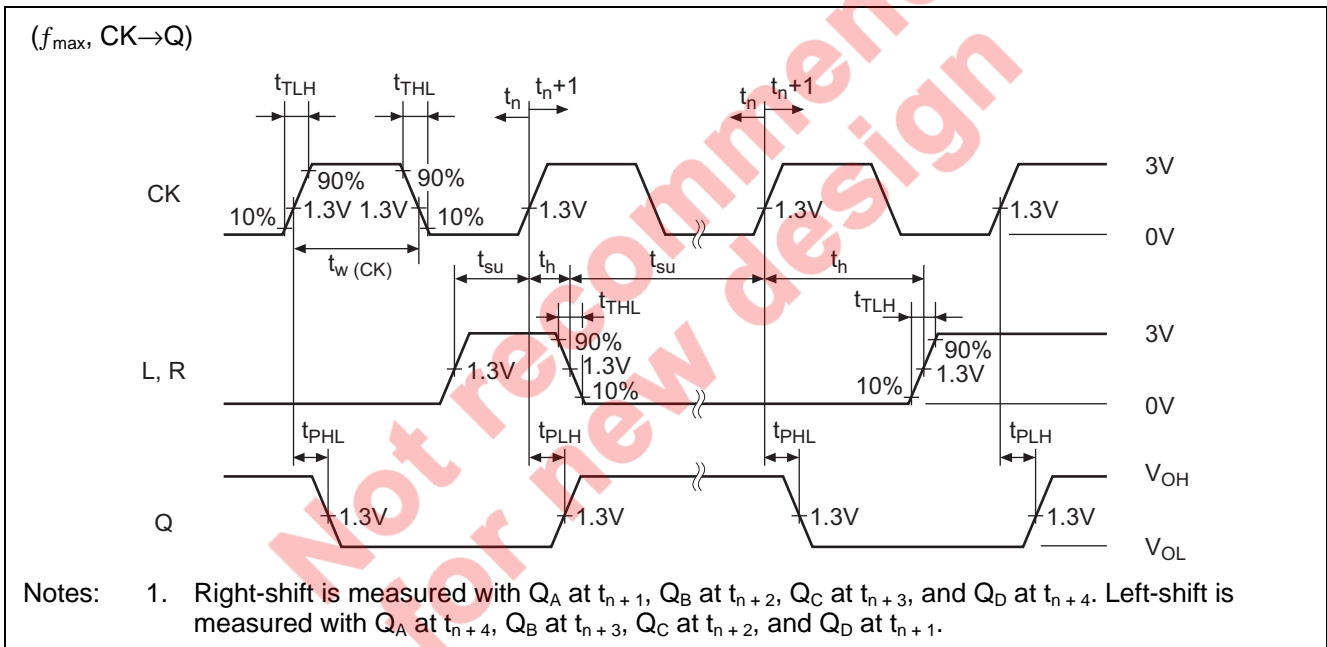
- Notes:
1. C<sub>L</sub> includes probe and jig capacitance.
  2. All diodes are 1S2074(H).

Testing Table

Item	From input to output	Inputs									
		CLR	S <sub>1</sub>	S <sub>0</sub>	CK	L	R	A	B	C	D
f <sub>max</sub>	right-shift	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
	left-shift	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	GND	GND
t <sub>PLH</sub>	Clear→Q	IN	4.5V	4.5V	IN	GND	GND	4.5V	4.5V	4.5V	4.5V
t <sub>PHL</sub>	Clock→Q	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
		4.5V	4.5V	GND	IN	IN	4.5V	GND	GND	GND	GND

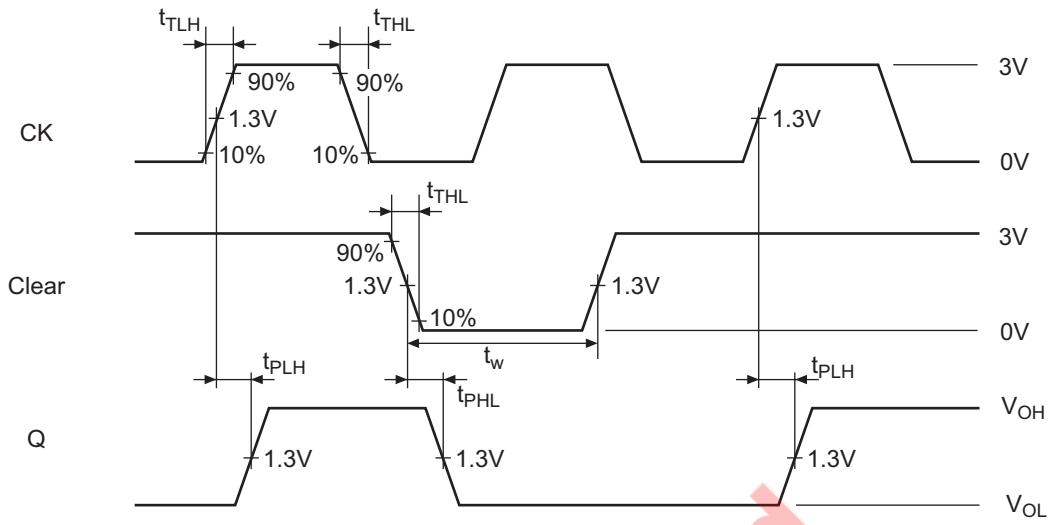
Item	From input to output	Outputs			
		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
f <sub>max</sub>	right-shift	OUT	OUT	OUT	OUT
	left-shift	OUT	OUT	OUT	OUT
t <sub>PLH</sub>	Clear→Q	OUT	OUT	OUT	OUT
t <sub>PHL</sub>	Clock→Q	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT

Waveforms 1



Waveforms 2

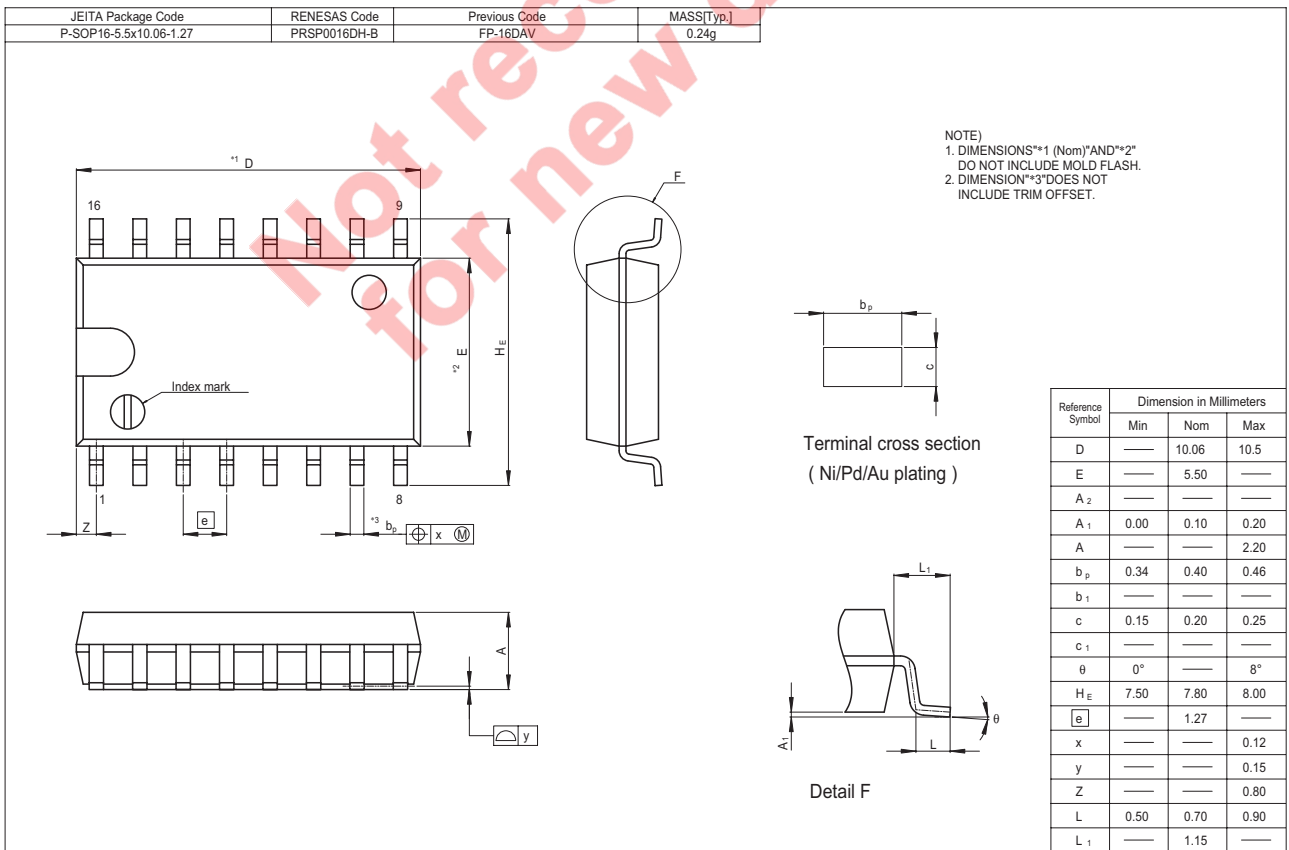
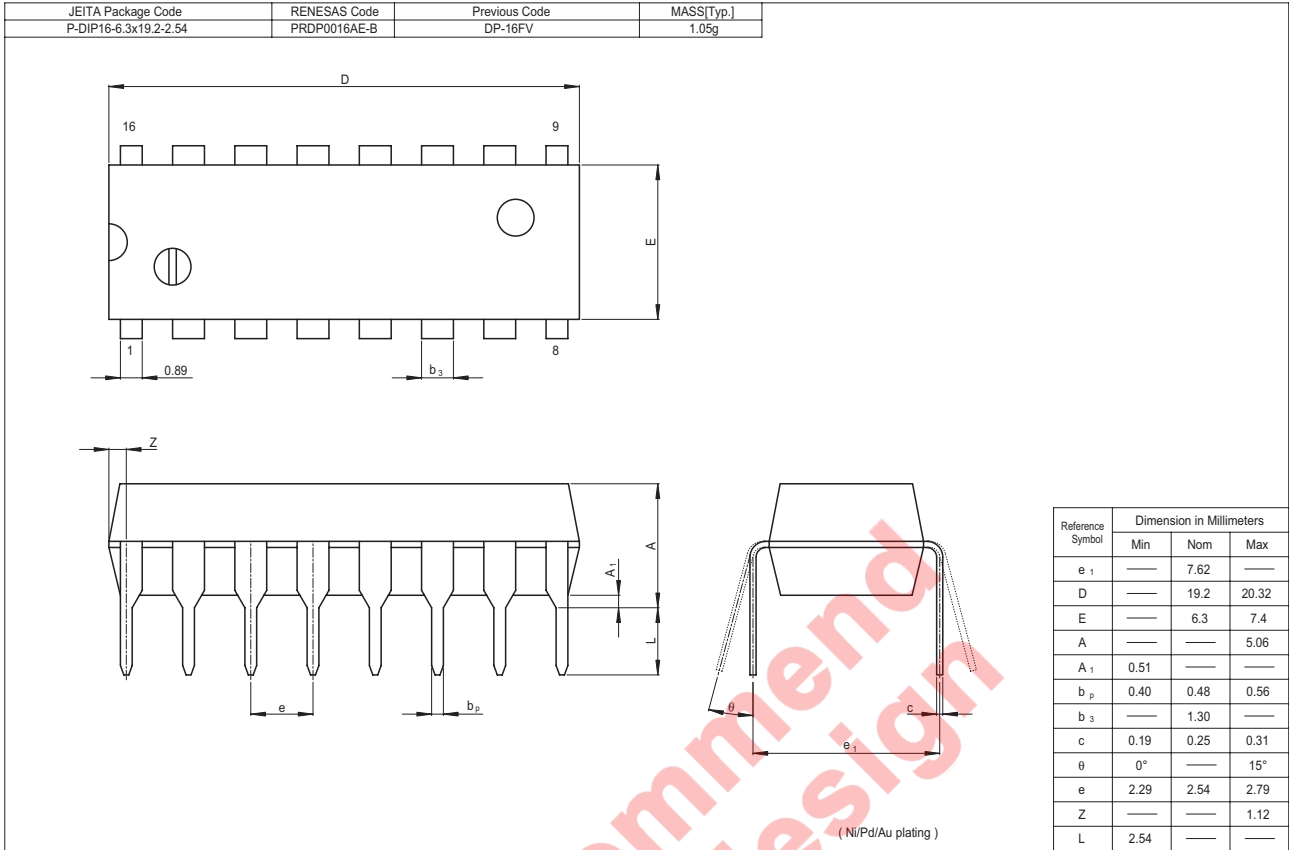
(Clear→Q)



Notes: Input pulse;  $t_{TLH} \leq 15 \text{ ns}$ ,  $t_{THL} \leq 6 \text{ ns}$

Not recommended  
for new design

Package Dimensions



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