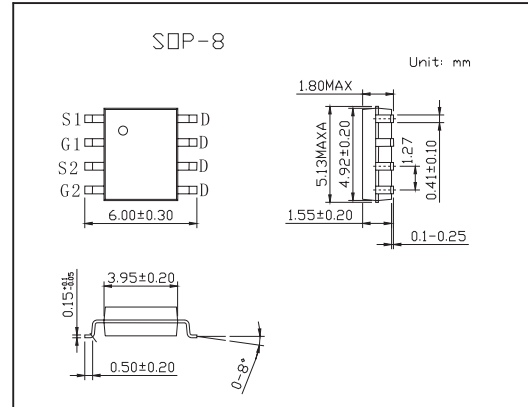
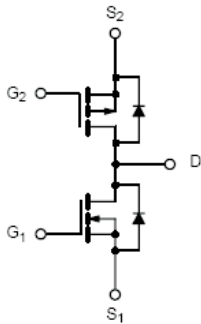


Complementary MOSFET Half-Bridge (N- and P-Channel)

KI4501DY

■ PIN Configuration

■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	30	-8	V
Gate-Source Voltage	V_{GS}	± 20	± 8	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)* $T_A = 25^\circ\text{C}$	I_D	± 9	± 6.2	A
		$T_A = 70^\circ\text{C}$	± 7.4	± 5.0
Pulsed Drain Current	I_{DM}	± 30	± 20	A
Continuous Source Current (Diode Conduction) ⁸	I_S	1.7	-1.7	A
Maximum Power Dissipation* $T_A = 25^\circ\text{C}$	P_D	2.5		W
		$T_A = 70^\circ\text{C}$		1.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

*Surface Mounted on FR4 Board; $t \leq 10$ sec

■ Thermal Resistance Ratings $T_A = 25^\circ\text{C}$

Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient*	R_{thJA}	$t \leq 10$ sec	38	50	40	50	$^\circ\text{C/W}$
		Steady State	73	95	73	95	
Maximum Junction-to-Foot	R_{thJc}	17	22	20	26		

*Surface Mounted on FR4 Board.

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■ Electrical Characteristics $T_J = 25^\circ\text{C}$

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	0.8			V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-0.45			
Gate Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	N-Ch			± 100	nA
		$V_{DS} = 0\text{V}, V_{GS} = \pm 8\text{V}$	P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$	N-Ch			1	
		$V_{DS} = -6.4\text{V}, V_{GS} = 0\text{V}$	P-Ch			-1	
		$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	N-Ch			5	μA
		$V_{DS} = -6.4\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	P-Ch			-5	
On State Drain Currenta	$I_{D(on)}$	$V_{DS} = 5\text{V}, V_{GS} = 10\text{V}$	N-Ch	30			A
		$V_{DS} = -5\text{V}, V_{GS} = -4.5\text{V}$	P-Ch	-20			
Drain Source On State Resistance*	$r_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 9\text{A}$	N-Ch		0.015	0.018	Ω
		$V_{GS} = -4.5\text{V}, I_D = -6.2\text{A}$	P-Ch		0.034	0.042	
		$V_{GS} = 4.5\text{V}, I_D = 7.4\text{A}$	N-Ch		0.022	0.027	
		$V_{GS} = -2.5\text{V}, I_D = -5.2\text{A}$	P-Ch		0.048	0.060	
Forward Transconductance*	g_{fs}	$V_{DS} = 15\text{V}, I_D = 9\text{A}$	N-Ch		20		S
		$V_{DS} = -15\text{V}, I_D = -6.2\text{A}$	P-Ch		14		
Diode Forward Voltage*	V_{SD}	$I_S = 1.7\text{A}, V_{GS} = 0\text{V}$	N-Ch		0.71	1.1	V
		$I_S = -1.7\text{A}, V_{GS} = 0\text{V}$	P-Ch		-0.70	-1.1	
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15\text{V}, V_{GS} = 5\text{V}, I_D = 9\text{A}$	N-Ch		4.5	20	pC
Gate Source Charge	Q_{gs}	P-Channel	N-Ch		3.3		
			P-Ch		3.0		
Gate Drain Charge	Q_{gd}	$V_{DS} = -4\text{V}, V_{GS} = -5\text{V}, I_D = -6.2\text{A}$	N-Ch		6.6		
			P-Ch		2.0		
Turn On Time	$t_{d(on)}$	N Channel $V_{DD} = 15\text{V}, R_L = 15\Omega$	N-Ch		13	20	ns
Rise Time	t_r	$I_D = 1\text{A}, V_{GEN} = 10\text{V}, R_g = 6\Omega$	P-Ch		20	40	
			N-Ch		9	18	
Turn Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -4\text{V}, R_L = 4\Omega$	N-Ch		35	50	
			P-Ch		110	220	
Fall Time	t_f	$I_D = -1\text{A}, V_{GEN} = -4.5\text{V}, R_g = 6\Omega$	N-Ch		17	30	
			P-Ch		60	120	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$	N-Ch		35	70	
			P-Ch		60	100	

* Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.