Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Little-endian
  - EmbeddedICE™ (In-circuit Emulation)
- 8-, 16- and 32-bit Read and Write Support
- 256K Bytes of On-chip SRAM
  - 32-bit Data Bus
  - Single-clock Cycle Access
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to Eight Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- Eight-level Priority, Individually Maskable, Vectored Interrupt Controller
  - Four External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 32 Programmable I/O Lines
- Three-channel 16-bit Timer/Counter
  - Three External Clock Inputs
  - Two Multi-purpose I/O Pins per Channel
- Two USARTs
  - Two Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Advanced Power-saving Features
  - CPU and Peripheral Can be Deactivated Individually
- Fully Static Operation
  - 0 Hz to 75 MHz Internal Frequency Range at V_{DDCORE} = 1.8V, 85°C
- 2.7V to 3.6V I/O Operating Range
- 1.65V to 1.95V Core Operating Range
- Available in 100-lead TQFP Package
- -40° C to +85° C Temperature Range

AT91 ARM® Thumb® Microcontrollers

AT91R40008 Electrical Characteristics

1. Description

The AT91R40008 microcontroller is a member of the Atmel AT91 16-/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance, 32-bit RISC architecture with a high-density, 16-bit instruction set and very low power consumption. Furthermore, it features 256K bytes of on-chip SRAM and a large number of internally banked registers, resulting in very fast exception handling, and making the device ideal for real-time control applications.

The AT91R40008 microcontroller features a direct connection to off-chip memory, including Flash, through the fully-programmable External Bus Interface (EBI). An 8-level priority vectored interrupt controller, in conjunction with the Peripheral Data Controller, significantly improves the real-time performance of the device.

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with a large, on-chip, high-speed SRAM and a wide range of peripheral functions on a monolithic chip, the AT91R40008 is a powerful microcontroller that offers a flexible and high-performance solution to many compute-intensive embedded control applications.

1795E–ATARM–12-Dec-05

2. Absolute Maximum Ratings*

Operating Temperature (Industrial) .. -40° C to + 85° C
Storage Temperature..... -60° C to + 150° C
Voltage on Any Input Pin with Respect to Ground .....-0.3V to max of V_{DDIO} ..... + 0.3V and 3.6V
Maximum Operating Voltage (V_{DDIO}) 3.6V
Maximum Operating Voltage (V_{DDCORE}) 1.95V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. DC Characteristics

The following characteristics are applicable to the Operating Temperature range: T_A = -40° C to +85° C, unless otherwise specified and are certified for a Junction Temperature up to 100° C.

Table 3-1. DC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{DDIO}	DC Supply I/Os			2.7		3.6	V
V_{DDCORE}	DC Supply Core			1.65		1.95	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DDIO} + 0.3	V
V_{OL}	Output Low Voltage	Pin Group 1[2]: I_{OL} = 16 mA[1]				0.4	V
		Pin Group 2[3]: I_{OL} = 8 mA[1]				0.4	V
		Pin Group 3[4]: I_{OL} = 2 mA[1]				0.4	V
		All Output Pins: I_{OL} = 0 mA[1]				0.2	V
V_{OH}	Output High Voltage	Pin Group 1[2]: I_{OH} = 16 mA[1]		V_{DDIO} - 0.4			V
		Pin Group 2[3]: I_{OH} = 8 mA[1]		V_{DDIO} - 0.4			
		Pin Group 3[4]: I_{OH} = 2 mA[1]		V_{DDIO} - 0.4			
		All Output Pins: I_{OH} = 0 mA[1]		V_{DDIO} - 0.2			
I_{LEAK}	Input Leakage Current					10	µA
I_{PULL}	Input Pull-up Current	V_{DDIO} = 3.6V, V_{IN} = 0V				280	µA
I_{OUT}	Output Current	Pin Group 1[2]				16	mA
		Pin Group 2[3]:				8	mA
		Pin Group 3[4]:				2	mA
C_{IN}	Input Capacitance	TQFP100 Package				5.3	pF
I_{SC}	Static Current	VDDIO= 3.6V, V_{DDCORE} = 1.95V, MCKI = 0Hz All Inputs Driven TMS, TCK, TDI, NRST = 1	T_A = 25° C			120	µA
			T_A = 85° C			2.3	mA

Notes:
1. I_{OL} = Output Current at low level. I_{OH}= Output Current at high level.
2. Pin Group 1 = NUB/NWR1, NWE/NWR0, NOE/NRD1
3. Pin Group 2 = D0-D15, A0/NLB, A1-A19, P28/A20/CS7, P29/A21/CS6, P30/A22/CS5, P31/A23/CS4, NCS0, NCS1, P26/NCS2, P27/NCS3
4. Pin Group 3 = All Others

4. Power Consumption

The values in the following tables are values measured in the typical operating conditions (i.e., V_{DDIO} = 3.3V, V_{DDCORE} = 1.8V, T_A = 25° C) on the AT91EB40A Evaluation Board and are given as demonstrative values.

Table 4-1. Power Consumption

Mode	Conditions	Consumption	Unit
Reset		0.02	mW/MHz
Normal	Fetch in ARM mode from internal SRAM All peripheral clocks activated	0.83	
	Fetch in ARM mode from internal SRAM All peripheral clocks deactivated	0.73	
	Fetch in ARM mode from external SRAM(1) All peripheral clocks deactivated	0.20	
	Fetch in Thumb mode from external SRAM(1) All peripheral clocks deactivated	0.24	
Idle	All peripheral clocks activated	0.16	
	All peripheral clocks deactivated	0.06	

Note: 1. With two Wait States.

Table 4-2. Power Consumption per Peripheral

Peripheral	Consumption	Unit
PIO Controller	15.3	µW/MHz
Timer/Counter Channel	15.0	
Timer/Counter Block (3 Channels)	36.3	
USART	27.8	

4.1 Thermal and Reliability Considerations

4.1.1 Thermal Data

In Table 4-3, the device lifetime is estimated with the MIL-217 standard in the “moderately controlled” environmental model (this model is described as corresponding to an installation in a permanent rack with adequate cooling air), depending on the device Junction Temperature. (For details see the section ”Junction Temperature” on page 5.)

Note that the user must be extremely cautious with this MTBF calculation: as the MIL-217 model is pessimistic with respect to observed values due to the way the data/models are obtained (test under severe conditions). The life test results that have been measured are always better than the predicted ones.

Table 4-3. MTBF Versus Junction Temperature

Junction Temperature (T_J) (°C)	Estimated Lifetime (MTBF) (Year)
100	10
125	5
150	3
175	2

Table 4-4 summarizes the thermal resistance data related to the package of interest.

Table 4-4. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	40	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	6.4	

4.1.2 Reliability Data

The number of gates and the device die size are provided for the user to calculate reliability data with another standard and/or in another environmental model.

Table 4-5. Reliability Data

Parameter	Data	Unit
Number of Logic Gates	280	K gates
Number of Memory Gates	12,897	K gates
Device Die Size	21.2	mm^2

4.2 Junction Temperature

The average chip-junction temperature T_J in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

Where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 4-4 on page 5.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 4-4 on page 5.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in the section "Power Consumption" on page 4.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and thereby decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C

5. Conditions

5.1 Timing Results

The delays are given as typical values in the following conditions:

- V_{DDIO} = 3.0V
- V_{DDCORE} = 1.8V
- Ambient Temperature = 25° C
- Load Capacitance = 0 pF
- The output level change detection is *0.5 x* V_{DDIO}
- The input level is *0.8V* for a low-level detection and is *2.0V* for a high level detection.

The minimum and maximum values given in the AC characteristic tables of this datasheet take into account the process variation and the design.

In order to obtain the timing for other conditions, the following equation should be used:

$$t = \delta_{T^\circ} \times \left((\delta_{VDDCORE} \times t_{DATASHEET}) + \left(\delta_{VDDIO} \times \sum C_{SIGNAL} \times \delta_{CSIGNAL} \right) \right)$$

Where:

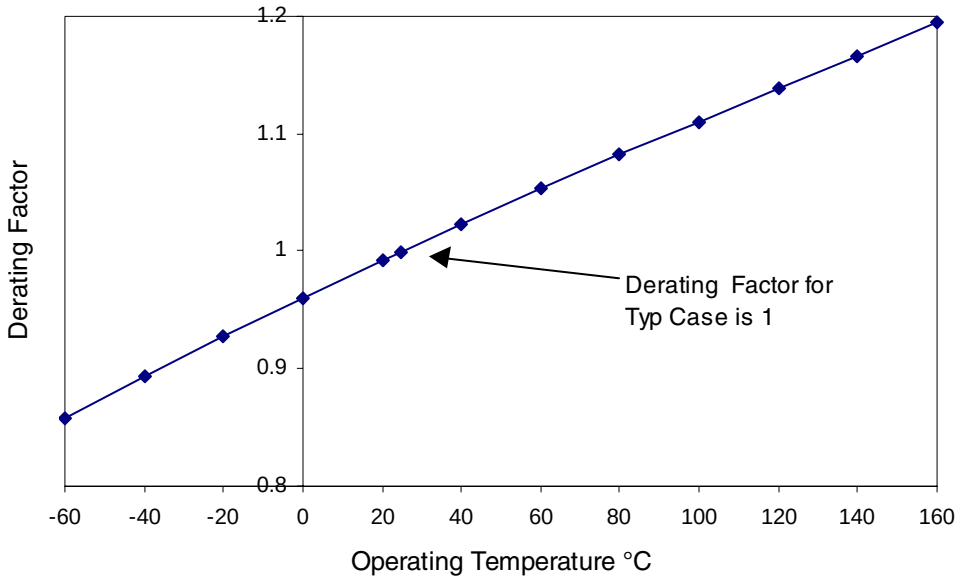
- δ_T° is the derating factor in temperature given in Figure 5-1.
- $\delta_{VDDCORE}$ is the derating factor for the Core Power Supply given in Figure 5-2 on page 7.
- $t_{DATASHEET}$ is the minimum or maximum timing value given in this datasheet for a load capacitance of 0 pF.
- δ_{VDDIO} is the derating factor for the I/O Power Supply given in Figure 5-3 on page 8.
- C_{SIGNAL} is the capacitance load on the considered output pin.(1)
- $\delta_{CSIGNAL}$ is the load derating factor depending on the capacitance load on the related output pins given in Min and Max values in this datasheet.

The input delays are given as typical values.

Note: The user must take into account the package capacitance load contribution (C_{IN}) described in Table 3-1 on page 3.

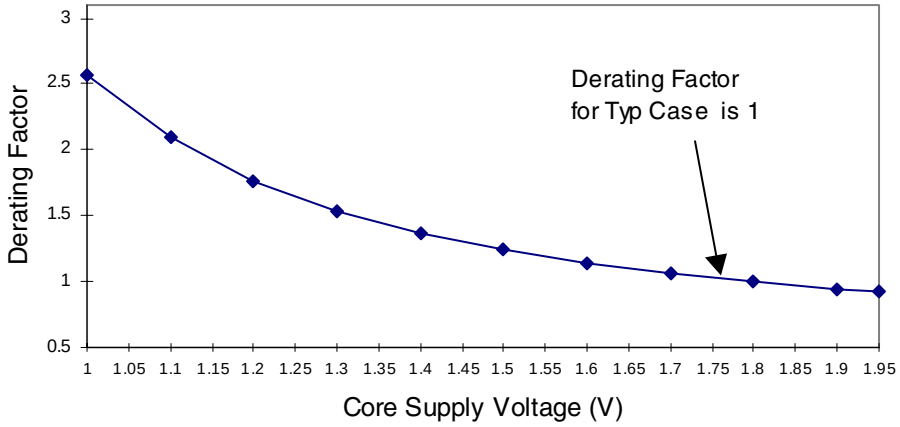
5.2 Temperature Derating Factor

Figure 5-1. Derating Curve for Different Operating Temperatures



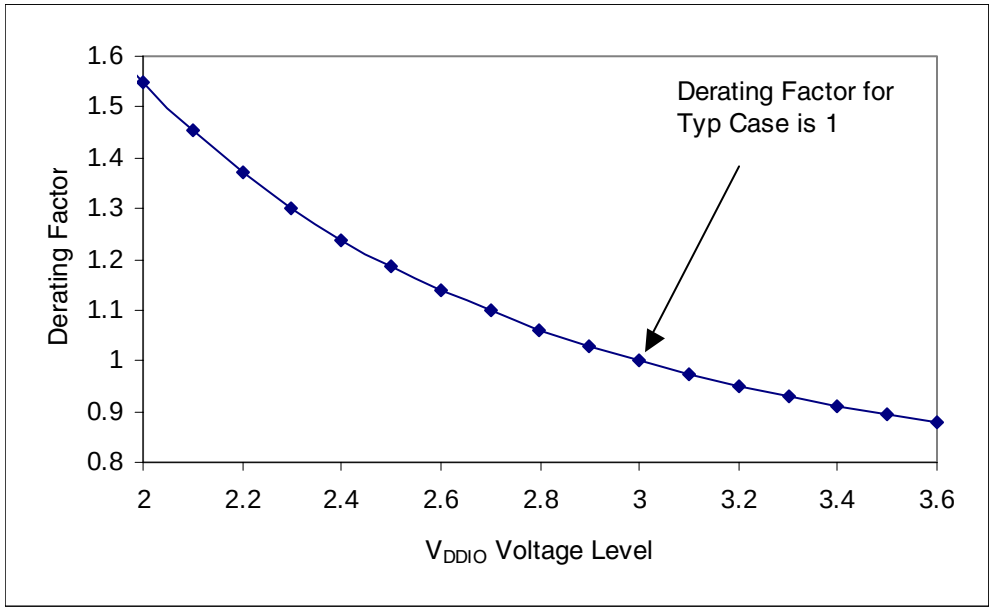
5.3 Core Voltage Derating Factor

Figure 5-2. Core Voltage Derating Factor



5.4 IO Voltage Derating Factor

Figure 5-3. Derating Factor for Different V_{DDIO} Power Supply Levels



6. Clock Waveforms

Table 6-1. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Units
$1/(t_{CP})$	Oscillator Frequency			82.1	MHz
t_{CP}	Oscillator Period		12.2		ns
t_{CH}	High Half-period		5.0		ns
t_{CL}	Low Half-period		5.5		ns

Table 1. Clock Propagation Times

Symbol	Parameter	Conditions	Min	Max	Units
t_{CDLH}	Rising Edge Propagation Time	C_{MCKO} = 0 pF	4.4	6.6	ns
		C_{MCKO} derating	0.199	0.295	ns/pF
t_{CDHL}	Falling Edge Propagation Time	C_{MCKO} = 0 pF	4.5	6.7	ns
		C_{MCKO} derating	0.153	0.228	ns/pF

Figure 6-1. Clock Waveform

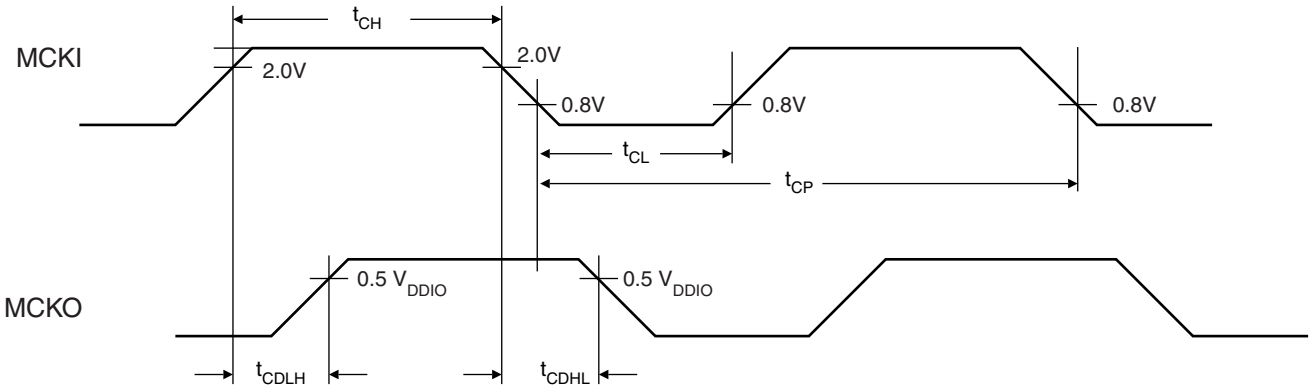
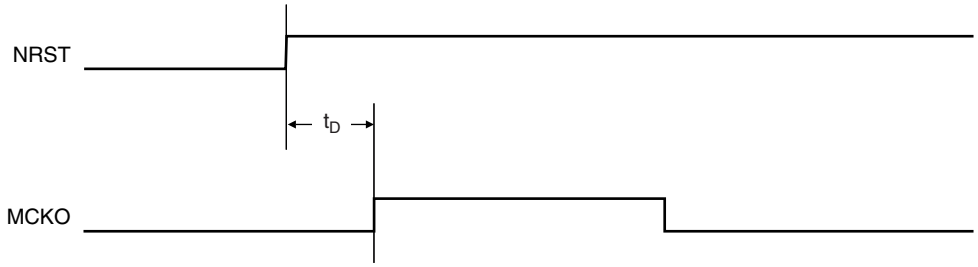


Table 6-2. NRST to MCKO

Symbol	Parameter	Min	Max	Units
t_D	NRST Rising Edge to MCKO Valid Time	$3(t_{CP}/2)$	$7(t_{CP}/2)$	ns

Figure 6-2. MCKO Relative to NRST



7. AC Characteristics

7.1 EBI Signals Relative to MCKI

The following tables show timings relative to operating condition limits defined in the section "Timing Results" on page 6. See Figure 7-1 on page 14.

Table 7-1. General-purpose EBI Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_1	MCKI Falling to NUB Valid	C_{NUB} = 0 pF	4.4	8.9	ns
		C_{NUB} derating	0.030	0.043	ns/pF
EBI_2	MCKI Falling to NLB/A0 Valid	C_{NLB} = 0 pF	3.7	6.7	ns
		C_{NLB} derating	0.045	0.069	ns/pF
EBI_3	MCKI Falling to A1 - A23 Valid	C_{ADD} = 0 pF	3.4	7.8	ns
		C_{ADD} derating	0.045	0.076	ns/pF
EBI_4	MCKI Falling to Chip Select Change	C_{NCS} = 0 pF	3.7	8.6	ns
		C_{NCS} derating	0.045	0.078	ns/pF
EBI_5	NWAIT Setup before MCKI Rising		1.7		ns
EBI_6	NWAIT Hold after MCKI Rising		1.7		ns

Table 7-2. EBI Write Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_7	MCKI Rising to NWR Active (No Wait States)	C_{NWR} = 0 pF	3.9	6.3	ns
		C_{NWR} derating	0.029	0.043	ns/pF
EBI_8	MCKI Rising to NWR Active (Wait States)	C_{NWR} = 0 pF	4.4	7.0	ns
		C_{NWR} derating	0.029	0.043	ns/pF
EBI_9	MCKI Falling to NWR Inactive (No Wait States)	C_{NWR} = 0 pF	3.8	6.3	ns
		C_{NWR} derating	0.029	0.044	ns/pF
EBI_{10}	MCKI Rising to NWR Inactive (Wait States)	C_{NWR} = 0 pF	4.2	6.7	ns
		C_{NWR} derating	0.029	0.044	ns/pF
EBI_{11}	MCKI Rising to D0 - D15 Out Valid	C_{DATA} = 0 pF	4.2	7.5	ns
		C_{DATA} derating	0.045	0.080	ns/pF
EBI_{12}	NWR High to NUB Change	C_{NUB} = 0 pF	3.1	7.0	ns
		C_{NUB} derating	0.030	0.043	ns/pF
EBI_{13}	NWR High to NLB/A0 Change	C_{NLB} = 0 pF	3.1	5.4	ns
		C_{NLB} derating	0.043	0.073	ns/pF
EBI_{14}	NWR High to A1 - A23 Change	C_{ADD} = 0 pF	2.9	7.0	ns
		C_{ADD} derating	0.043	0.076	ns/pF

Table 7-2. EBI Write Signals (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
EBI_{15}	NWR High to Chip Select Inactive	C_{NCS} = 0 pF	2.9	6.8	ns
		C_{NCS} derating	0.052	0.067	ns/pF
EBI_{16}	Data Out Valid before NWR High (No Wait States)(1)	C = 0 pF	t_{CH} - 1.8		ns
		C_{DATA} derating	-0.080		ns/pF
		C_{NWR} derating	0.044		ns/pF
EBI_{17}	Data Out Valid before NWR High (Wait States)(1)	C = 0 pF	n x t_{CP} - 1.3(2)		ns
		C_{DATA} derating	-0.080		ns/pF
		C_{NWR} derating	0.044		ns/pF
EBI_{18}	Data Out Valid after NWR High		2.2		ns
EBI_{19}	NWR Minimum Pulse Width (No Wait States)(1)	C_{NWR} = 0 pF	t_{CH} - 0.6		ns
		C_{NWR} derating	0		ns/pF
EBI_{20}	NWR Minimum Pulse Width (Wait States)(1)	C_{NWR} = 0 pF	n x t_{CP} - 0.9(2)		ns
		C_{NWR} derating	0		ns/pF

Notes: 1. The derating factor should not be applied to t_{CH} or t_{CP}
2. n = number of standard wait states inserted.

Table 7-3. EBI Read Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_{21}	MCKI Falling to NRD Active(1)	C_{NRD} = 0 pF	4.5	7.9	ns
		C_{NRD} derating	0.029	0.043	ns/pF
EBI_{22}	MCKI Rising to NRD Active(2)	C_{NRD} = 0 pF	3.8	7.3	ns
		C_{NRD} derating	0.029	0.043	ns/pF
EBI_{23}	MCKI Falling to NRD Inactive(1)	C_{NRD} = 0 pF	4.1	6.5	ns
		C_{NRD} derating	0.030	0.044	ns/pF
EBI_{24}	MCKI Falling to NRD Inactive (2)	C_{NRD} = 0 pF	3.9	5.8	ns
		C_{NRD} derating	0.030	0.044	ns/pF
EBI_{25}	D0 - D15 In Setup before MCKI Falling Edge(5)		1.5		ns
EBI_{26}	D0 - D15 In Hold after MCKI Falling Edge(6)		1.2		ns
EBI_{27}	NRD High to NUB Change	C_{NUB} = 0 pF	3.2	7.1	ns
		C_{NUB} derating	0.030	0.043	ns/pF
EBI_{28}	NRD High to NLB/A0 Change	C_{NLB} = 0 pF	3.2	4.6	ns
		C_{NLB} derating	0.043	0.073	ns/pF
EBI_{29}	NRD High to A1 - A23 Change	C_{ADD} = 0 pF	2.8	6.1	ns
		C_{ADD} derating	0.043	0.076	ns/pF
EBI_{30}	NRD High to Chip Select Inactive	C_{NCS} = 0 pF	2.9	6.2	ns
		C_{NCS} derating	0.052	0.067	ns/pF

Table 7-3. EBI Read Signals

Symbol	Parameter	Conditions	Min	Max	Units
EBI_{31}	Data Setup before NRD High[6]	C_{NRD} = 0 pF	8.0		ns
		C_{NRD} derating	0.044		ns/pF
EBI_{32}	Data Hold after NRD High[6]	C_{NRD} = 0 pF	-3.1		ns
		C_{NRD} derating	-0.030		ns/pF
EBI_{33}	NRD Minimum Pulse Width[1] [3]	C_{NRD} = 0 pF	(n +1) t_{CP} - 1.9[4]		ns
		C_{NRD} derating	0.001		ns/pF
EBI_{34}	NRD Minimum Pulse Width[2] [3]	C_{NRD} = 0 pF	n x t_{CP} + (t_{CH} - 1.5)[4]		ns
		C_{NRD} derating	0.001		ns/pF

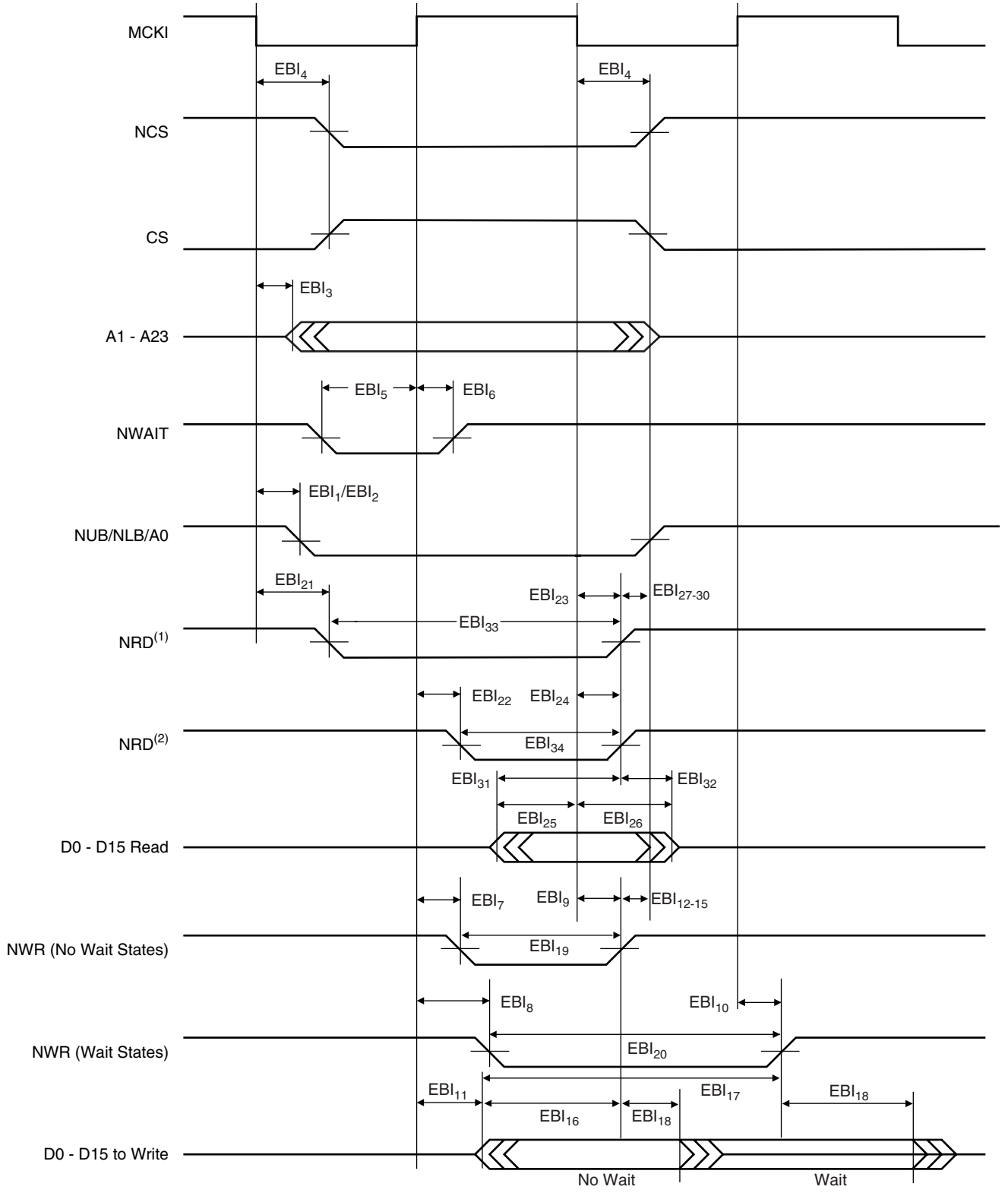
Notes:
1. Early Read Protocol.
2. Standard Read Protocol.
3. The derating factor should not be applied to t_{CH} or t_{CP}
4. n = number of standard wait states inserted.
5. Only one of these two timings, EB_{25} or EBI_{31}, needs to be met.
6. Only one of these two timings, EB_{26} or EBI_{32}, needs to be met.

Table 7-4. EBI Read and Write Control Signals. Capacitance Limitation

Symbol	Parameter	Conditions	Min	Max	Units
T_{CPLNRD}[1]	Master Clock Low Due to NRD Capacitance	C_{NRD} = 0 pF	7.3		ns
		C_{NRD} derating	0.044		ns/pF
T_{CPLNWR}[2]	Master CLock Low Due to NWR Capacitance	C_{NWR} = 0 pF	7.6		ns
		C_{NWR} derating	0.044		ns/pF

Notes:
1. If this condition is not met, the action depends on the read protocol intended for use.
   • Early Read Protocol: Programing an additional t_{DF} (Data Float Output Time) cycle.
   • Standard Read Protocol: Programming an additional t_{DF} Cycle and an additional wait state.
2. Applicable only for chip select programmed with 0 wait state. If this condition is not met, at least one wait state must be programmed.

Figure 7-1. EBI Signals Relative to MCKI



Notes: 1. Early Read Protocol.
2. Standard Read Protocol.

7.2 Peripheral Signals

7.2.1 USART Signals

The inputs have to meet the minimum pulse width and period constraints shown in Table 7-5 and Table 7-6, and represented in Figure 7-2.

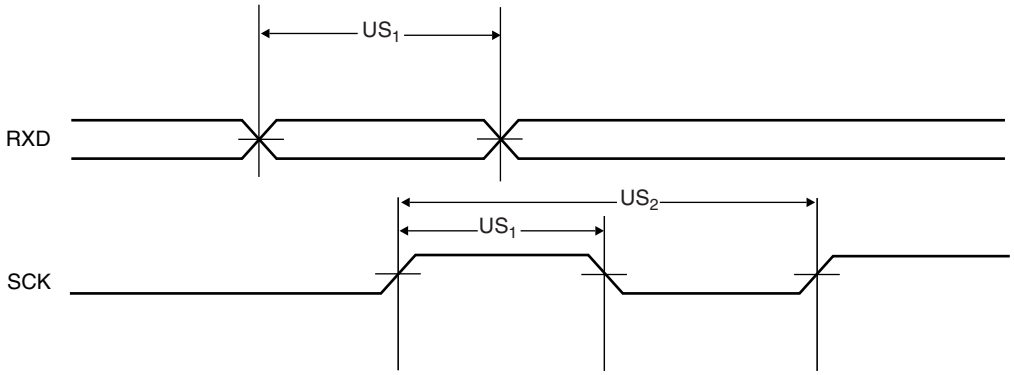
Table 7-5. USART Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
US_1	SCK/RXD Minimum Pulse Width	$5(t_{CP}/2)$	ns

Table 7-6. USART Minimum Input Period

Symbol	Parameter	Min Input Period	Units
US_2	SCK Minimum Input Period	$9(t_{CP}/2)$	ns

Figure 7-2. USART Signals



7.2.2 Timer/Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CP})$ in Waveform Event Detection mode and $4(t_{CP})$ in Waveform Total-count Detection mode. The inputs have to meet the minimum pulse width and minimum input period shown in Table 7-7 and Table 7-8, and as represented in Figure 7-3.

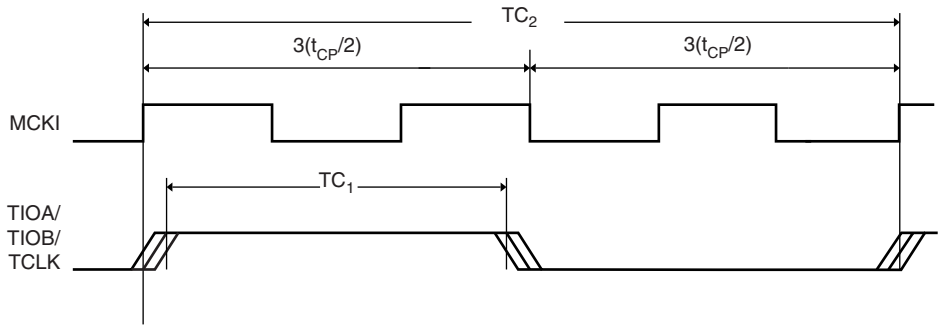
Table 7-7. Timer Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
TC_1	TCLK/TIOA/TIOB Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 7-8. Timer Input Minimum Period

Symbol	Parameter	Min Input Period	Units
TC_2	TCLK/TIOA/TIOB Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 7-3. Timer Input



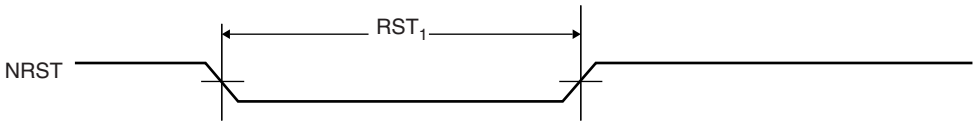
7.2.3 Reset Signals

A minimum pulse width is necessary, as shown in Table 7-9 and as represented in Figure 7-4.

Table 7-9. Reset Minimum Pulse Width

Symbol	Parameter	Min Pulse-width	Units
RST_1	NRST Minimum Pulse Width	$10(t_{CP})$	ns

Figure 7-4. Reset Signal



Only the NRST rising edge is synchronized with MCKI. The falling edge is asynchronous.

7.2.4 Advanced Interrupt Controller Signals

Inputs have to meet the minimum pulse width and minimum input period shown in Table 7-10 and Table 7-11 and represented in Figure 7-5.

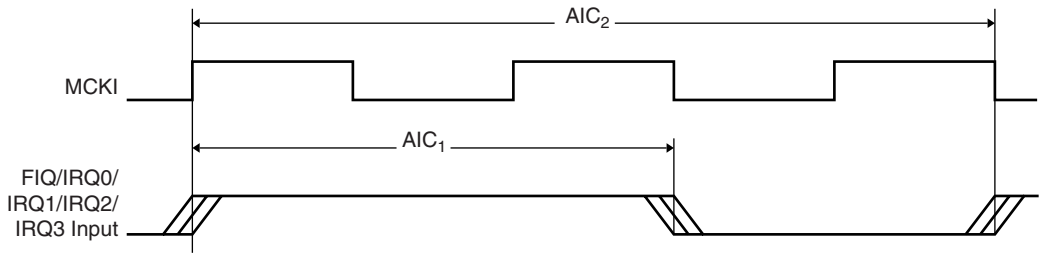
Table 7-10. AIC Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
AIC_1	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 7-11. AIC Input Minimum Period

Symbol	Parameter	Min Input Period	Units
AIC_2	AIC Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 7-5. AIC Signals



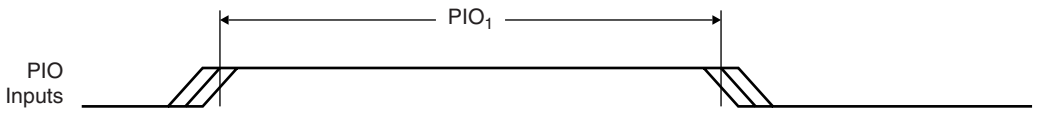
7.2.5 Parallel I/O Signals

The inputs have to meet the minimum pulse width shown in Table 7-12 and represented in Figure 7-6.

Table 7-12. PIO Input Minimum Pulse Width

Symbol	Parameter	Min Pulse Width	Units
PIO_1	PIO Input Minimum Pulse Width	$3(t_{CP}/2)$	ns

Figure 7-6. PIO Signal

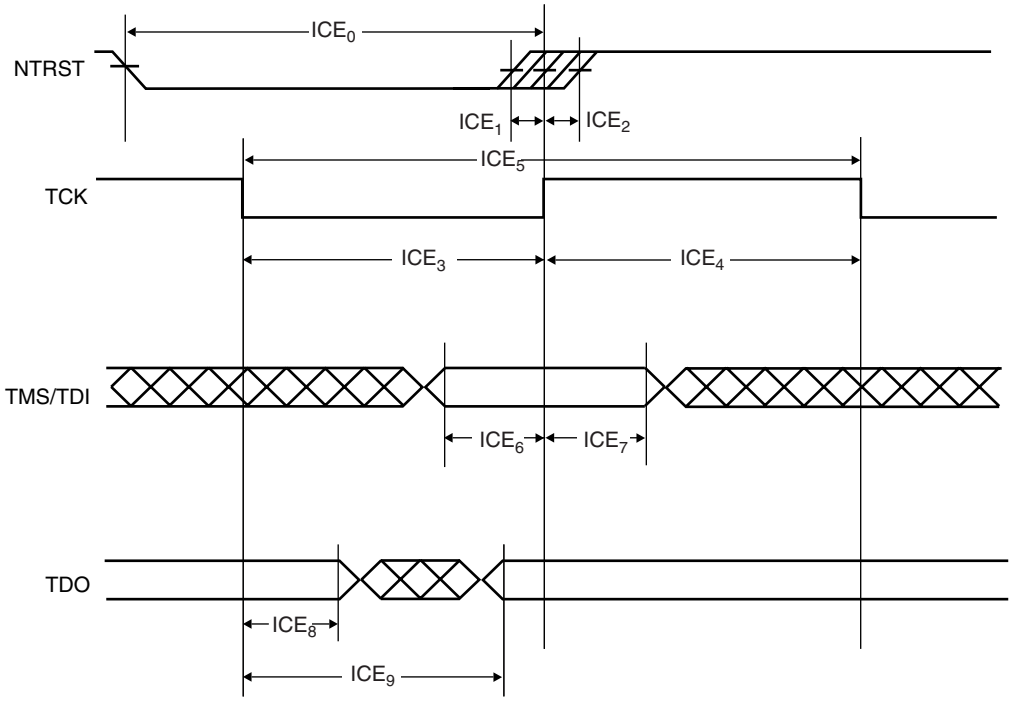


7.2.6 ICE Interface Signals

Table 7-13. ICE Interface Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
ICE_0	NTRST Minimum Pulse Width		10.9		ns
ICE_1	NTRST High Recovery to TCK High		0.9		ns
ICE_2	NTRST High Removal from TCK High		-0.3		ns
ICE_3	TCK Low Half-period		23.5		ns
ICE_4	TCK High Half-period		22.7		ns
ICE_5	TCK Period		46.1		ns
ICE_6	TDI, TMS Setup before TCK High		0.4		ns
ICE_7	TDI, TMS Hold after TCK High		0.4		ns
ICE_8	TDO Hold Time	C_{TDO} = 0 pF	3.3		ns
		C_{TDO} derating	0.001		ns/pF
ICE_9	TCK Low to TDO Valid	C_{TDO} = 0 pF		7.4	ns
		C_{TDO} derating		0.28	ns/pF

Figure 7-7. ICE Interface Signal



Revision History

Version	page	Comments
1795A		10-Dec-01 First Issue
1795B		7-Aug-2002
	page 2	Absolute Maximum Ratings: changed
	page 2	Table 1. DC Characteristics: changed
	page 3	Table 2. Power Consumption: changed
	page 3	Table 3. Power Consumption per Peripheral: changed
	page 9	Table 7. Master Waveclock Parameters: changed
1795C		24-Mar-2004
	page 1	Features: Change to “Fully Static Operation” values.
	page 9	Figure 4. Clock Waveform: t_R and t_F removed, t_{CL} measurement changed.
	page 13	Table 12. Footnote 5 changed and footnote 6 added to clarify selection needs.
1795D		22-Oct-04
	page 6	Change to Timing Results (CSR 04-320)
	page 9	Change to Table 7 and Figure 4 (CSR 04-320)
1795E		12-Dec-05
	all	Reformatted in Atmel template version 5.2. Numbering properties are changed as a result.
	page 9	Table 6-1, “Master Clock Waveform Parameters,” note deleted. (CSR 05-446)

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