Transcend 40-Pin IDE Flash Module
128MB ~ 8GB

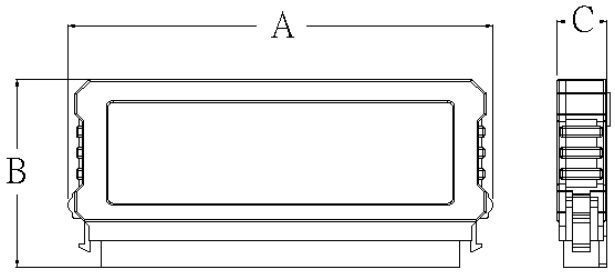
Description

With an IDE interface and strong data retention ability, 40-Pin IDE Flash Modules are ideal for use in the harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Features

- RoHS compliant products
- Storage Capacity: 128MB ~ 8GB
- Operating Voltage: 3.3V±5% or 5V±10%
- Operating Temperature: 0°C ~ 70°C
- Endurance: 2,000,000 Program/Erase cycles
- MTBF: 1,000,000 hours
- Durability of Connector: 10,000 times
- Fully compatible with devices and OS that support the IDE standard (pitch = 2.54mm)
- Built-in ECC function assures high reliability of data transfer
- Supports up to Ultra DMA Mode 4
- Supports PIO Mode 6

Placement



Dimensions

Side	Millimeters	Inches
A	61.00 ± 0.40	2.402 ± 0.016
B	27.10 ± 0.50	1.067 ± 0.020
C	7.10 ± 0.20	0.280 ± 0.008

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Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	-RESET	11	HD3	21	DMARQ	31	IREQ
02	GND	12	HD12	22	GND	32	IOIS16B
03	HD7	13	HD2	23	IOWB	33	HA1
04	HD8	14	HD13	24	GND	34	PDIAGB
05	HD6	15	HD1	25	IORB	35	HA0
06	HD9	16	HD14	26	GND	36	HA2
07	HD5	17	HD0	27	IORDY	37	CE1B
08	HD10	18	HD15	28	NC	38	CE2B
09	HD4	19	GND	29	-DMACK	39	DASPB
10	HD11	20	VCC	30	GND	40	GND

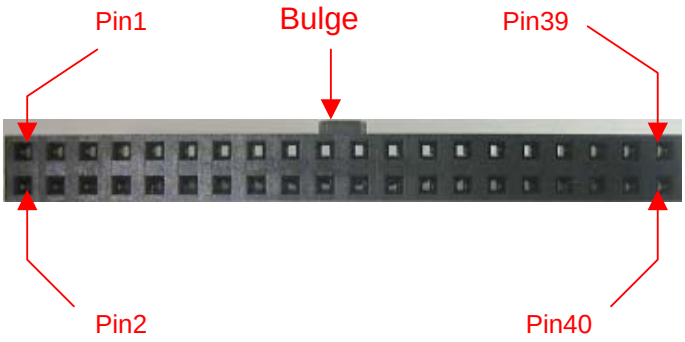
Input Power

The 40-Pin IDE Flash Module offers 2 ways to get input power, either via the small power cord or through Pin 20 of the IDE connector. If Pin 20 of the IDE connector is defined as NC (No Connect), then the 40-Pin IDE Flash Module must be directly connected to your system's power supply. If Pin 20 of the IDE connector is defined as VCC, then the 40-Pin IDE Flash Module can get necessary power without use of the power cord.

Pin Definition

Symbol	Function
HD0 ~ HD15	Data Bus (Bi-directional)
HA0 ~ HA2	Address Bus (Input)
-RESET	Device Reset (Input)
IORB	Device I/O Read (Input)
IOWB	Device I/O Write (Input)
IOIS16B	Transfer Type 8/16 bit (Output)
CE1B, CE2B	Chip Select (Input)
PDIAGB	Pass Diagnostic (Bi-directional)
DASPB	Disk Active/Slave Present (Bi-directional)
DMARQ	DMA request
-DMACK	DMA acknowledge
IORDY	I/O channel ready
IREQ	Interrupt Request (Output)
NC	No Connection
GND	Ground
VCC	Vcc Power Input

Pin Layout



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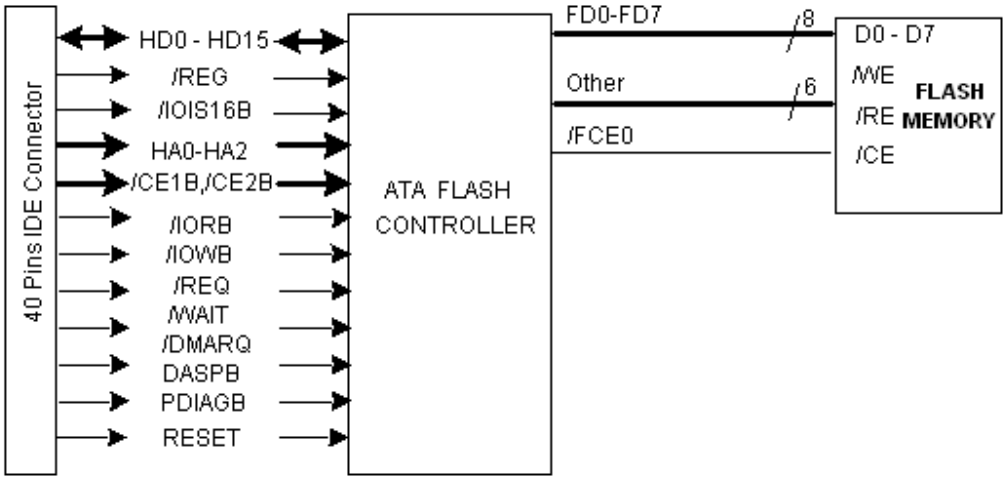
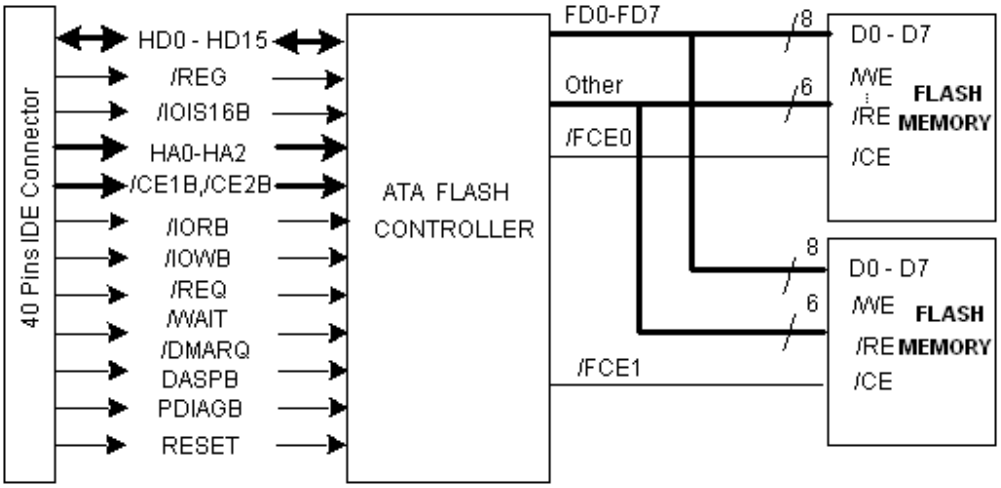
Block Diagram

With 1 pcs of Flash Memory:



With 2 pcs of Flash Memory:



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD-VSS	DC Power Supply	-0.6	+6	V
Ta	Operating Temperature	0	+70	°C
Tst	Storage Temperature	-40	+85	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VDD	Power supply	3.0	5.5	V
VIN	Input voltage	0	VDD+0.3	V
Ta	Operating Temperature	0	+70	°C

DC Characteristics (Ta=0 oC to +70 oC, Vcc = 3.3V ±10%)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	VIH	--	2	--	--	V
	VIL	--	--	--	0.2 x Vcc	V
Output Voltage	VOH	IOH = 4,8mA	Vcc – 0.8	--	--	V
	VOL	IOL = 4,8mA	--	--	0.4	V
Input leakage current	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep current	ISP	--	--	0.5	1	mA

■ True IDE Mode

The card can be configured in a True IDE This card is configured in this mode only when the -OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operations to the task file and data register are allowed. The default operation of the data register is 16-bit mode. The card permits 8-bit accessed if the user issued a Set Feature Command to put the device in 8-bit mode.

(1) True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	High-Z	High-Z
Standby mode	H	H	x	x	x	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

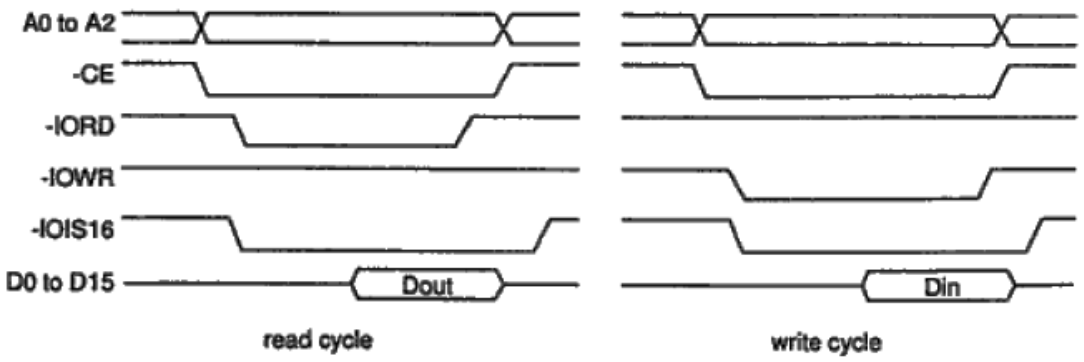
Note: x: L or H

(2) True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	don't care	don't care
Standby mode	H	H	x	x	x	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: x: L or H

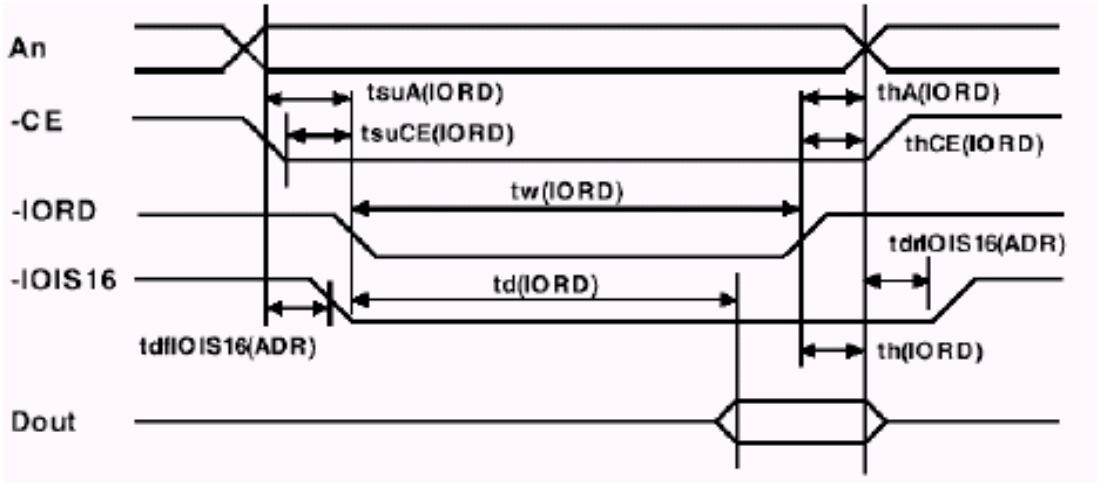
(3) True IDE Mode I/O Access Timing Example



True IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after IORD	td(IORD)	—	—	50	ns
Data hold following IORD	th(IORD)	5	—	—	ns
IORD width time	tw(IORD)	70	—	—	ns
Address setup before IORD	tsuA(IORD)	15	—	—	ns
Address hold following IORD	thA(IORD)	10	—	—	ns
CE setup before IORD	tsuCE(IORD)	5	—	—	ns
CE hold following IORD	thCE(IORD)	10	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

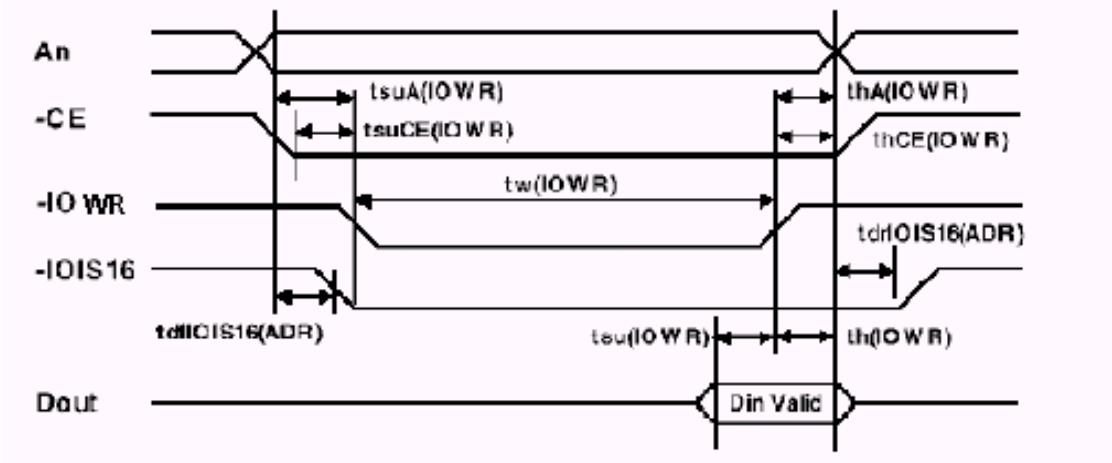
True IDE Mode Access Read Timing



True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	20	—	—	ns
Data hold following IOWR	th(IOWR)	10	—	—	ns
IOWR width time	tw(IOWR)	50	—	—	ns
Address setup before IOWR	tsuA(IOWR)	15	—	—	ns
Address hold following IOWR	thA(IOWR)	10	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	5	—	—	ns
CE hold following IOWR	thCE(IOWR)	10	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

True IDE Mode Access Write Timing



■ IDE Mode Access Read/Write AC Characteristics

CFA Rev 2.0 and ATA/ATAPI-5 Defined True IDE Mode I/O Timing Specification (*1)

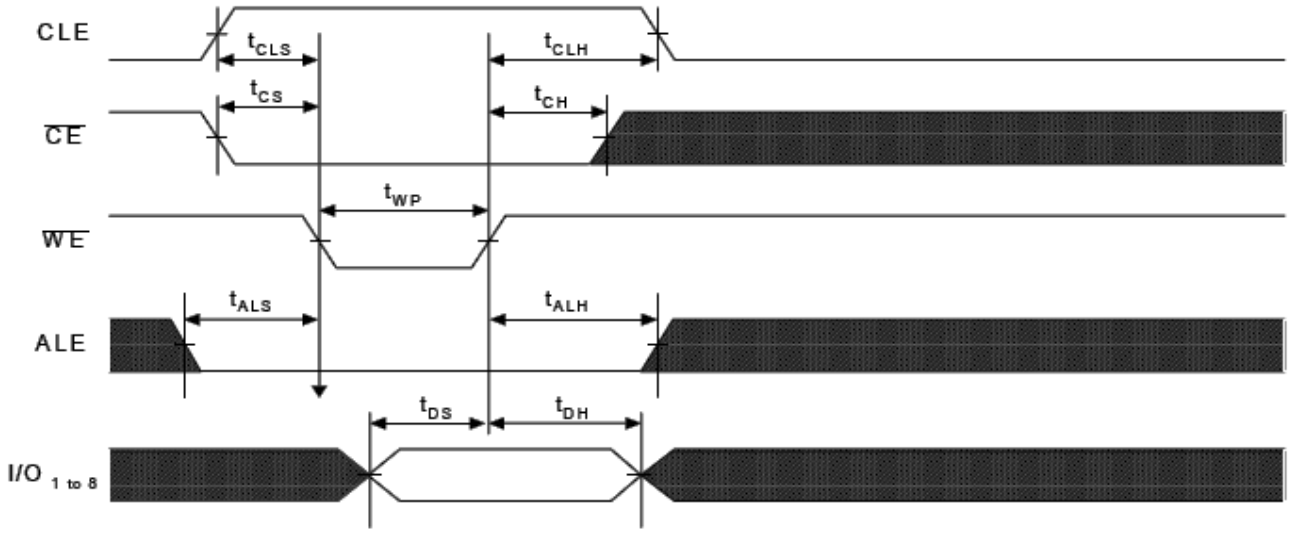
Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Data setup before IOWR (min)	tsu(IOWR)	60	45	30	30	20	ns
Data hold following IOWR (min)	th(IOWR)	30	20	15	10	10	ns
Data delay after IORD (max)	td(IORD)	115	90	80	60	50	ns
Data hold following IORD (min)	th(IORD)	5	5	5	5	5	ns
IOWR/IORD width time (min)	tw(IOWR/IORD)	165	125	100	80	70	ns
Address setup before IOWR/IORD (min)	tsuA(IOWR/IORD)	70	50	30	30	25	ns
Address hold following IOWR/IORD (min)	thA(IOWR/IORD)	20	15	10	10	10	ns
CE setup before IOWR/IORD (min)	tsuCE(IOWR/IORD)	70	50	30	30	25	ns
CE hold following IOWR/IORD (min)	thCE(IOWR/IORD)	20	15	10	10	10	ns
IOIS16 delay falling from address (max)	tdfIOIS16(ADR)	90	50	40	n/a (*3)	n/a (*3)	ns
IOIS16 delay rising from address (max)	tsfIOIS16(ADR)	60	45	30	n/a (*3)	n/a (*3)	ns

Supported True IDE Mode I/O Timing Specification (*2)

Parameter	Symbol	Controller Supported	Unit
Data setup before IOWR (min)	tsu(IOWR)	20	ns
Data hold following IOWR (min)	Th(IOWR)	10	ns
Data delay after IORD (max)	Td(IORD)	50	ns
Data hold following IORD (min)	Th(IORD)	5	ns
IOWR/ IORD width time (min)	tw(IOWR/ IORD)	70	ns
Address setup before IOWR/IORD (min)	tsuA(IOWR/IORD)	15	ns
Address hold following IOWR/IORD (min)	thA(IOWR/IORD)	10	ns
CE setup before IOWR/IORD (min)	TsuCE(IOWR/IORD)	5	ns
CE hold following IOWR/IORD (min)	thCE(IOWR/IORD)	10	ns
IOIS16 delay falling from address (max)	tdfIOIS16(ADR)	35	ns
IOIS16 delay rising from address (max)	tsfIOIS16(ADR)	35	ns

Note: This timing apply only to modes 0, 1 and 2. For modes 3 and 4, the "IOIS16" signal is not valid.

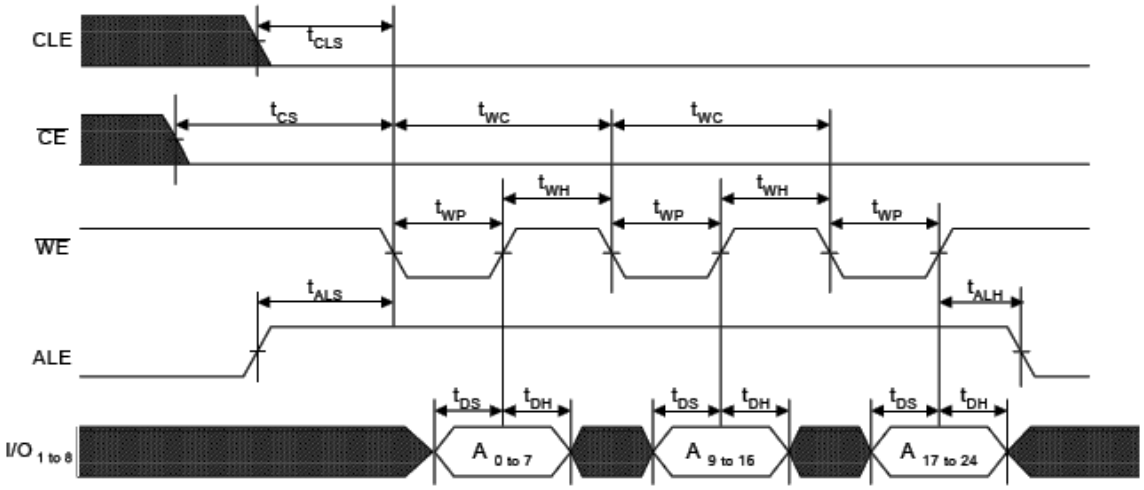
FLASH Interface Command write Timing：



AC Timing Characteristics -Flash side (T_{OPR} = 0°C to 70°C, T_{OPRI} = -40°C to 85°C, Vcc = 3.0V to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Setup Time	t_{CLS}	0	0		ns
CLE Output Hold Time	t_{CLH}	10	34		ns
CE Output Setup Time	t_{CS}	0	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
ALE Output Setup Time	t_{ALS}	0	>34		ns
ALE Output Hold Time	t_{ALH}	10	>34		ns
Data Output Setup Time	t_{DS}	20	25		ns
Data Output Hold Time	t_{DH}	10	40		ns

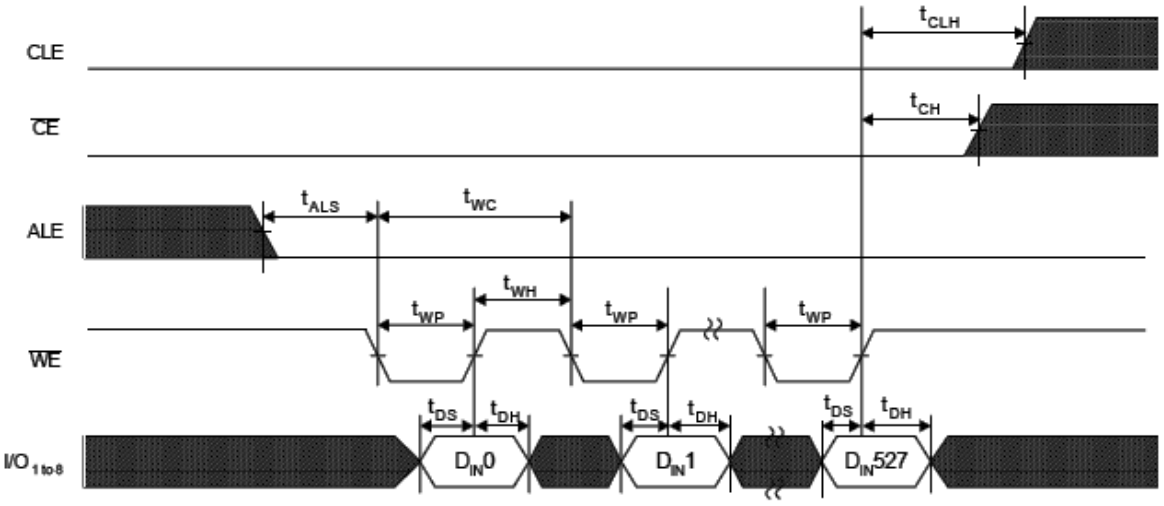
FLASH Interface Address Write Timing：



AC Timing Characteristics -Flash side (T_{OPR} = 0°C to 70°C, T_{OPRI} = -40°C to 85°C, Vcc = 3.0V to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Setup Time	t_{CLS}	0	>34		ns
CLE Output Hold Time	t_{CLH}	10	>34		ns
CE Output Setup Time	t_{CS}	0	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
WE Output High Hold Time	t_{WH}	15	34		ns
ALE Output Setup Time	t_{ALS}	0	0		ns
ALE Output Hold Time	t_{ALH}	10	34		ns
Data Output Setup Time	t_{DS}	20	25		ns
Data Output Hold Time	t_{DH}	10	40		ns
Flash Write Cycle Time	t_{WC}	50	68		ns

FLASH Interface DATA Write Timing：



AC Timing Characteristics -Flash side (T_{OPR} = 0°C to 70°C, T_{OPRI} = -40°C to 85°C, Vcc = 3.0V to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Hold Time	t_{CLH}	10	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
WE Output High Hold Time	t_{WH}	15	34		ns
ALE Output Setup Time	t_{ALS}	0	>34		ns
Data Output Setup Time	t_{DS}	20	40		ns
Data Output Hold Time	t_{DH}	10	20		ns
Flash Write Cycle Time	t_{WC}	50	68		ns

■ **True IDE Mode I/O map**

-CE2	-CE1	A2	A1	A0	-IORD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

(1) Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

(2) Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0"(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	"0"	IDNF	"0"	ABRT	"0"	AMNF

bit	Name	Function
7	BBK(Bad Block detected)	This bit is set when a Bad Block is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT(ABoRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready, Write fault, Invalid command, etc.)
0	AMNF(Address Mark Not Found)	This bit is set in case of a general error.

(3) Feature register: This register is write only register, and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

(4) Sector count register:

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

(5) Sector number register: This register contains the starting sector number, which is started by following sector transfer command.

Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

(6) Cylinder low register: This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

(7) Cylinder high register: This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

(8) Drive head register: This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolete	LBA	Obsolete	DRV	Head number bit[3:0]			

bit	Name	Function
7	Obsolete bit	This bit is set to "1" normally.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector(CHS)or Logical Block Address (LBA) mode. When LBA =0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00：Sector Number Register D7-D0. LBA15-LBA08：Cylinder Low Register D7-D0. LBA23-LBA16：Cylinder High Register D7-D0. LBA27-LBA24：Drive / Head Register bits HS3-HS0.
5	Obsolete bit	This bit is set to "1" normally.
4	DRV(DRiVe select)	This bit is used for selecting the Master Drive or Slave Drive in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3	Head number	These bits are used for selecting the Head number for the following command. Bit 3 is MSB.

(9) Status register: This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY(BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1" , other bits in this register are invalid.
6	DRDY(Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF(Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC(Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ(Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR(CORRected data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX(InDeX)	This bit is always set to "0".
0	ERR(ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

(10) Alternate status register: This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that –IREQ is not negated when data read.

(11) Command register: This register is write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card is Ready state.

(12) Device control register: This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	x	x	x	1	SRST	nIEN	0

Bit	Name	Function
7to 4	X	don't care
3	1	This bit is set to "1".
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN(Interrupt Enable)	This bit is used for enabling –IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

(13) Drive Address register: This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Bit	Name	Function
7	X	This bit is unknown. It remains tri-state, when host read.
6	nWTG(WriTing Gate)	This bit is set 0.
5 to 2	nHS3-0(Head Select3-0)	These bits is the negative value of Head Select bits(bit 3 to 0)in Drive/Head register.
1	nDS1(Idrive Select1)	This bit is 0, when drive 1 is selected.
0	nDS0(Idrive Select0)	This bit is 0, when drive 0 is selected.

ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LSB
1	Check power mode	E5H or 98H	–	–	–	–	Y	–	–
2	Execute drive diagnostic	90H	–	–	–	–	Y	–	–
3	Erase sector(s)	C0H	–	Y	Y	Y	Y	Y	Y
4	Format track	50H	–	Y	–	Y	Y	Y	Y
5	Identify Drive	ECH	–	–	–	–	Y	–	–
6	Idle	E3H or 97H	–	Y	–	–	Y	–	–
7	Idle immediate	E1H or 95H	–	–	–	–	Y	–	–
8	Initialize drive parameters	91H	–	Y	–	–	Y	Y	–
9	Read buffer	E4H	–	–	–	–	Y	–	–
10	Read multiple	C4H	–	Y	Y	Y	Y	Y	Y
11	Read long sector	22H,23H	–	–	Y	Y	Y	Y	Y
12	Read sector(s)	20H,21H	–	Y	Y	Y	Y	Y	Y
13	Read verify sector(s)	40H, 41H	–	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	–	–	–	–	Y	–	–
15	Request sense	03H	–	–	–	–	Y	–	–
16	Seek	7XH	–	–	Y	Y	Y	Y	Y
17	Set features	EFH	Y	–	–	–	Y	–	–
18	Set multiple mode	C6H	–	Y	–	–	Y	–	–
19	Set sleep mode	E6H or 99H	–	–	–	–	Y	–	–
20	Stand by	E2H or 96H	–	–	–	–	Y	–	–
21	Stand by immediate	E0H or 94H	–	–	–	–	Y	–	–
22	Translate sector	87H	–	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	–	–	–	–	Y	Y	–
24	Write buffer	E8H	–	–	–	–	Y	–	–
25	Write long sector	32H or 33H	–	–	Y	Y	Y	Y	Y
26	Write multiple	C5H	–	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	–	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	–	Y	Y	Y	Y	Y	Y
29	Write sector w/o erase	38H	–	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	–	Y	Y	Y	Y	Y	Y

Note： FR：Feature Register

SC：Sector Count register (00H to FFH)

SN：Sector Number register (01H to 20H)

CY：Cylinder Low/High register

DR：Drive bit of Drive/Head register

HD：Head No.(0 to 3) of Drive/Head register

PIO data in command protocol

This class includes:

- CFA TRANSLATE SECTOR
- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ MULTIPLE
- READ SECTOR(S)
- SMART READ DATA

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 12 describes the protocol of a PIO data in command. This description does not include all possible error conditions.

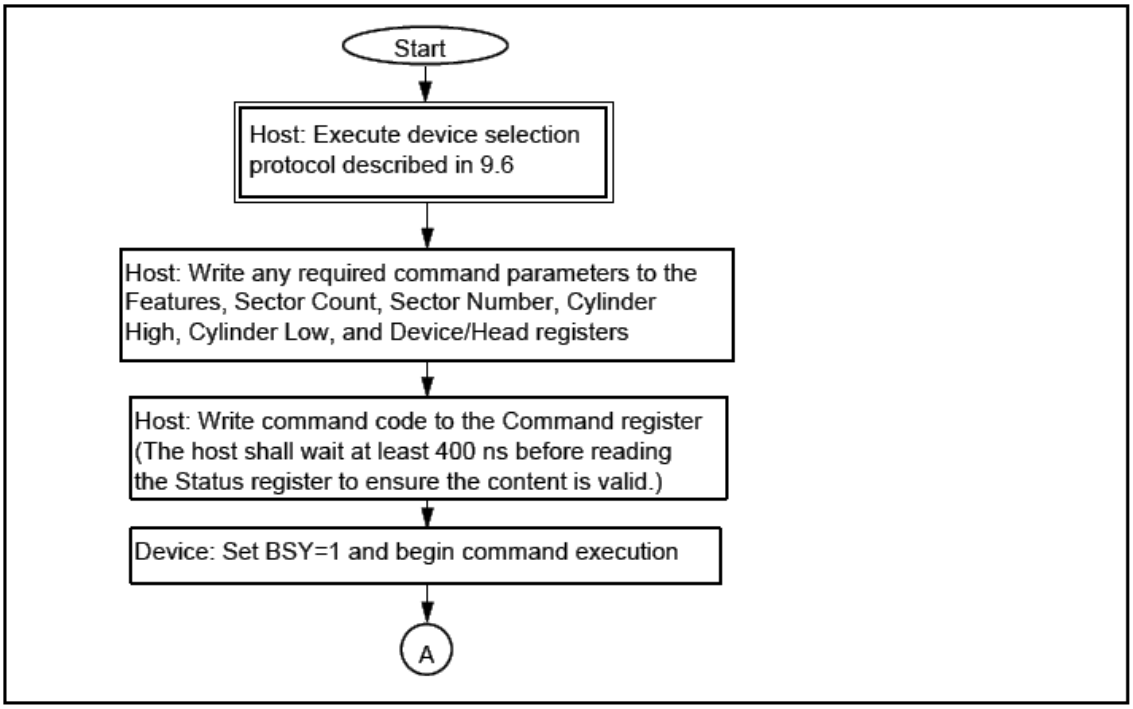


Figure 12 – PIO data in command protocol *(continued)*

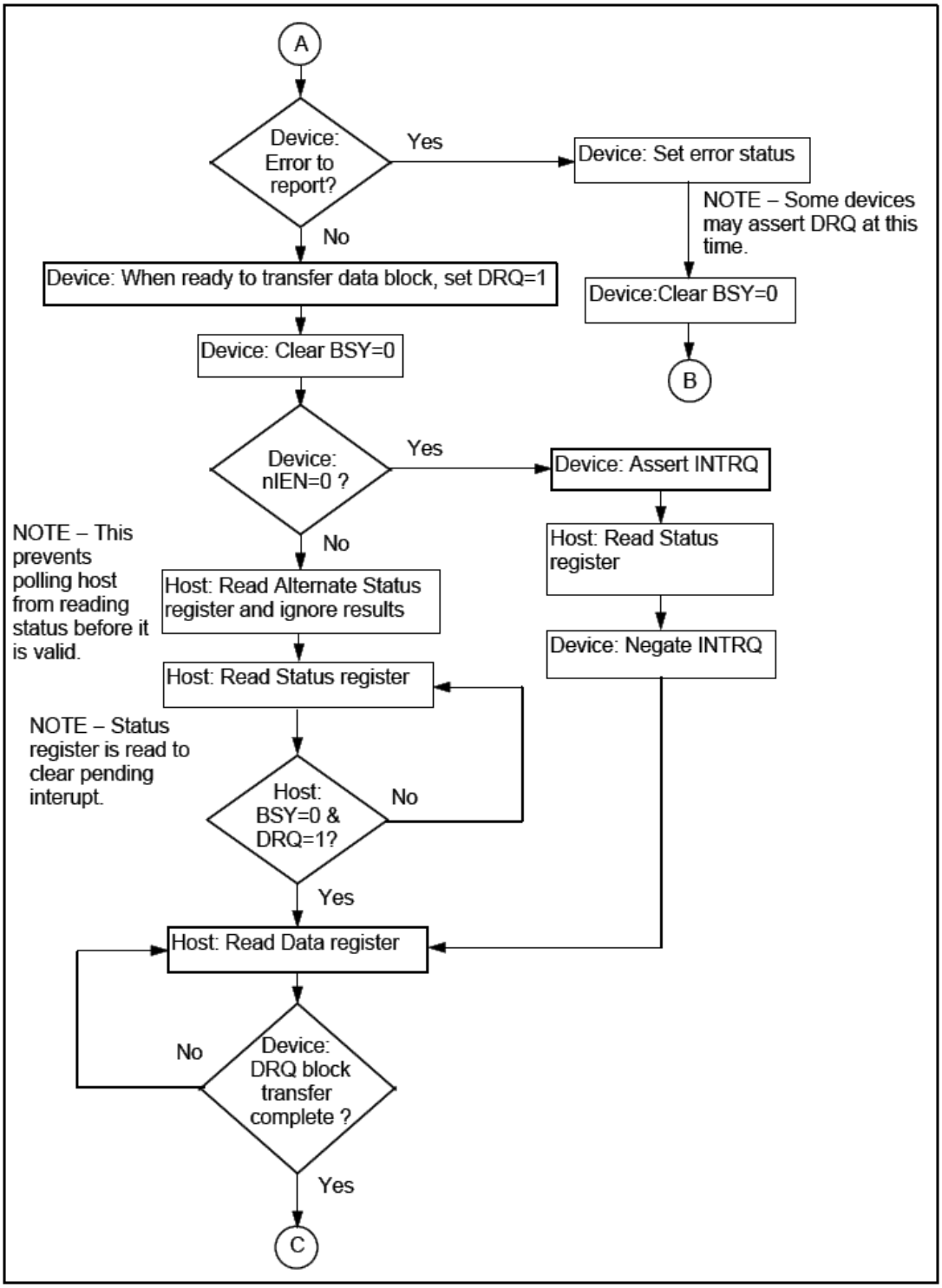


Figure 12 – PIO data in command protocol *(continued)*

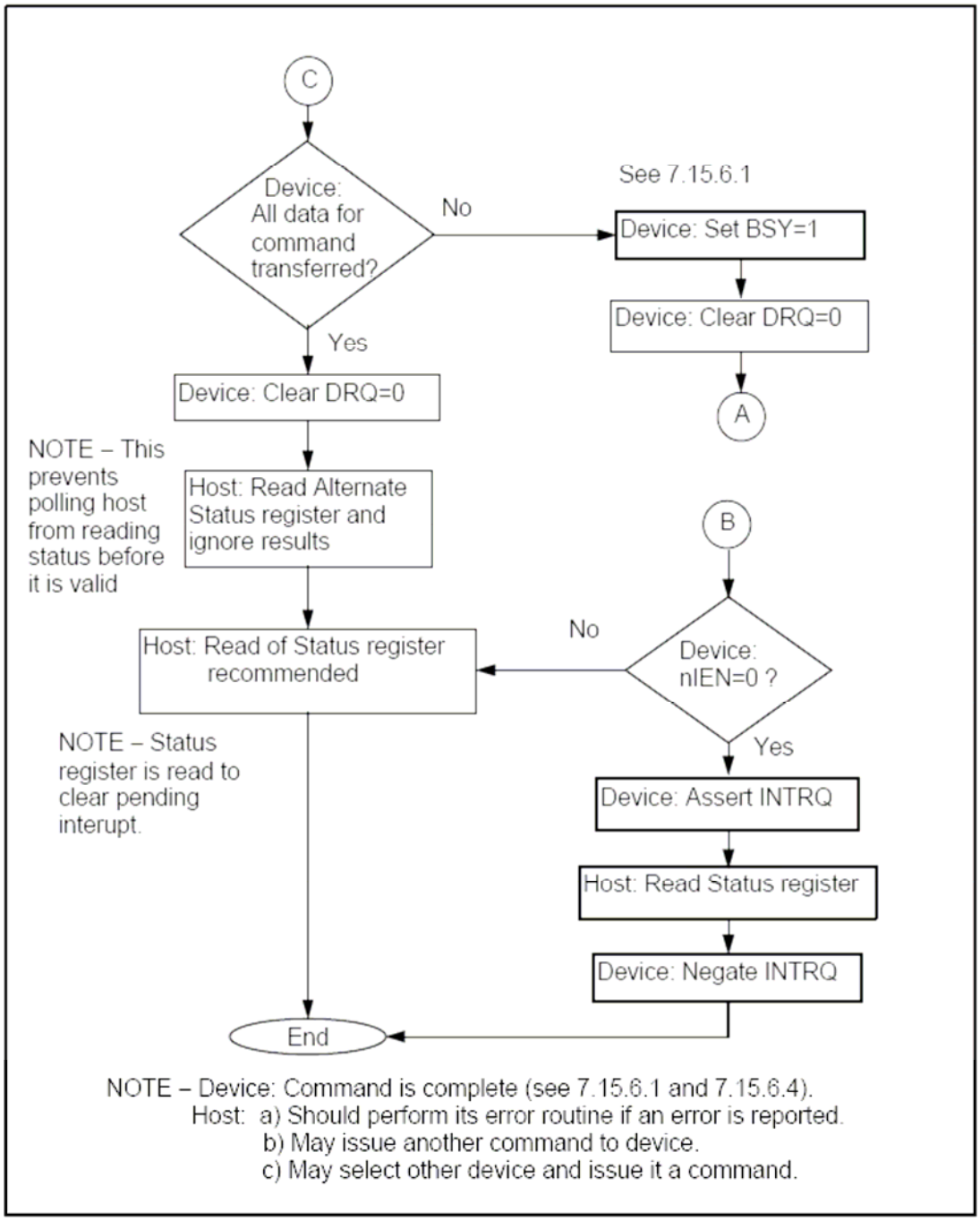


Figure 12 – PIO data in command protocol*(concluded)*

PIO data out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 13 describes the protocol of a PIO data out command. This description does not include all possible error conditions.

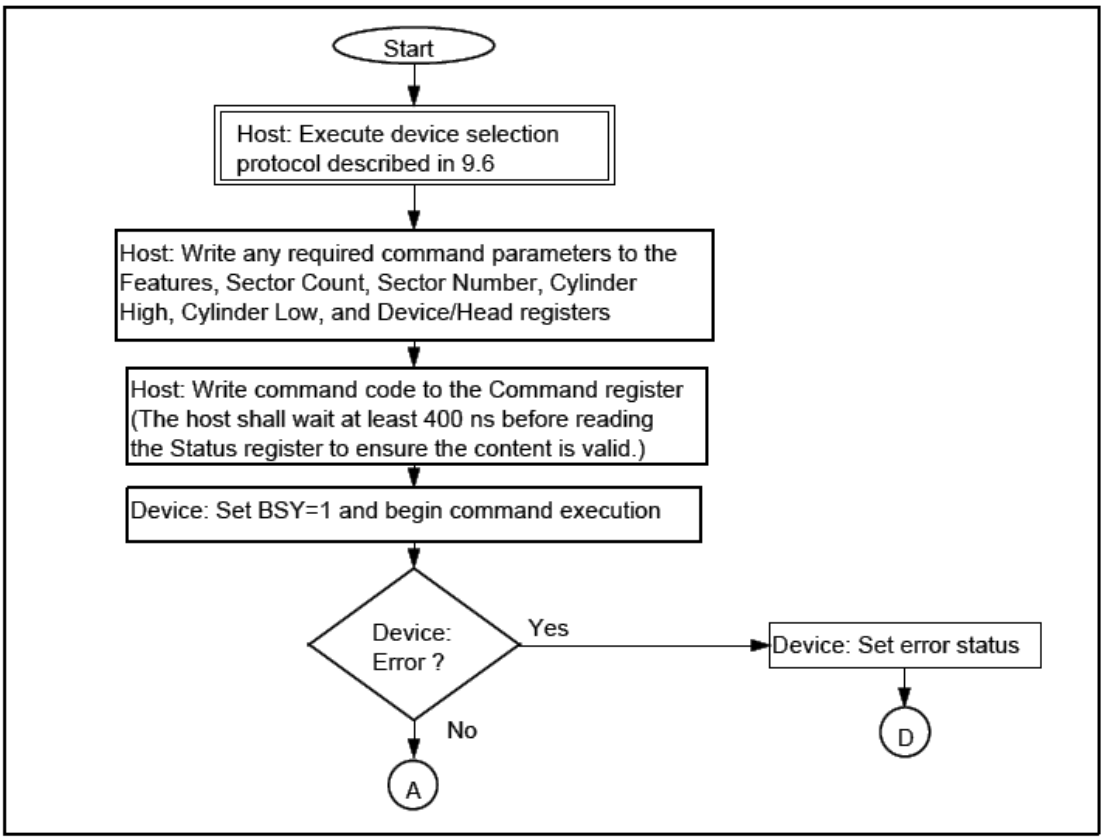


Figure 13 – PIO data out command protocol *(continued)*

PIO data out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 13 describes the protocol of a PIO data out command. This description does not include all possible error conditions.

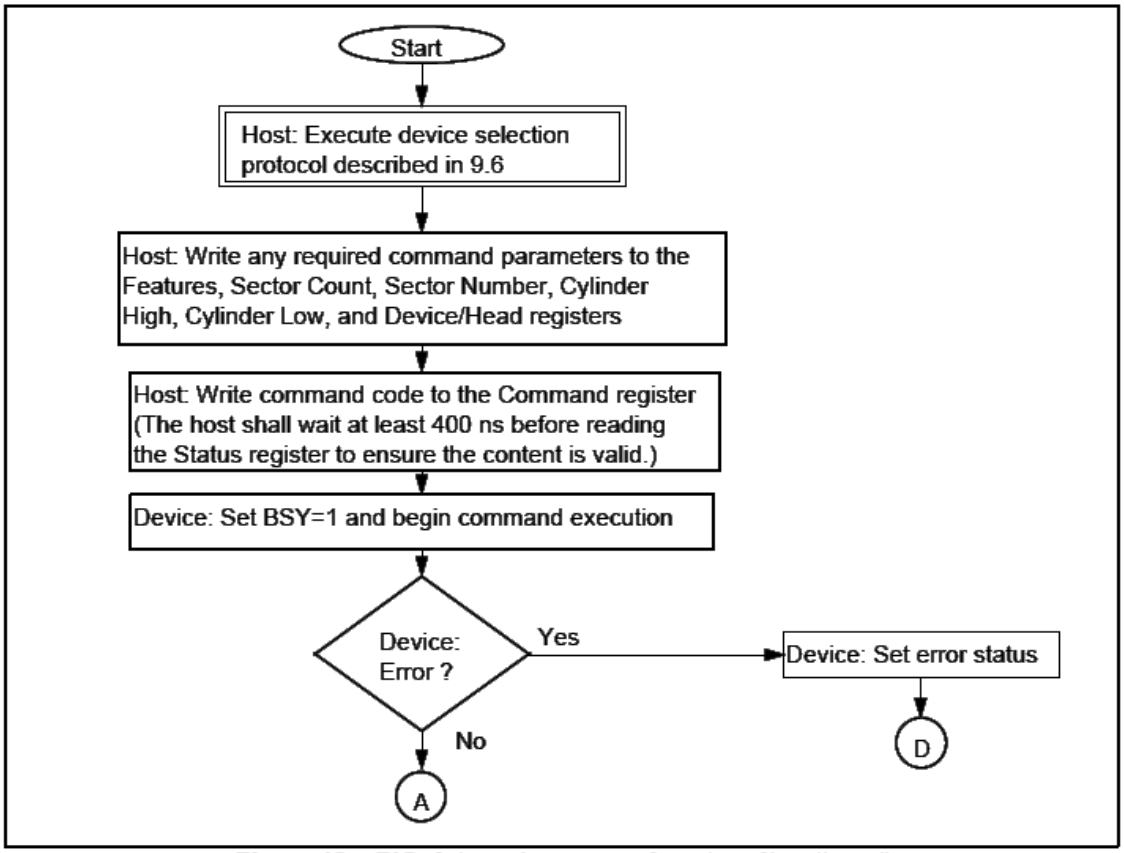


Figure 13 – PIO data out command protocol *(continued)*

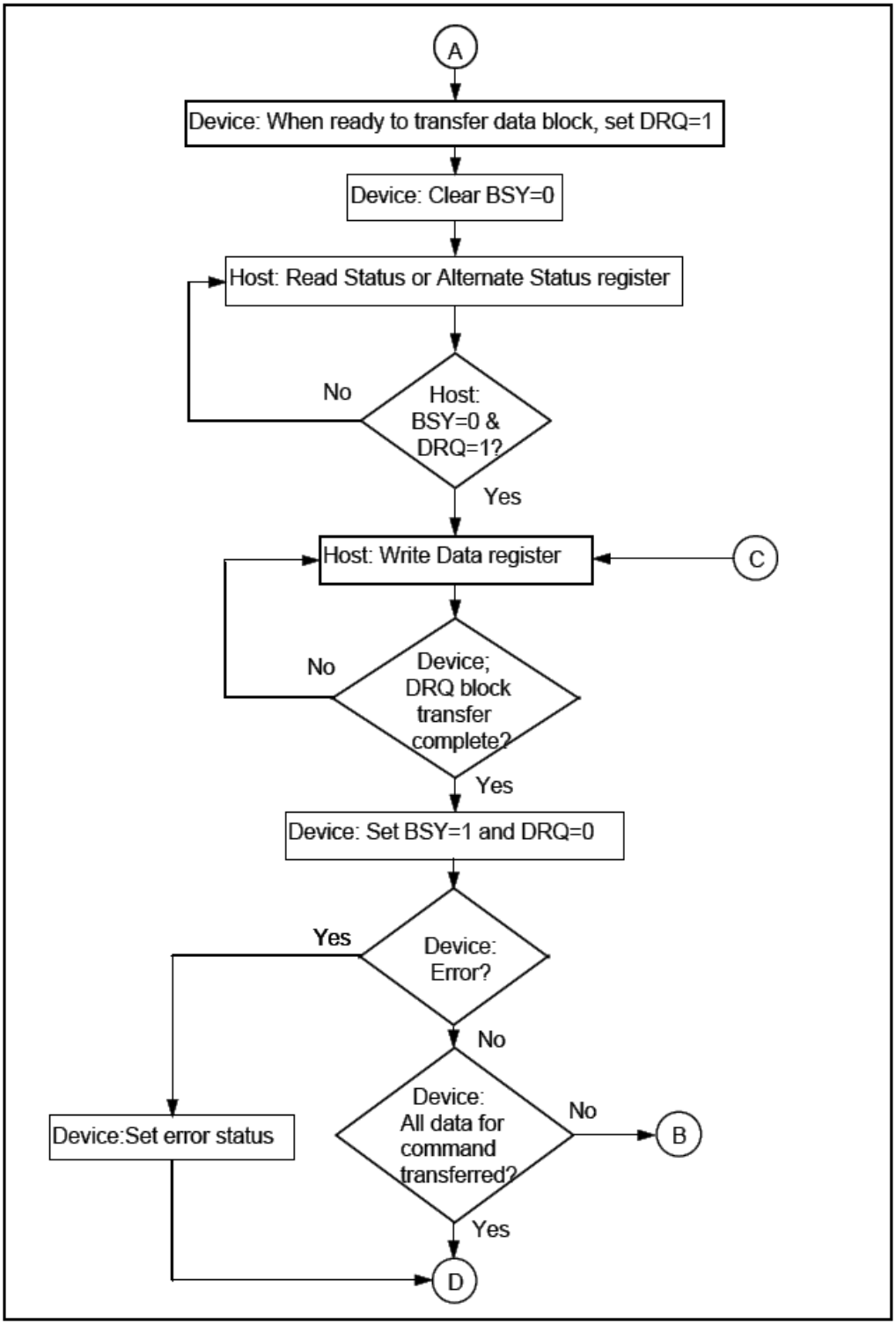


Figure 13 – PIO data out command protocol *(continued)*

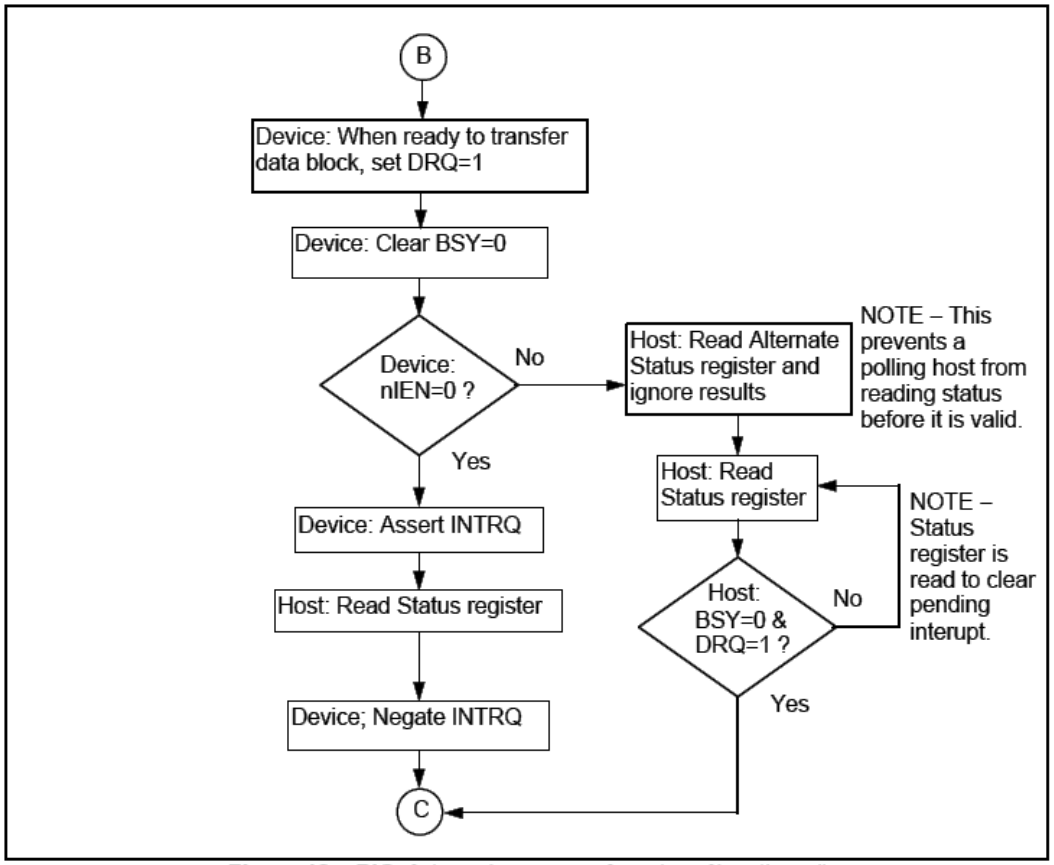


Figure 13 – PIO data out command protocol *(continued)*

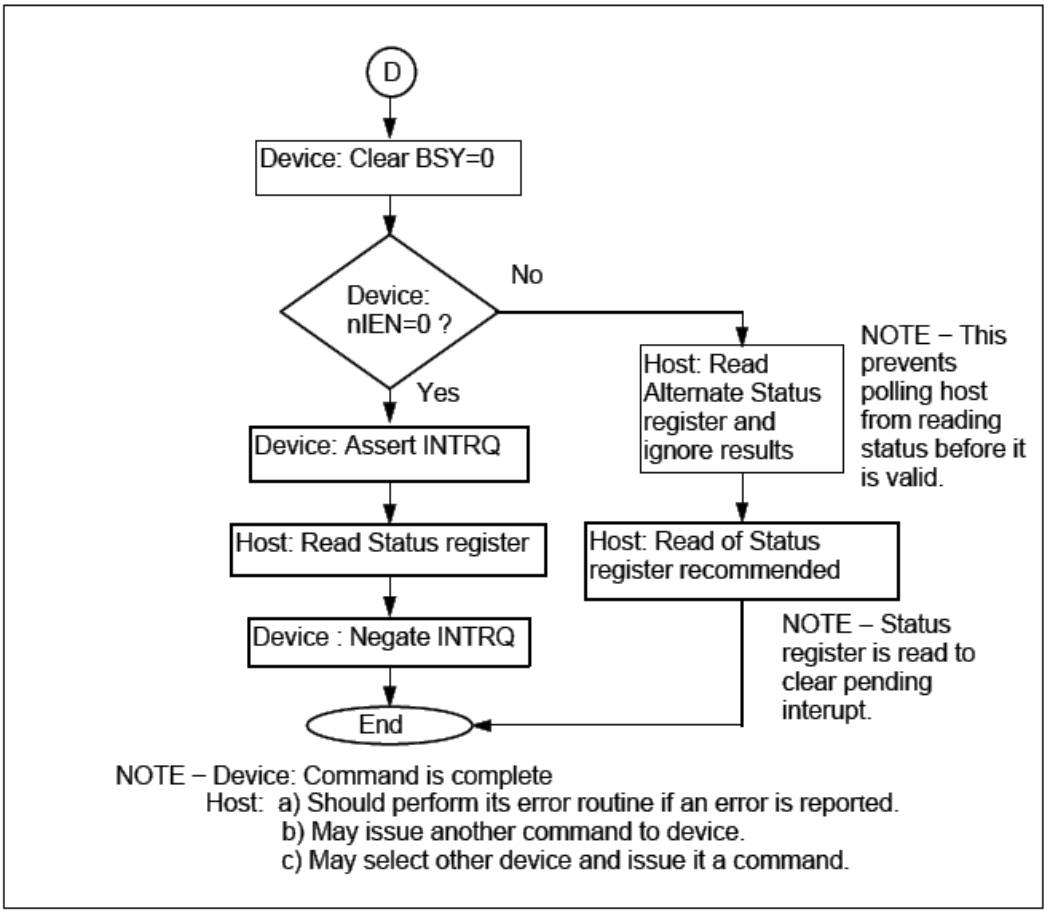


Figure 13 – PIO data out command protocol *(concluded)*

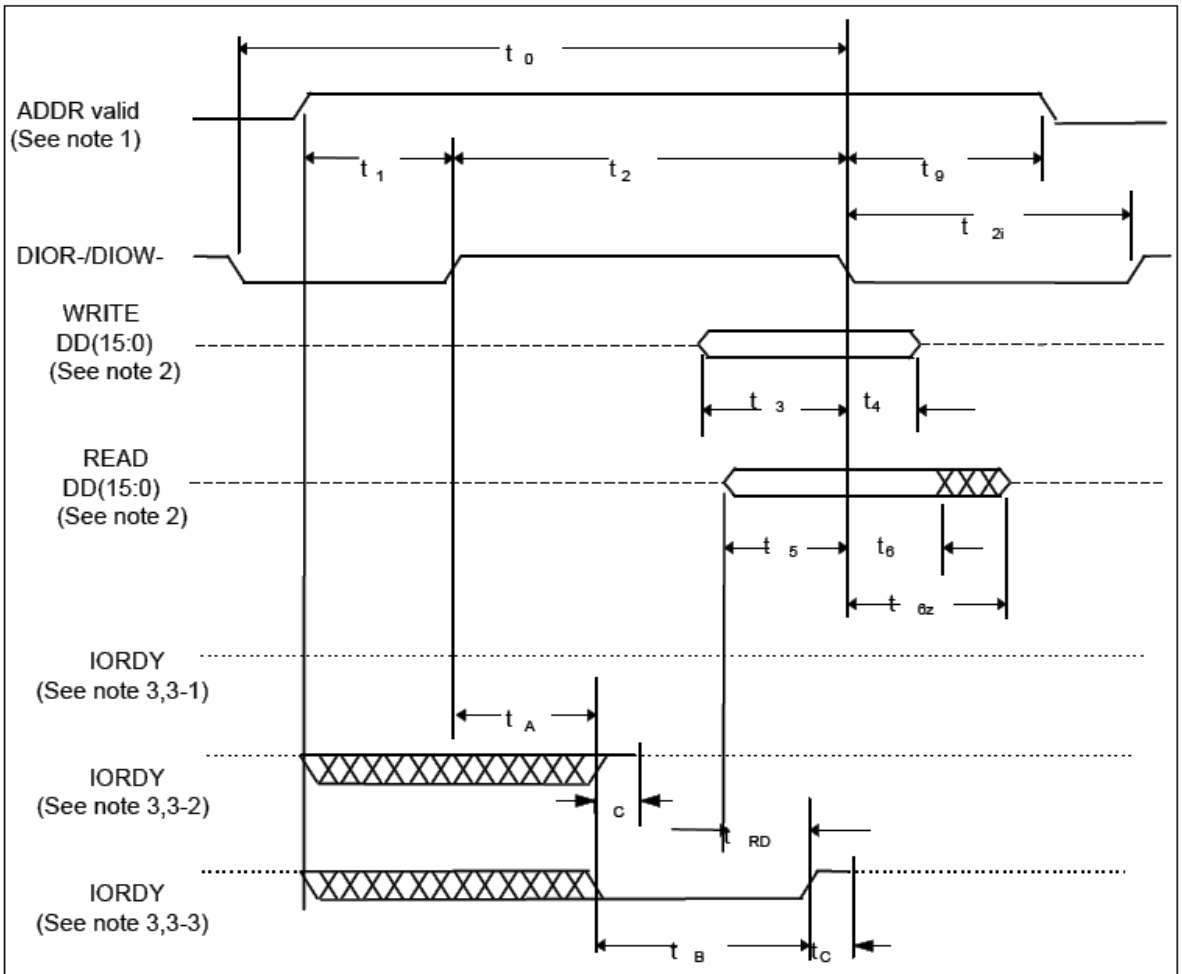
■ PIO data transfers

Figure 21 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 30 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.



NOTES –
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(15:0).
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for t_{RD} before asserting IORDY.

Figure 21 – PIO data transfer to/from device

Table 30 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time	(min)	600	383	240	180	120	1
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR- data hold	(min)	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	(max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	(max)	5	5	5	5	5	

NOTES –

1 t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements is greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.

True IDE Multiword DMA Mode Read/Write Timing Specification

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t_0	Cycle time (min) [1]	480	150	120	100	80
t_D	-IORD / -IOWR asserted width(min) [1]	215	80	70	65	55
t_E	-IORD data access (max)	150	60	50	50	45
t_F	-IORD data hold (min)	5	5	5	5	5
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10
t_H	-IOWR data hold (min)	20	15	10	5	5
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5
t_{KR}	-IORD negated width (min) [1]	50	50	25	25	20
t_{KW}	-IOWR negated width (min) [1]	215	50	25	25	20
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5
t_N	CS(1:0) hold	15	10	10	10	10
t_Z	-DMACK	20	25	25	25	25

Notes:

(1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

True IDE Multiword DMA Mode Read/Write Timing Diagram

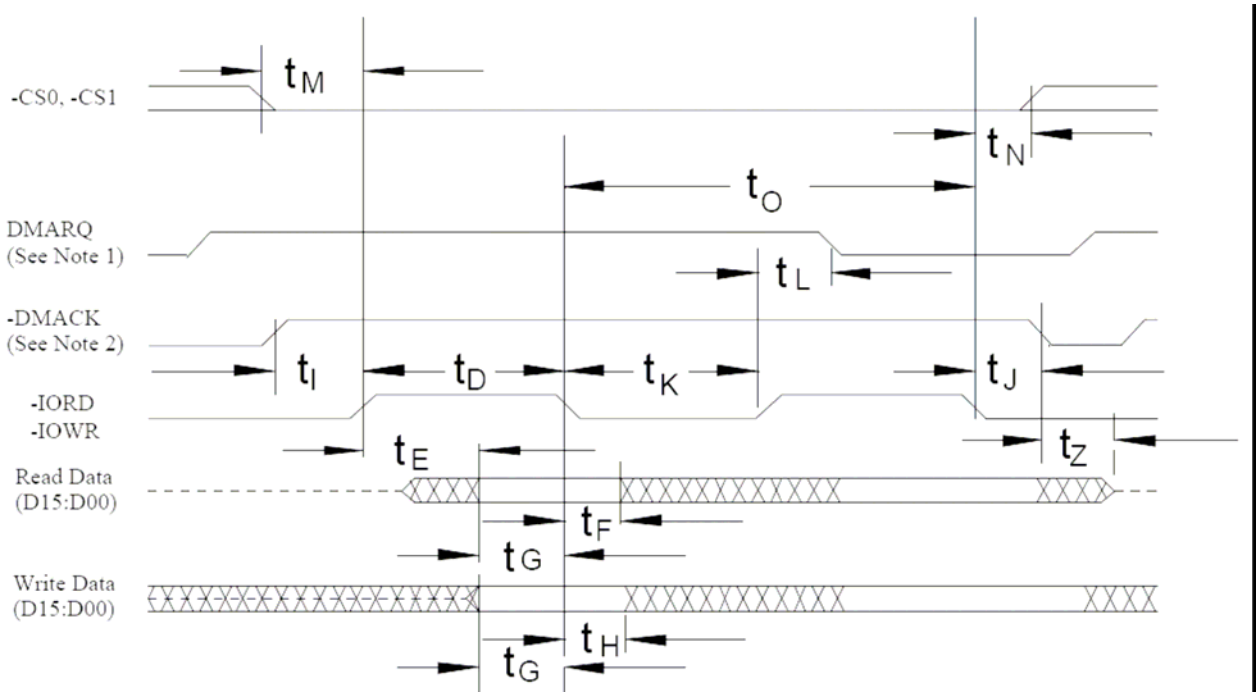


Figure 2: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:
(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
(2) This signal may be negated by the host to suspend the DMA transfer in progress.

Ultra DMA Mode Read/Write Timing Specification

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol.

UDMA Signal	Type	TRUE IDE MODE UDMA
DMARQ	Output	DMARQ
DMACK	Input	-DMACK
STOP	Input	STOP[1]
HDMARDY(R) HSTROBE(W)	Input	-HDMARDY[1,2] HSTROBE(W)[1,3,4]
DDMARDY(W) DSTROBE(R)	Output	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]
DATA	Bidir	D[15:00]
ADDRESS	Input	A[02:00][5]
CSEL	input	-CSEL
INTRQ	Output	INTRQ
Card Select	Input	-CS0 -CS1

Notes: 1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5) Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA data burst. These lines assume their UDMA definitions when:

1. an Ultra DMA mode is selected, and

2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and

3. the device asserts (-)DMARQ, and

4. the host asserts (-)DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA data burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the

same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA data burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA data burst. At the end of an Ultra DMA data burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE – If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measure location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes: All Timings in ns

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector.

(3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

(4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

(5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

(6) See Page 14 the AC Timing requirements in Ultra DMA AC Signal Requirements.

Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2,
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4,
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters t_{UI}, t_{MLI} (in Page 19: Ultra DMA Data-In Burst Device Termination Timing and Page 20: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks,i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.t_{UI} is an unlimited interlock that has no maximum time value. t_{ML}I is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

(2) 80-conductor cabling (see see ATA specification :Annex A)) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

(3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

(4) For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0	

t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)

Notes:
(1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.
(2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
(3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Ultra DMA AC Signal Requirements

Name	**Comment**	**Min[V/ns]**	**Max [V/ns]**	Note
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:
(1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

Initiating an Ultra DMA Data-In Burst

(a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

(b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(c) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated.

(d) The device shall assert DMARQ to initiate an Ultra DMA data burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

(e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

(f) The host shall negate -HDMARDY.

(g) In True IDE mode, the host shall not assert -CS0, -CS1 and A[02:00].

(h) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA data burst.

(i) The host shall release D[15:00] within t_{AZ} after asserting -DMACK.

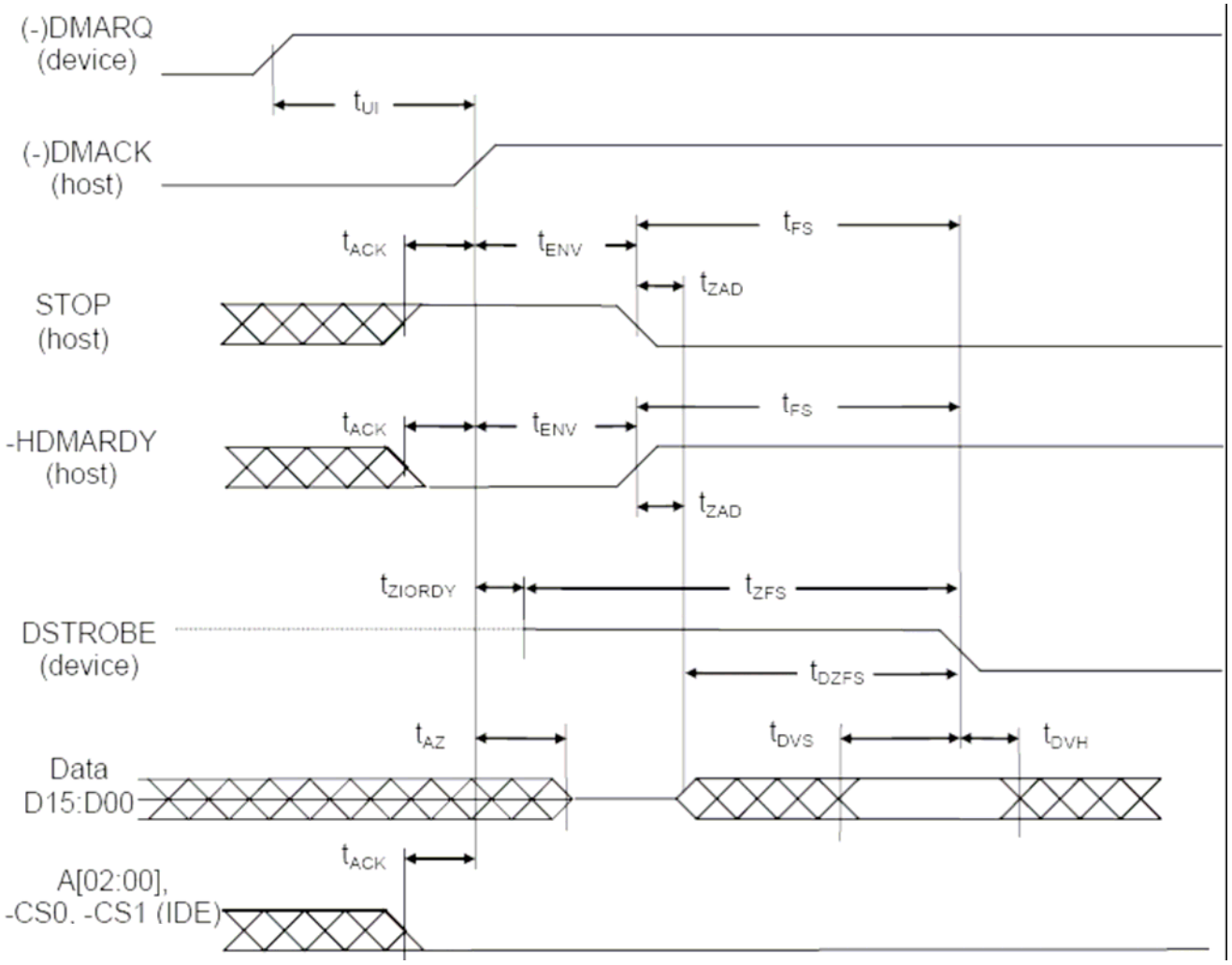
(j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted -DMACK. While operating in True IDE mode, once the device has driven DSTROBE, the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA data burst.

(k) The host shall negate STOP and assert -HDMARDY within t_{ENV} after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

(l) The device shall drive D[15:00] no sooner than t_{ZAD} after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.

(m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).

(n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto D[15:00].



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in below: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

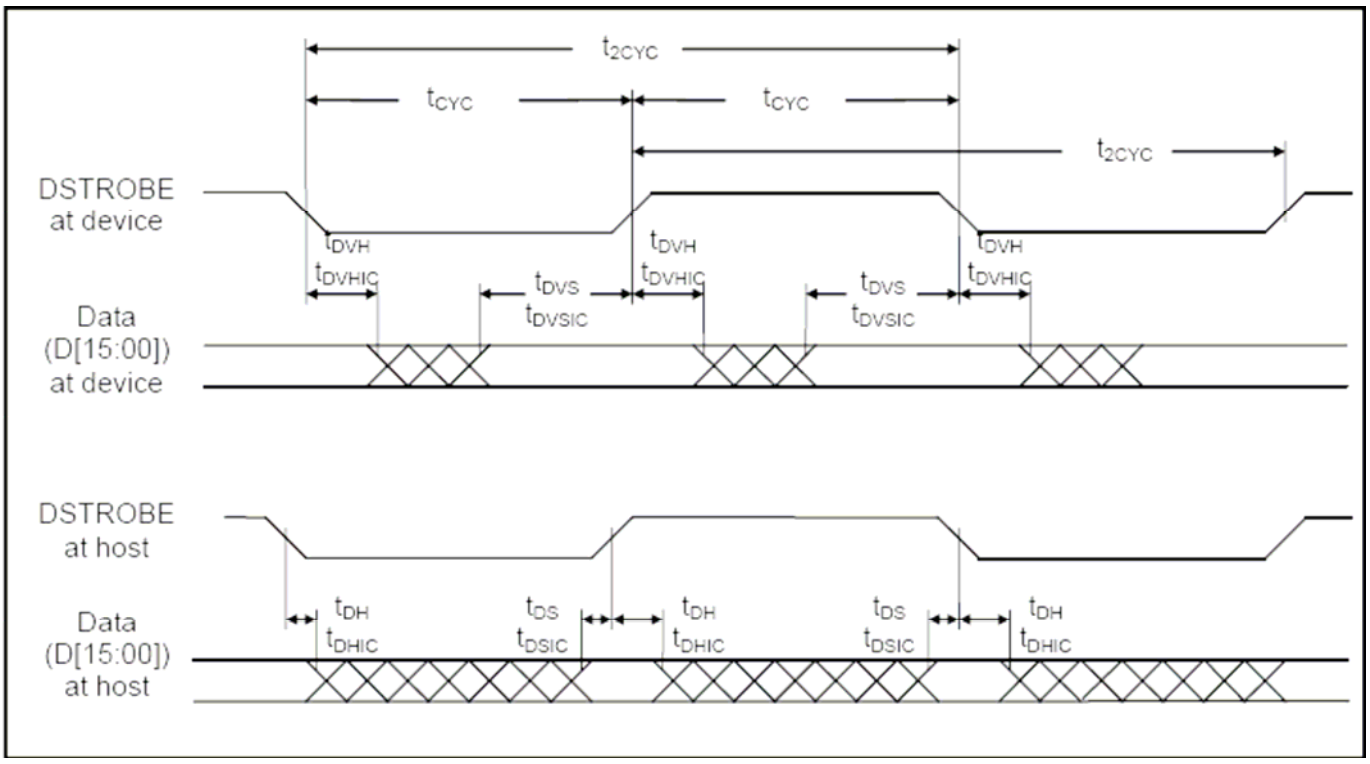
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].

b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than $2t_{cyc}$ for the selected Ultra DMA mode.

c) The device shall not change the state of D[15:00] until at least t_{DVH} after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first.



Notes: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in below: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

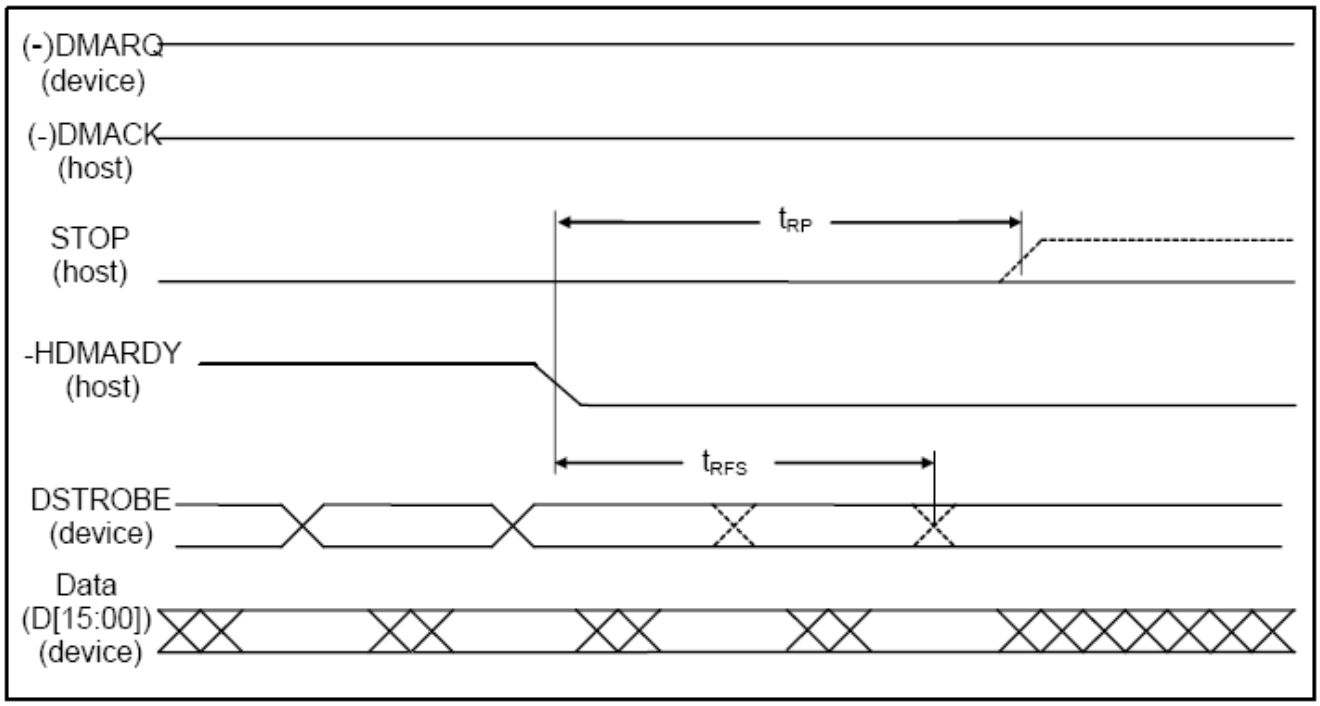
(a) The host shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

(b) The host shall pause an Ultra DMA data burst by negating -HDMARDY.

(c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY.

(d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

(e) The host shall resume an Ultra DMA data burst by asserting -HDMARDY.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than t_{RP} after -HDMARDY is negated.

(2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

(3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode.

Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

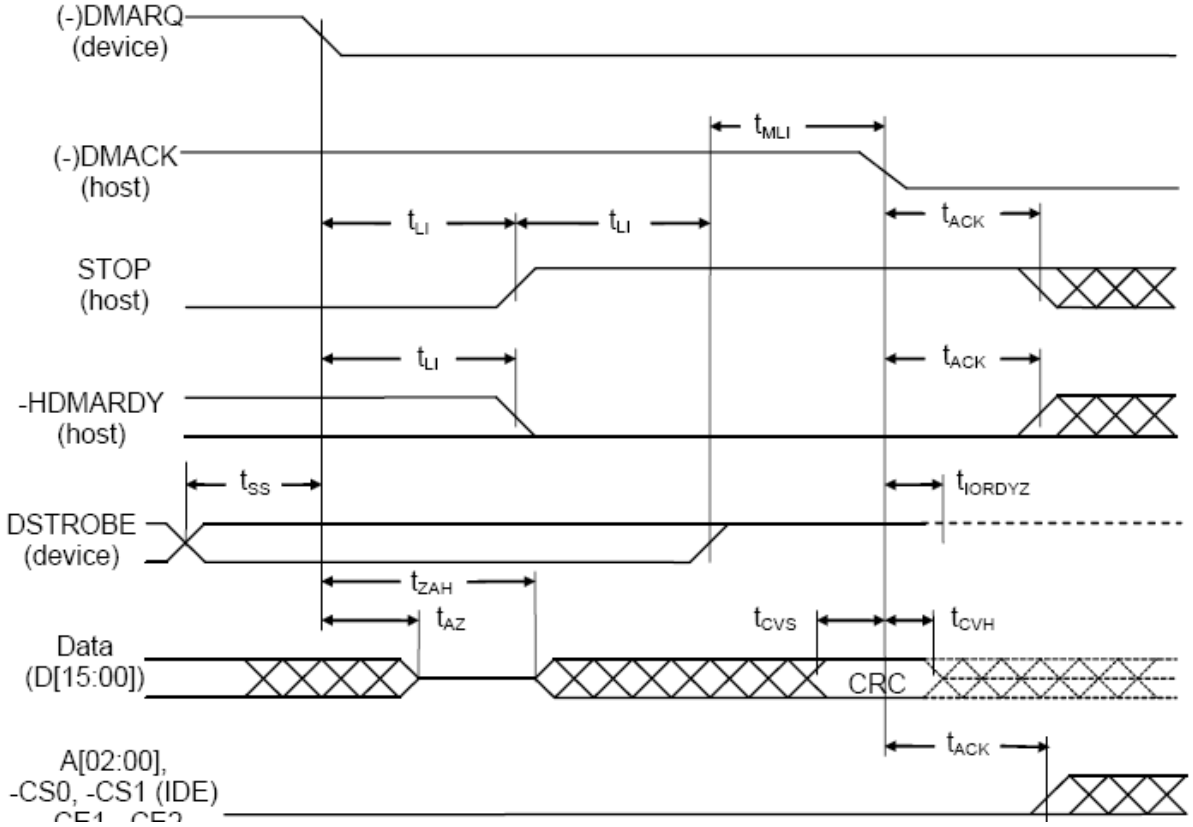
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

(b) The device shall pause an Ultra DMA data burst by not generating DSTROBE edges.

(c) NOTE – The host shall not immediately assert STOP to initiate Ultra DMA data burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate Ultra DMA data burst termination, the host shall negate -HDMARDY and wait t_{RP} before asserting STOP.

(d) The device shall resume an Ultra DMA data burst by generating a DSTROBE edge.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The host shall not initiate Ultra DMA data burst termination until at least one data word of an Ultra DMA data burst has been transferred.

(b) The host shall initiate Ultra DMA data burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA data burst is terminated.

(c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY

(d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

(e) The host shall assert STOP no sooner than t_{RP} after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

(f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

(g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

(h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.

(i) The host shall drive D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation (see ATA specification Ultra DMA CRC Calculation).

(j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00] (see ATA specification Ultra DMA CRC Calculation).

(k) The host shall negate -DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].

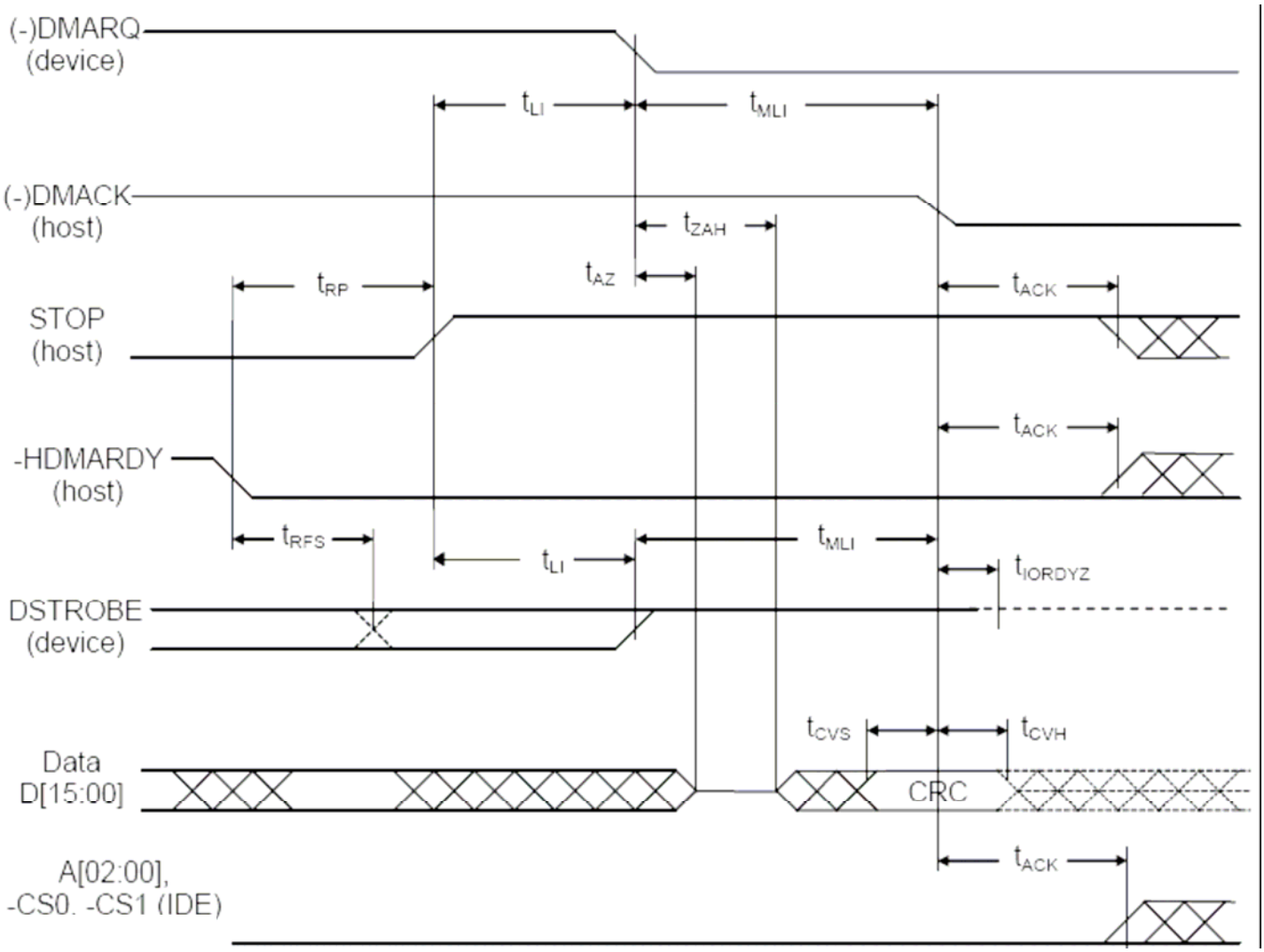
(l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

(m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data burst for any one command, at the end of the command, the device shall report the first error that occurred (see ATA specification Ultra DMA CRC Calculation)

(n) While operating in True IDE mode, the device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.

(o) The host shall neither negate STOP nor assert -HDMARDY until at least t_{ACK} after the host has negated -DMACK.

(p) In True IDE mode, the host shall not assert -IORD, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13:Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated.

(b) The device shall assert DMARQ to initiate an Ultra DMA data burst.

(c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

(d) The host shall assert HSTROBE.

(e) In True IDE mode, the host shall not assert -CS0, -CS1, nor A[02:00].

(f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK.The host shall keep -DMACK asserted until the end of an Ultra DMA data burst.

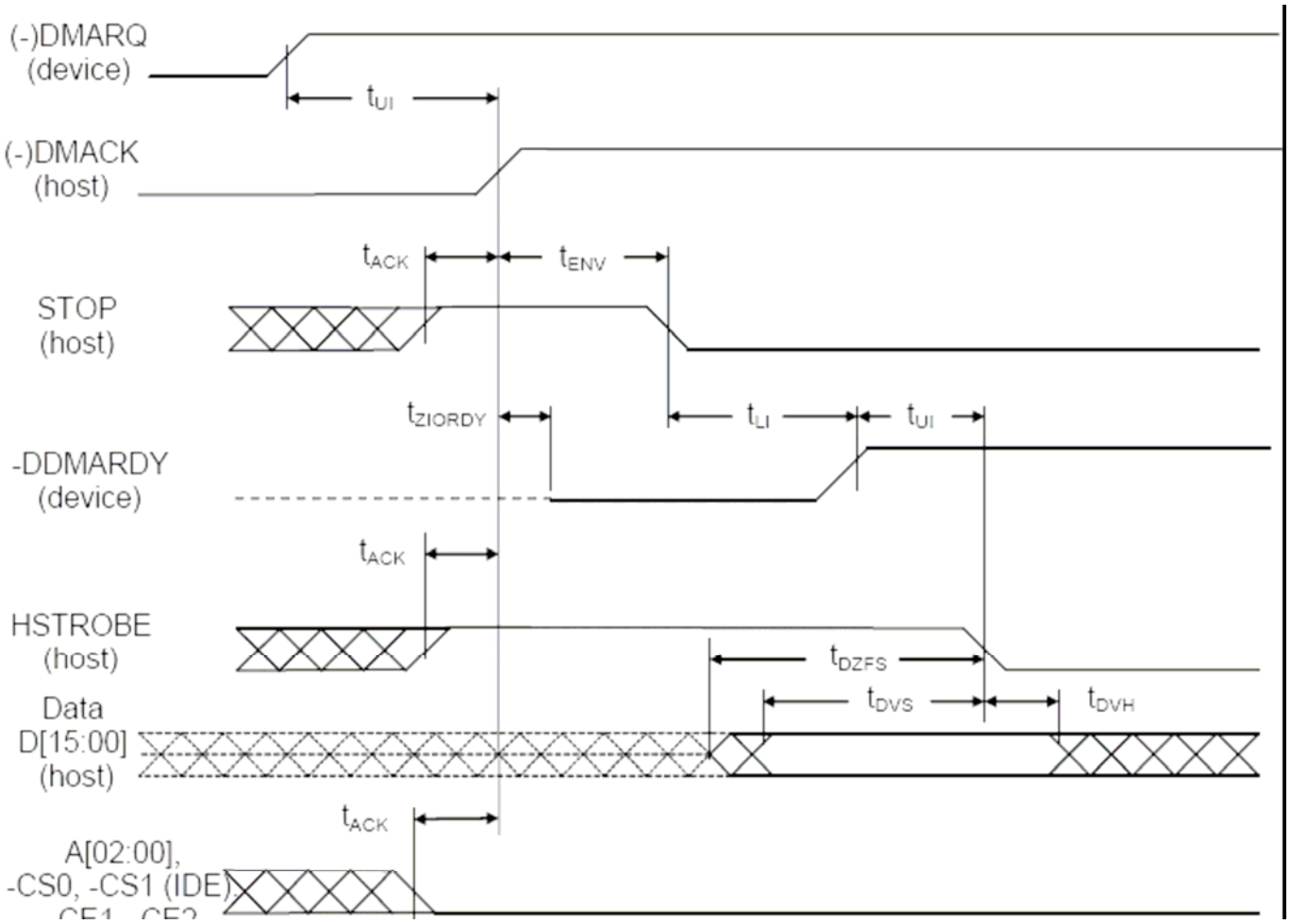
(g) The device may negate -DDMARDY t_{ZIORDY} after the host has asserted -DMACK. While operating in True IDE mode, once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA data burst.

(h) The host shall negate STOP within t_{ENV} after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

(i) The device shall assert -DDMARDY within t_{LI} after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

(j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA data burst initiation.

(k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto D[15:00].



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in below: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

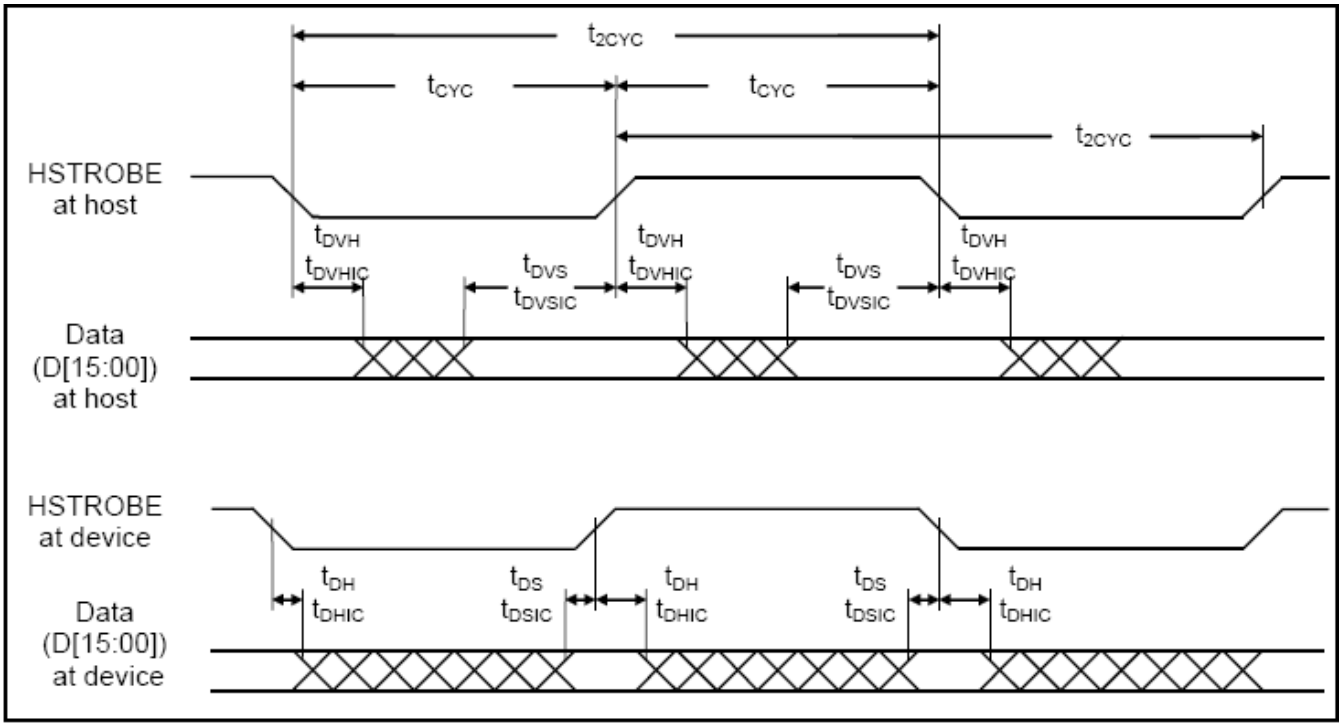
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The host shall drive a data word onto D[15:00].

(b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than $2t_{cyc}$ for the selected Ultra DMA mode.

(c) The host shall not change the state of D[15:00] until at least t_{DVH} after generating an HSTROBE edge to latch the data.

(d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first.



Note: Data (D[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in below: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

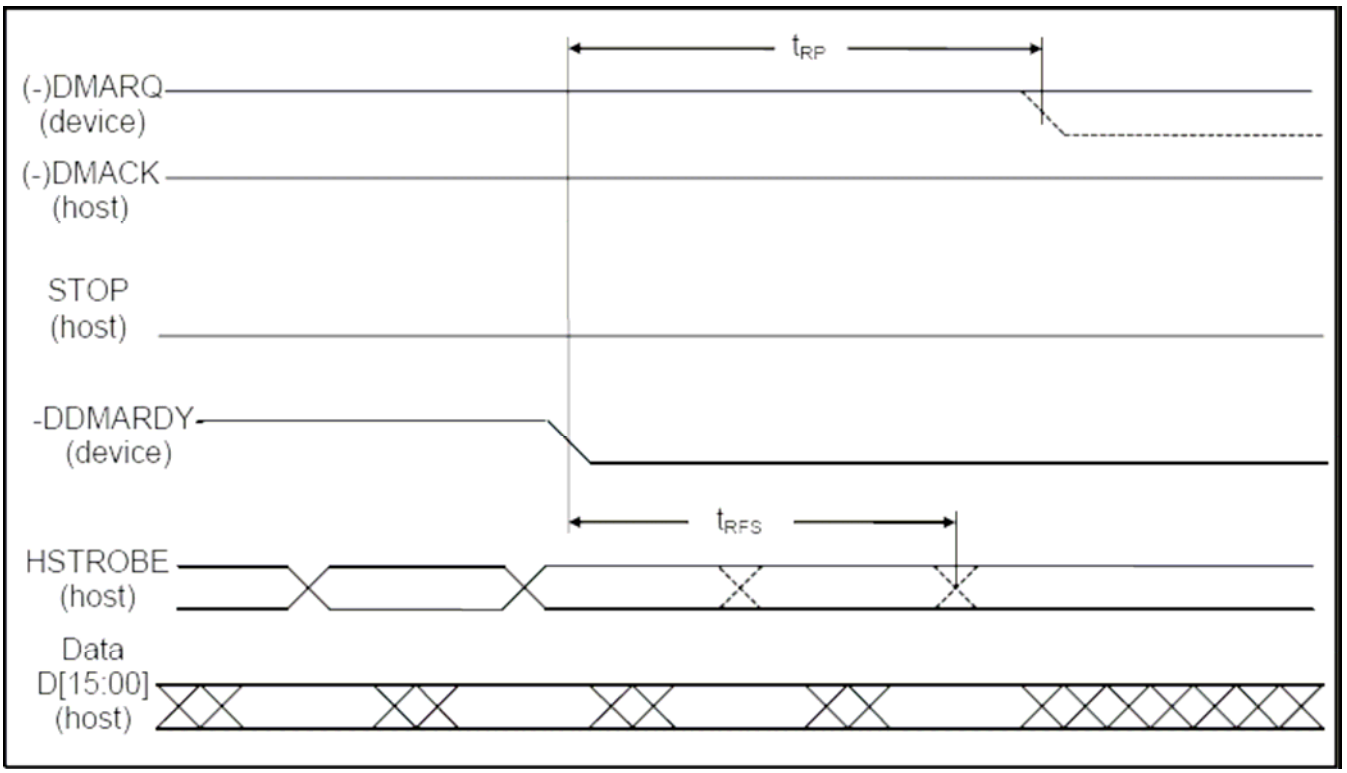
(a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

(b) The device shall pause an Ultra DMA data burst by negating -DDMARDY.

(c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating -DDMARDY.

(d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

(e) The device shall resume an Ultra DMA data burst by asserting -DDMARDY.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than t_{RP} after -DDMARDY is negated.

(2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in below: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The device shall not initiate Ultra DMA data burst termination until at least one data word of an Ultra DMA data burst has been transferred.

(b) The device shall initiate Ultra DMA data burst termination by negating -DDMARDY.

(c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating -DDMARDY.

(d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

(e) The device shall negate DMARQ no sooner than t_{RP} after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

(f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

(g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

(h) The host shall place the result of its CRC calculation on D[15:00] (see ATA specification Ultra DMA CRC Calculation).

(i) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

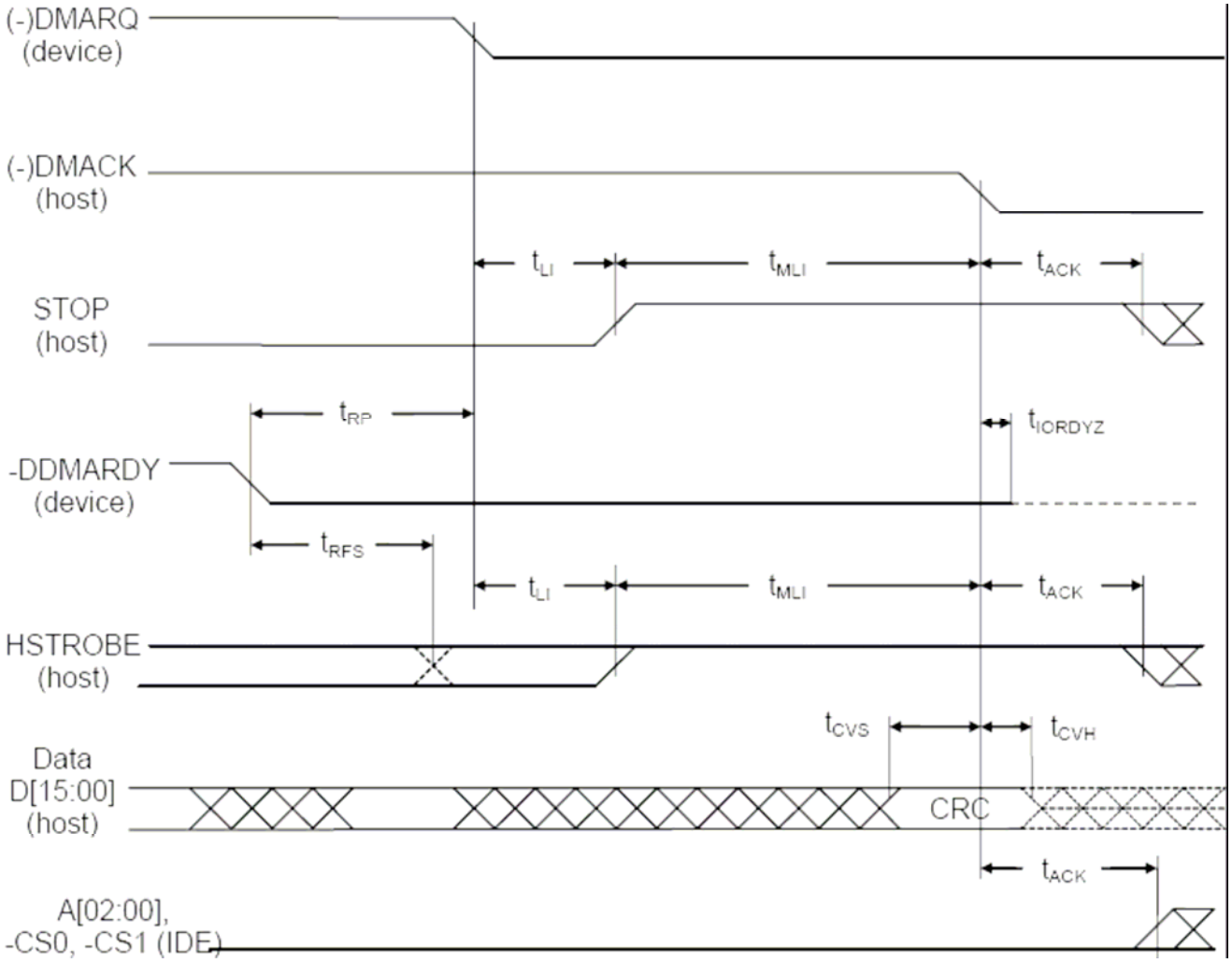
(j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

(k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred (see ATA specification Ultra DMA CRC Calculation).

(l) While operating in True IDE mode, the device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.

(m) The host shall not negate STOP nor assert –HDMARDY until at least t_{ACK} after negating -DMACK.

(n) In True IDE mode, the host shall not assert -IOWR, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A00-A02, -CS0 & -CS1 are True IDE mode signal definitions.

Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in below: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Page 12: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Page 13: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

(a) The host shall initiate termination of an Ultra DMA data burst by not generating HSTROBE edges.

(b) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge.The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

(c) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

(d) The device shall negate -DDMARDY within t_{LI} after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA data burst termination is complete.

(e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

(f) The host shall place the result of its CRC calculation on D[15:00] (see ATA specification Ultra DMA CRC Calculation).

(g) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

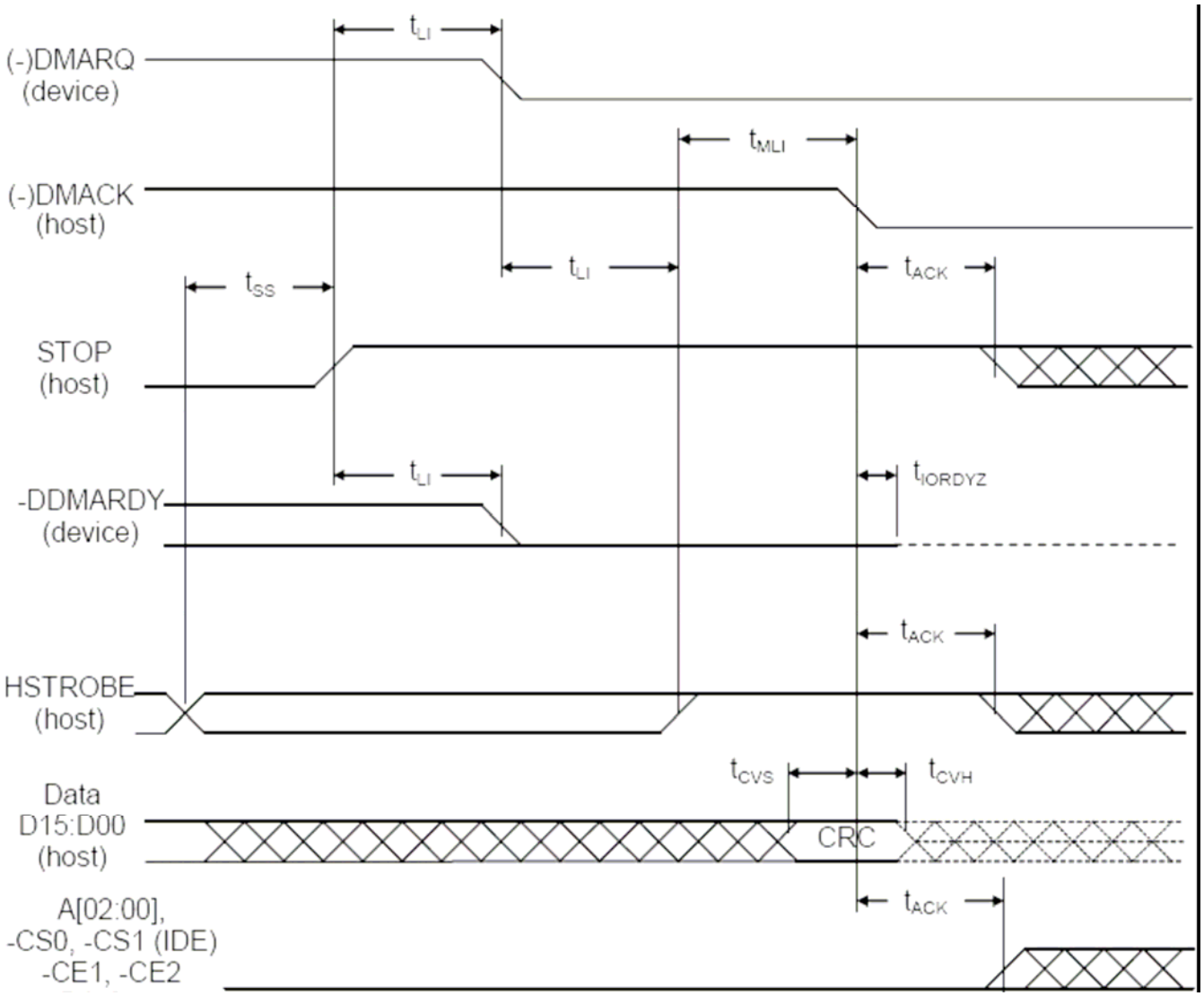
(h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

(i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, at the end of the command, the device shall report the first error that occurred (see ATA specification Ultra DMA CRC Calculation).

(j) While operating in True IDE mode, the device shall release -DDMARDY within t_{IORDYZ} after the host has negated -DMACK.

(k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating -DMACK.

(l) In True IDE mode, the host shall not assert -IOWR, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK..



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions.

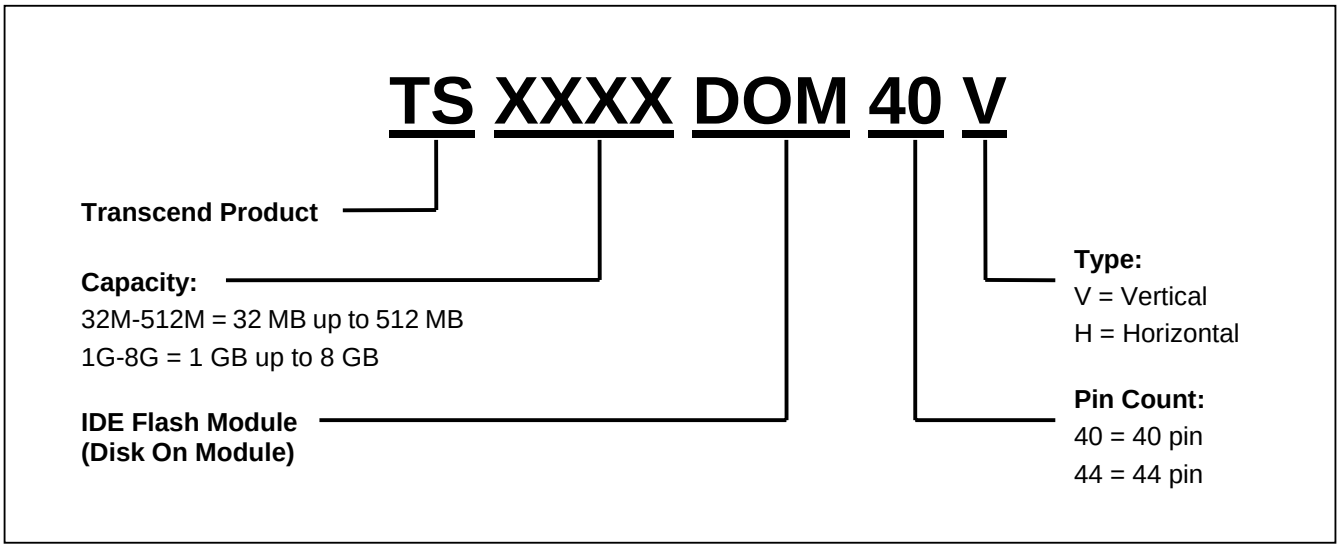
Transcend 40-Pin IDE Flash Module
128MB ~ 8GB

Capacity Specifications:

Transcend P/N	Capacity	Cylinder (C)	Head (H)	Sector (S)
TS128MDOM40V	128MB	978	8	32
TS256MDOM40V	256MB	978	16	32
TS512MDOM40V	512MB	993	16	63
TS1GDOM40V	1GB	1985	16	63
TS2GDOM40V	2GB	3954	16	63
TS4GDOM40V	4GB	7889	16	63
TS8GDOM40V	8GB	15778	16	63

Transcend 40-Pin IDE Flash Module
128MB ~ 8GB

Ordering Information



The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

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