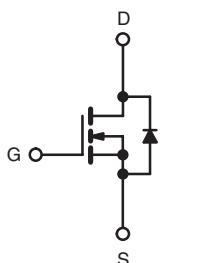
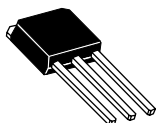




Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0$ V	0.27
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.1	
Configuration	Single	

DPAK
(TO-252)IPAK
(TO-251)

N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR120/SiHLR120)
- Straight Lead (IRLU120/SiHLU120)
- Available in Tape and Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- Lead (Pb)-free Available

RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU/SiHLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRLR120PbF	IRLR120TRLPbF ^a	IRLR120TRPbF ^a	IRLR120TRRPbF ^a	IRLU120PbF
	SiHLR120-E3	SiHLR120TL-E3 ^a	SiHLR120T-E3 ^a	SiHLR120TR-E3 ^a	SiHLU120-E3
SnPb	IRLR120	IRLR120TRL ^a	IRLR120TR ^a	-	-
	SiHLR120	SiHLR120TL ^a	SiHLR120T ^a	-	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	31	W/°C
Linear Derating Factor		0.33	
Linear Derating Factor (PCB Mount) ^e		0.020	mJ
Single Pulse Avalanche Energy ^b	E_{AS}	210	
Repetitive Avalanche Current ^a	I_{AR}	7.7	A
Repetitive Avalanche Energy ^a	E_{AR}	4.2	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25$ °C	
Peak Diode Recovery dV/dt ^c	dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	260 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 5.3$ mH, $R_G = 25$ Ω , $I_{AS} = 7.7$ A (see fig. 12).

c. $I_{SD} \leq 9.2$ A, $dI/dt \leq 110$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

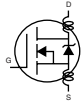
THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.13	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 5.0 V	I _D = 4.6 A ^b	-	-	0.27	Ω
		V _{GS} = 4.0 V	I _D = 3.9 A ^b	-	-	0.38	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 4.6 A ^b		4.4	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	490	-	pF
Output Capacitance	C _{oss}			-	150	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = 5.0 V	I _D = 9.2 A, V _{DS} = 80 V, see fig. 6 and 13 ^b	-	-	12	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	7.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, I _D = 9.2 A, R _G = 9.0 Ω, R _D = 5.2 Ω, see fig. 10 ^b		-	9.8	-	ns
Rise Time	t _r			-	64	-	
Turn-Off Delay Time	t _{d(off)}			-	21	-	
Fall Time	t _f			-	27	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact ^c 		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7.7	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	31	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 7.7 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 9.2 A, dI/dt = 100 A/μs ^b		-	110	140	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.80	1.0	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

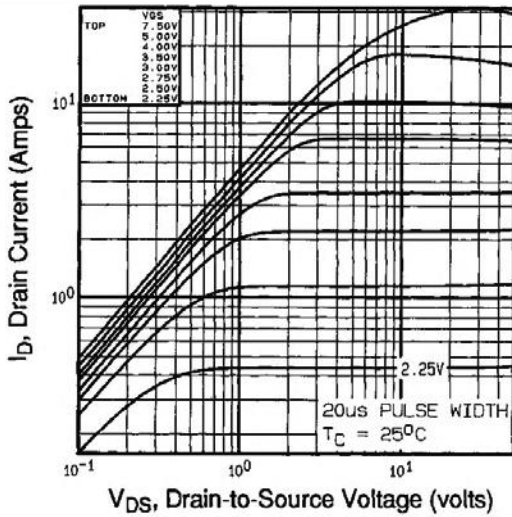


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

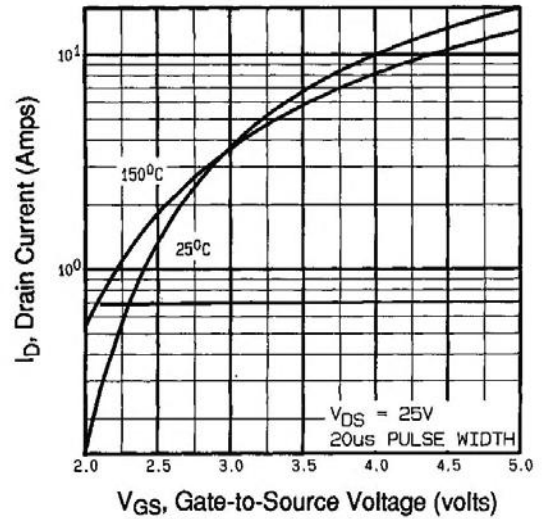


Fig. 3 - Typical Transfer Characteristics

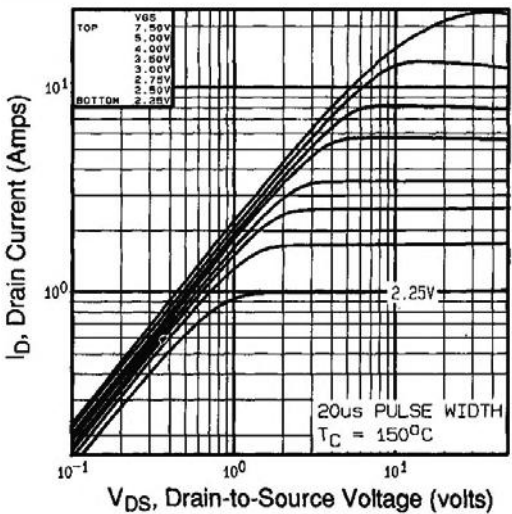


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

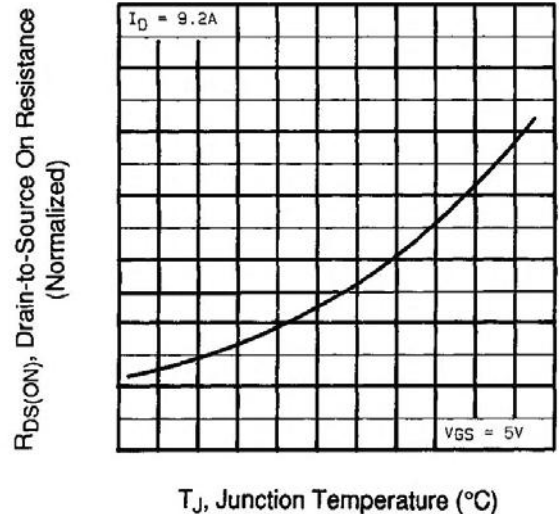


Fig. 4 - Normalized On-Resistance vs. Temperature

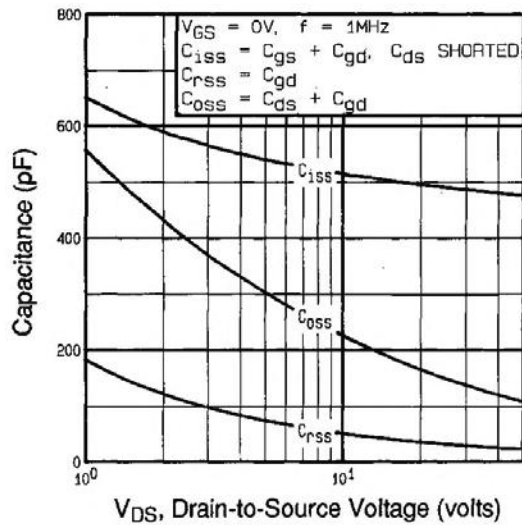


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

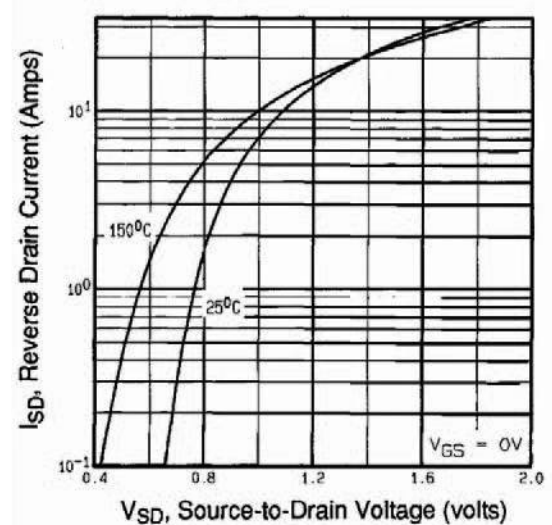


Fig. 7 - Typical Source-Drain Diode Forward Voltage

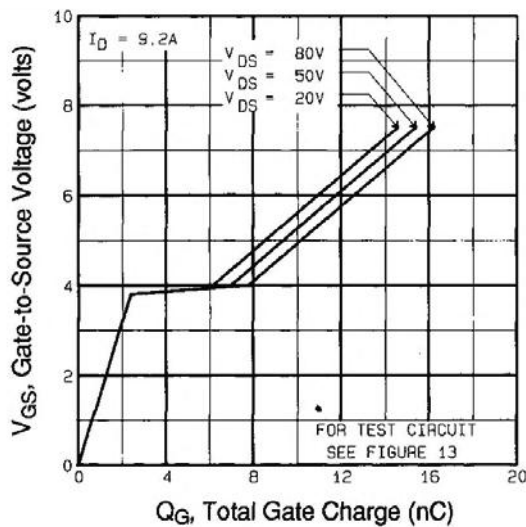


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

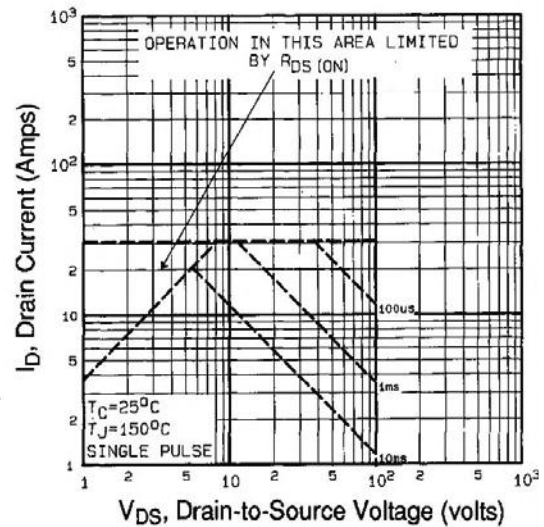


Fig. 8 - Maximum Safe Operating Area

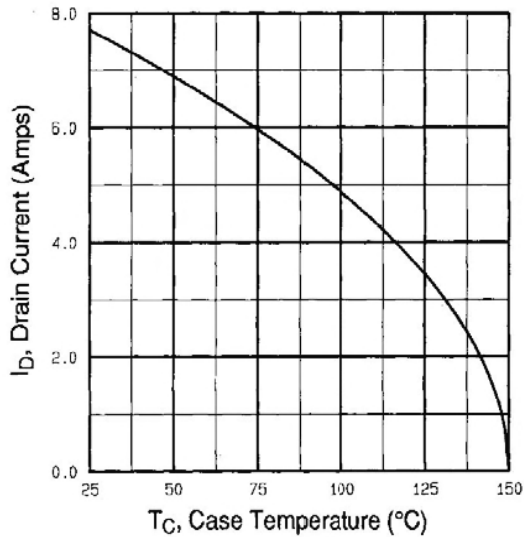


Fig. 9 - Maximum Drain Current vs. Case Temperature

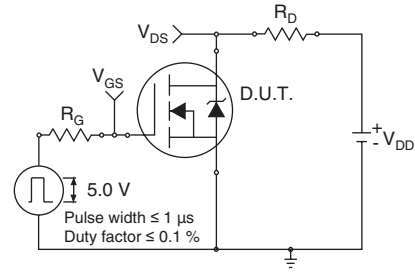


Fig. 10a - Switching Time Test Circuit

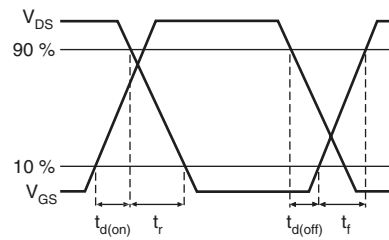


Fig. 10b - Switching Time Waveforms

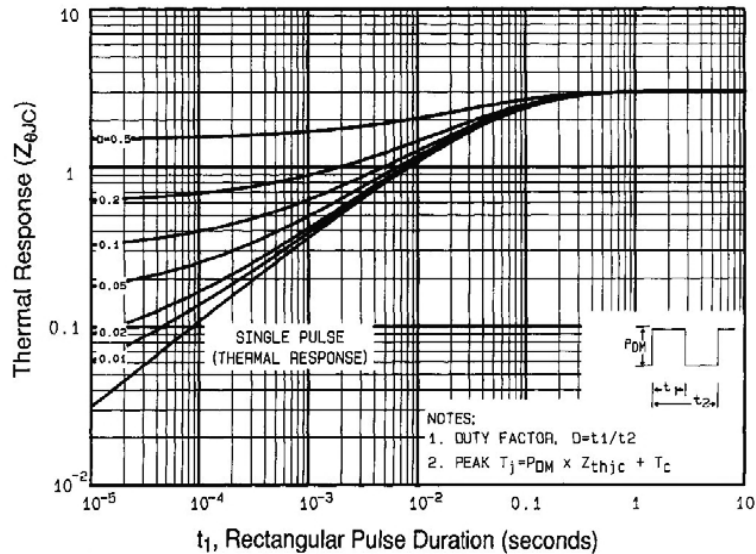


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

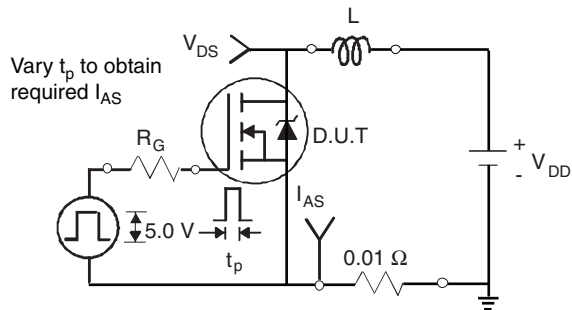


Fig. 12a - Unclamped Inductive Test Circuit

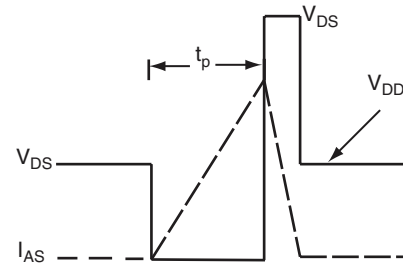


Fig. 12b - Unclamped Inductive Waveforms

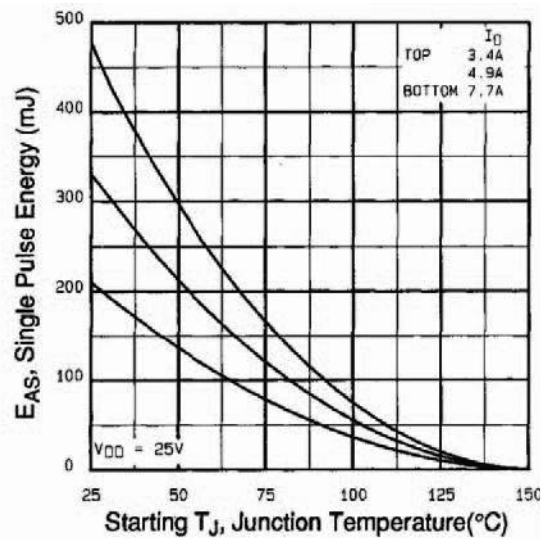


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

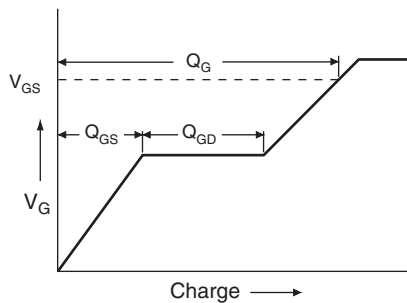


Fig. 13a - Basic Gate Charge Waveform

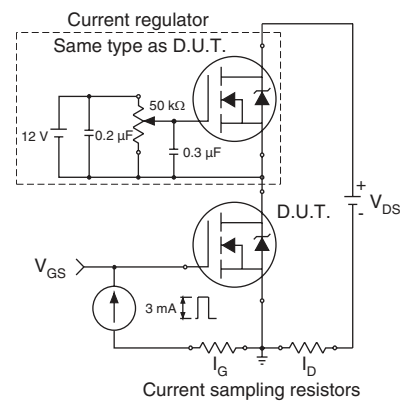
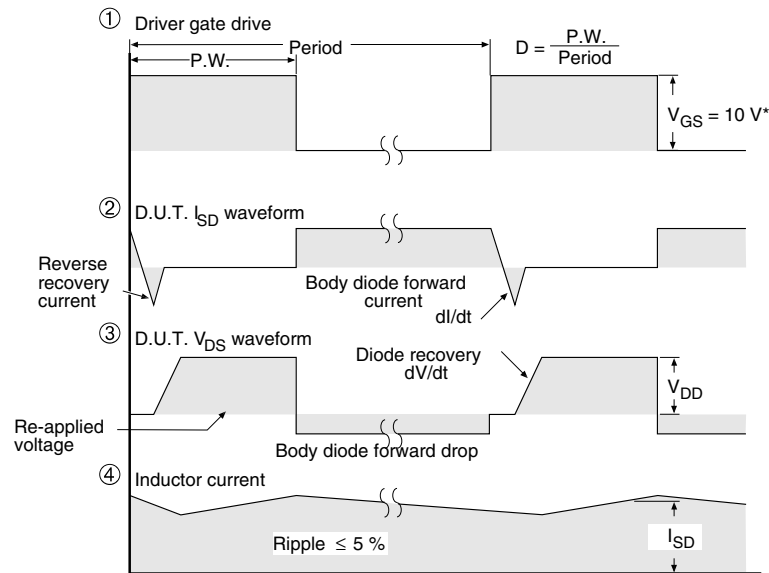
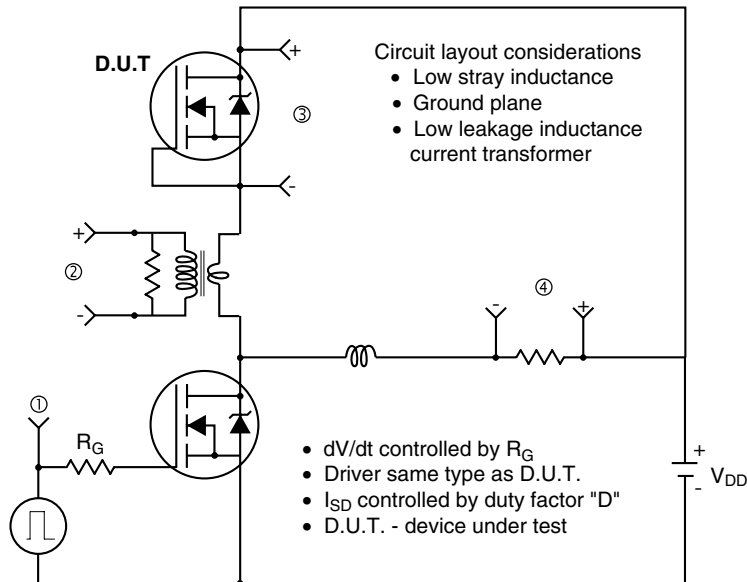


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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