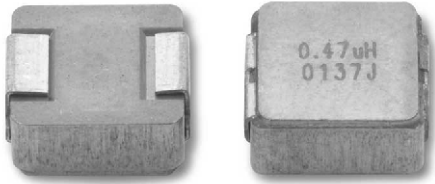


Low Profile, High Current Inductor



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
 Several foreign patents, and other patents pending.

STANDARD ELECTRICAL SPECIFICATIONS

Lo INDUCTANCE µH ± 20 % at 100 kHz, 0.25 V, 0 A	DCR mΩ TYPICAL 25 °C	DCR mΩ MAX 25 °C	HEAT RATING CURRENT DC AMPS ³ TYPICAL	SATURATION CURRENT DC AMPS ⁴ TYPICAL
0.10	1.5	1.7	32.5	60
0.15	1.9	2.5	26	52
0.20	2.4	3.0	24	41
0.22	2.5	2.8	23	40
0.33	3.5	3.9	20	30
0.47	4	4.2	17.5	26
0.68	5	5.5	15.5	25
0.82	6.7	8	13	24
1.0	9	10	11	22
1.5	14	15	9	18
2.2	18	20	8	14
3.3	28	30	6	13.5
4.7	37	40	5.5	10
6.8	54	60	4.5	8
8.2	64	68	4	7.5
10	102	105	3	7.0

NOTES:

- All test data is referenced to 25 °C ambient
- Operating Temperature Range - 55 °C to + 125 °C
- DC current (A) that will cause an approximate ΔGT of 40 °C
- DC current (A) that will cause Lo to drop approximately 20 %
- The part temperature (ambient + temp rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

FEATURES

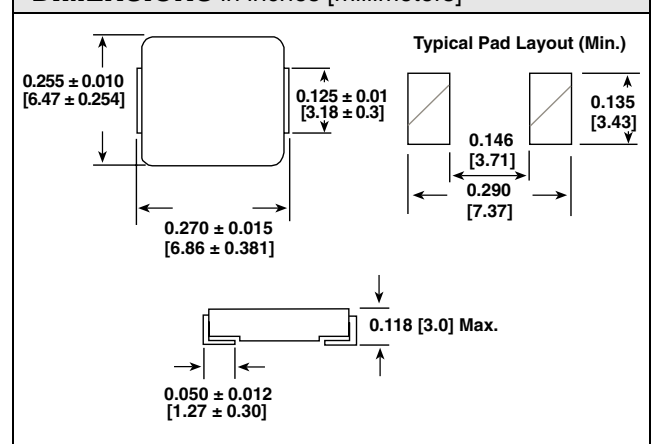
- Lowest height (3.0 mm) in this package footprint
- Shielded construction
- Frequency range up to 5.0 MHz
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- 100 % lead (Pb)-free and RoHS compliant


**RoHS
COMPLIANT**

APPLICATIONS

- PDA/Notebook/Desktop/Server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

DIMENSIONS in inches [millimeters]



DESCRIPTION

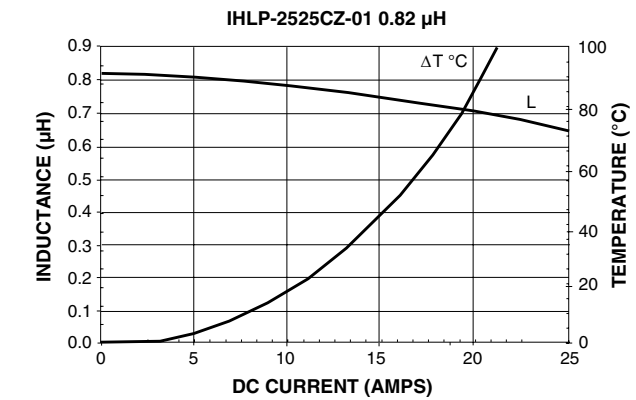
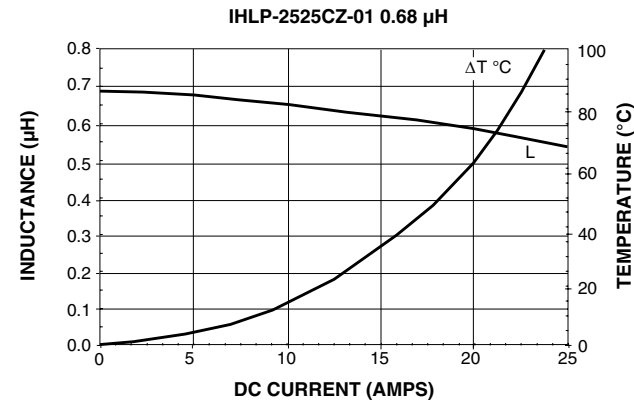
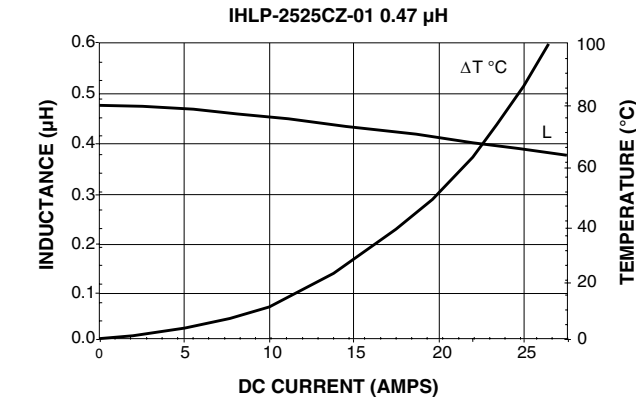
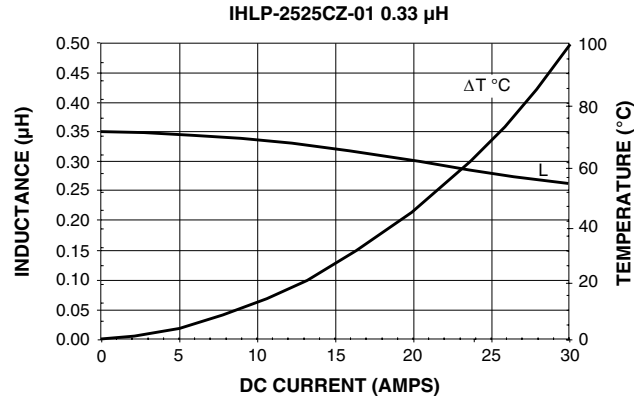
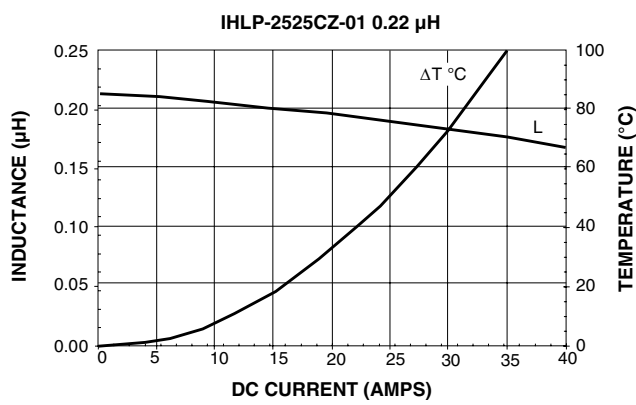
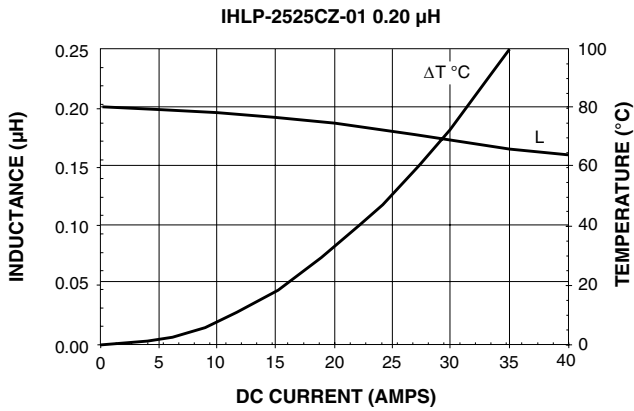
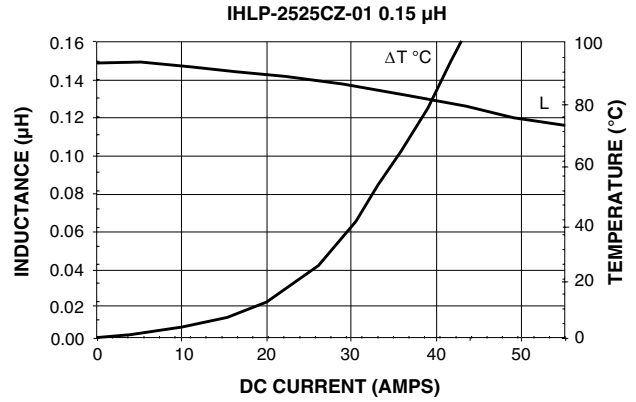
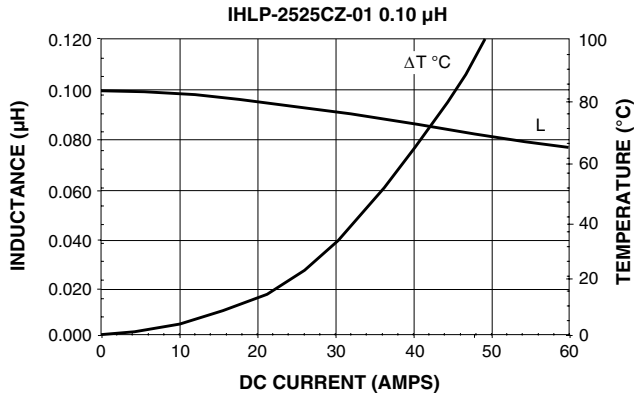
IHLP-2525CZ-01	1.0 µH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER

I	H	L	P	2	5	2	5	C	Z	E	R	1	R	0	M	0	1
MODEL				SIZE				PACKAGE CODE		INDUCTANCE VALUE		INDUCTANCE TOLERANCE		SERIES			

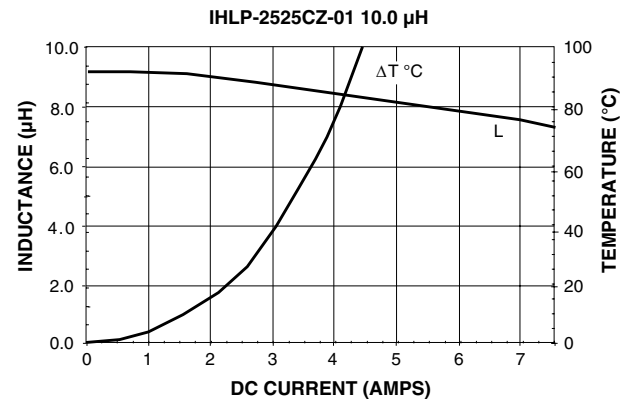
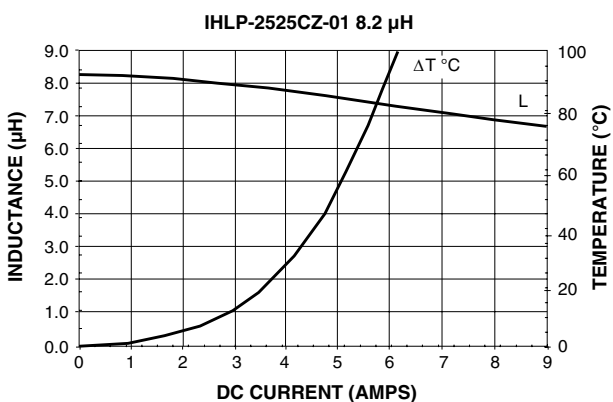
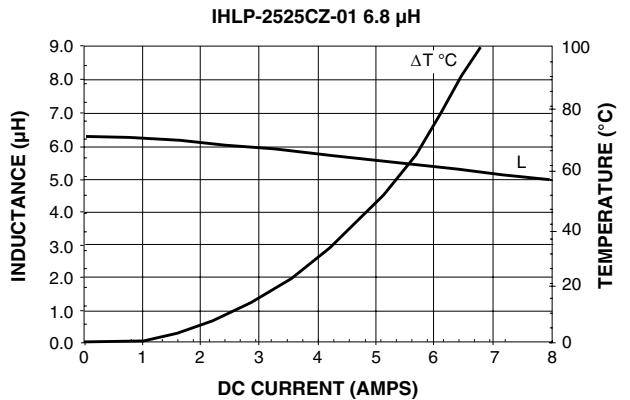
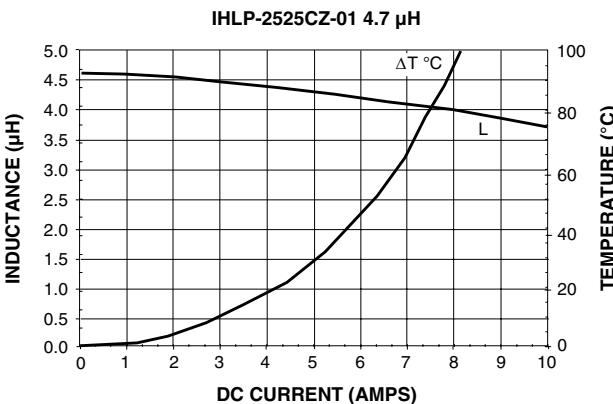
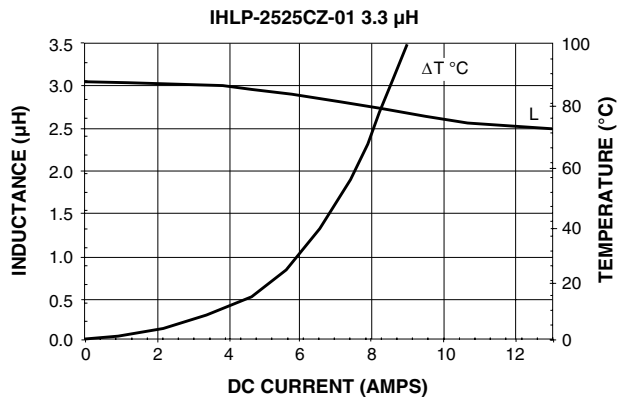
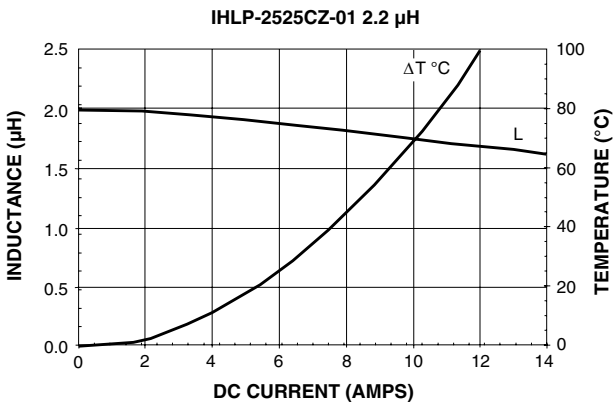
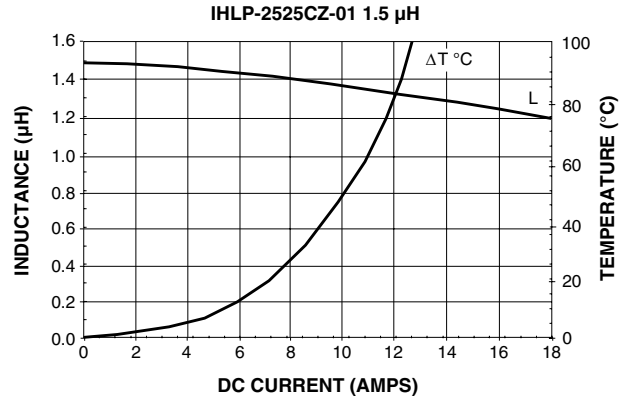
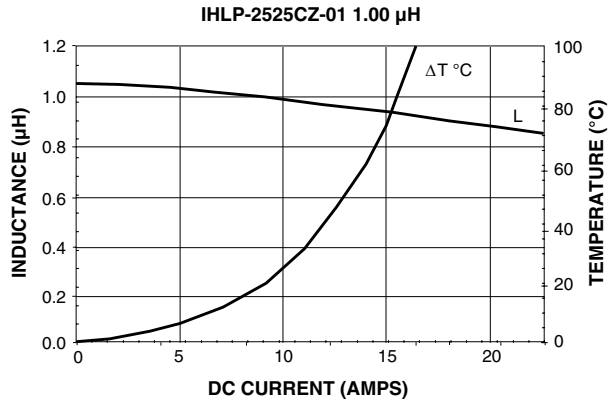


PERFORMANCE GRAPHS





PERFORMANCE GRAPHS





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