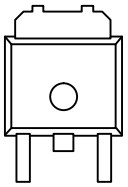
N-Channel 100-V (D-S) 175°C MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
100	0.200 @ V_{GS} = 10 V	6.5	2.7
	0.225 @ V_{GS} = 4.5 V	6.0	

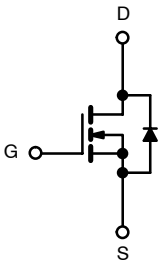
175°C Rated Maximum Junction Temperature TrenchFET® Power MOSFETs

TO-252



Top View

Drain Connected to Tab



N-Channel MOSFET

Order Number: SUD06N10-225L
SUD06N10-225L—E3 (lLead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175°C)[b]	T_C = 25°C	I_D	6.5	A
	T_C = 125°C		3.75	
Pulsed Drain Current		I_{DM}	8.0	
Continuous Source Current (Diode Conduction)		I_S	6.5	
Avalanche Current		I_{AR}	5.0	
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)	L = 0.1 mH	E_{AR}	1.25	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	20[b]	W
	T_A = 25°C		1.5[a]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	40	50	°C/W
	Steady State		80	100	
Junction-to-Case		R_{thJC}	6.0	7.5	

Notes
a. Surface Mounted on 1" x1" FR4 Board.
b. See SOA curve for voltage derating.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

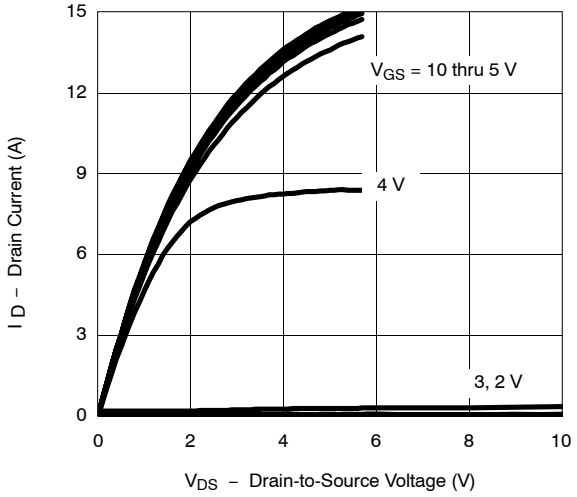
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0		3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125°C			50	
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	8.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A		0.160	0.200	Ω
		V_{GS} = 10 V, I_D = 3 A, T_J = 125°C			0.350	
		V_{GS} = 10 V, I_D = 3 A, T_J = 175°C			0.450	
		V_{GS} = 4.5 V, I_D = 1.0 A		0.180	0.225	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3 A		8.5		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, F = 1 MHz		240		pF
Output Capacitance	C_{oss}			42		
Reverse Transfer Capacitance	C_{rss}			17		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 6.5 A		2.7	4.0	nC
Gate-Source Charge[c]	Q_{gs}			0.6		
Gate-Drain Charge[c]	Q_{gd}			0.7		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 7.5 Ω I_D ≅ 6.5 A, V_{GEN} = 10 V, R_g = 2.5 Ω		7	11	ns
Rise Time[c]	t_r			8	12	
Turn-Off Delay Time[c]	$t_{d(off)}$			8	12	
Fall Time[c]	t_f			9	14	
Source-Drain Diode Ratings and Characteristic (T_C = 25°C)						
Pulsed Current	I_{SM}				8.0	A
Diode Forward Voltage[b]	V_{SD}	I_F = 6.5 A, V_{GS} = 0 V		0.9	1.3	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 6.5 A, di/dt = 100 A/μs		35	60	ns

Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
c. Independent of operating temperature.

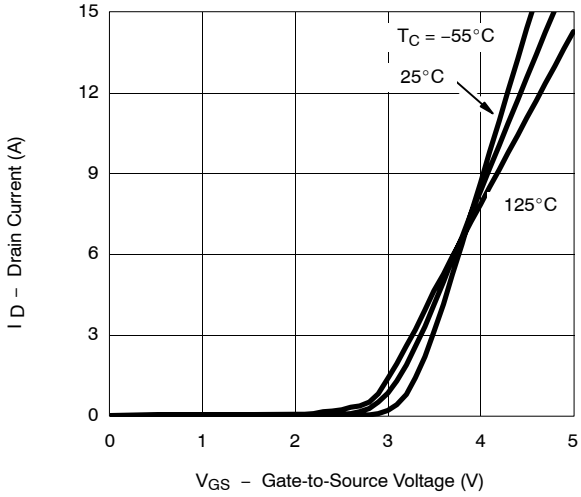
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

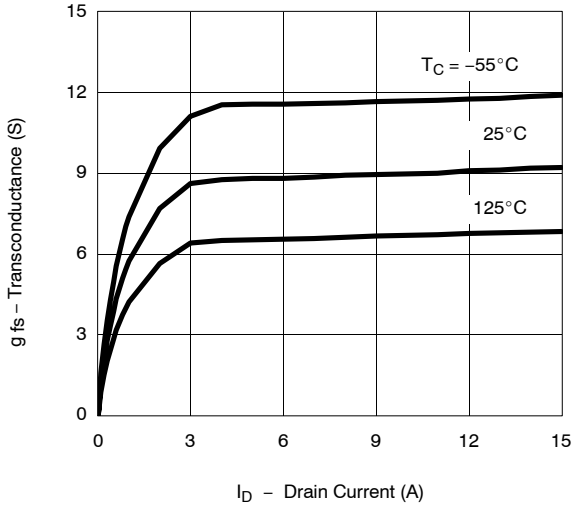
Output Characteristics



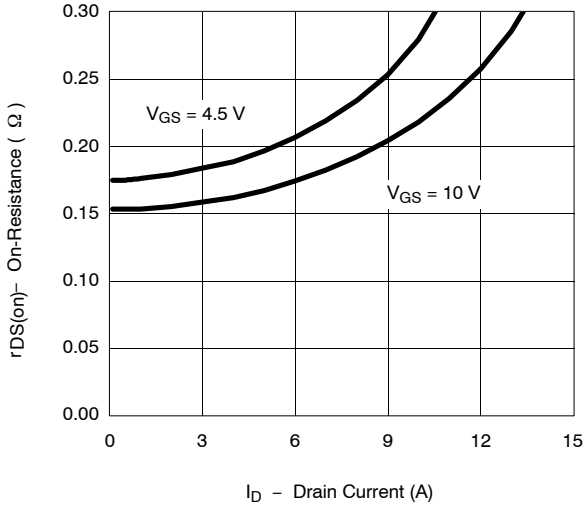
Transfer Characteristics



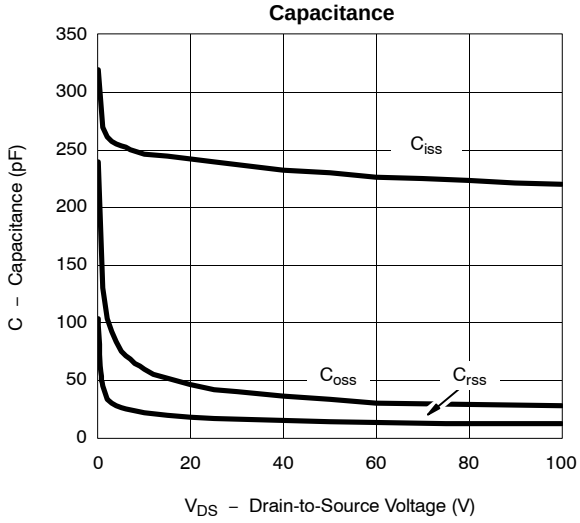
Transconductance



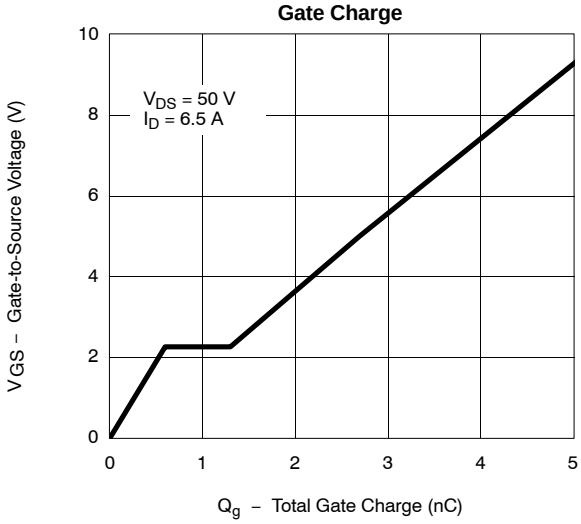
On-Resistance vs. Drain Current



Capacitance

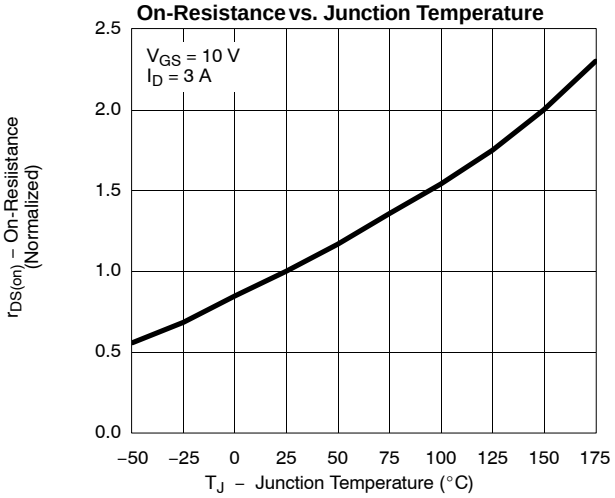


Gate Charge

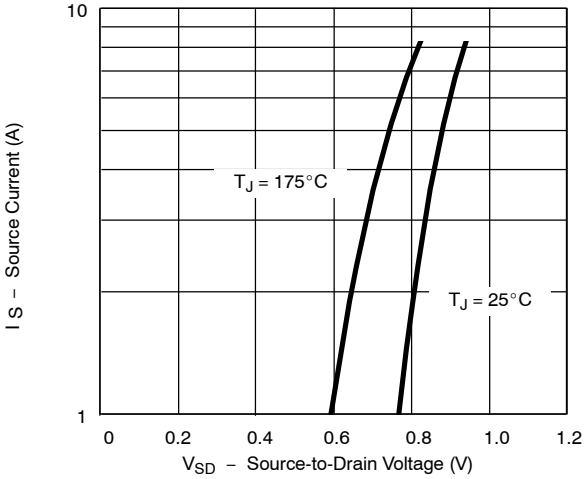


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

On-Resistance vs. Junction Temperature

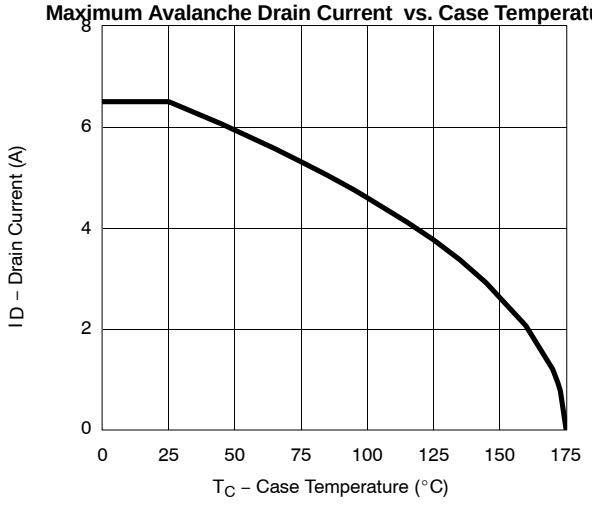


Source-Drain Diode Forward Voltage

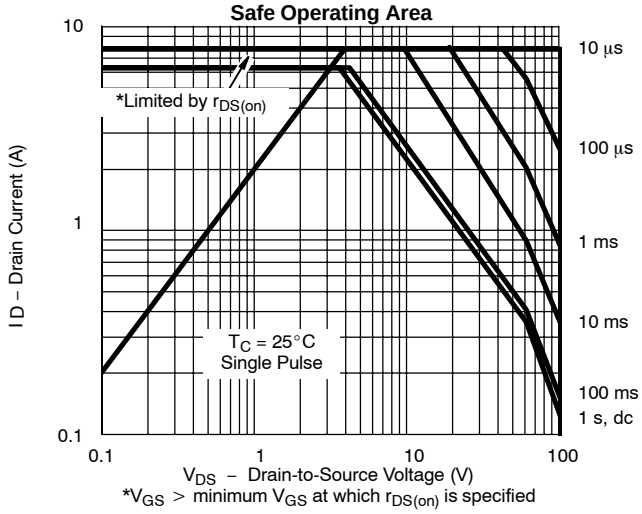


THERMAL RATINGS

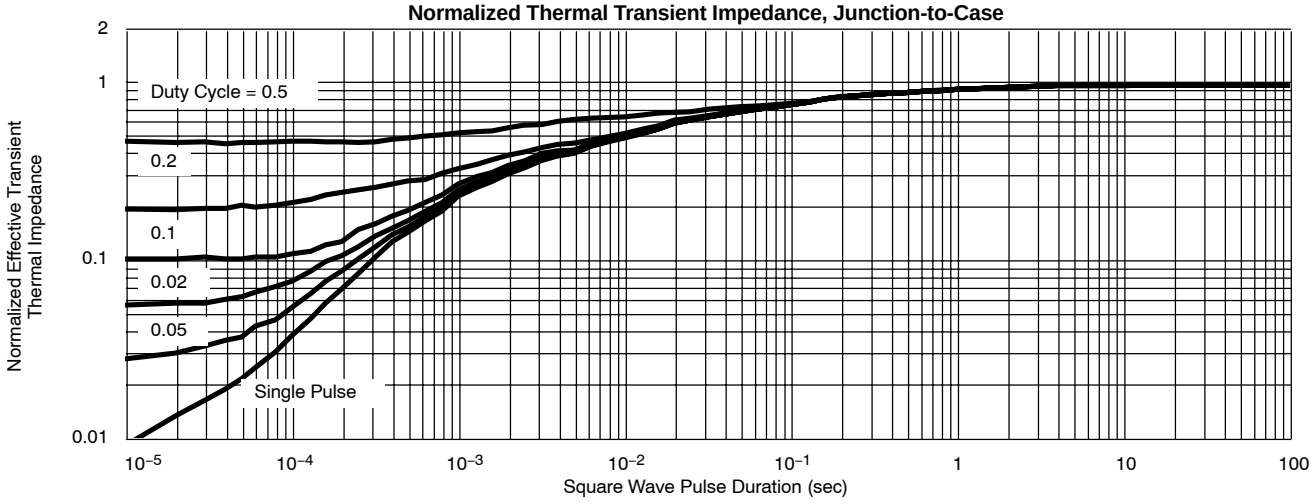
Maximum Avalanche Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71253.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.