Low-Voltage, 0.4-Ω r_{ON}, Single SPST Analog Switch

DESCRIPTION

The DG2715/2716 are low voltage, single supply, dual SPST analog switches. Designed for high performance switching of analog signals, the DG2715/2716 provide low on-resistance (0.4 Ω at + 2.7 V), fast speed (t_{ON}, t_{OFF} at 17 ns and 14 ns) and the ability to handle signals over the entire analog voltage range.

When operated on a + 3 V supply, control pins are compatible with 1.8 V digital logic. Additionally, on-resistance flatness and matching (0.05 Ω and 0.1 Ω) offer high accuracy between channels.

Built on Vishay Siliconix's low voltage submicron CMOS process, the DG2715/16 were designed to offer solutions that extend beyond audio/video functions, to providing the performance required for today's demanding mixed-signal switching in portable applications.

The DG2715 contains a normally open (NO) switch, and the DG2716 contains a normally closed switch. An epitaxial layer prevents latch-up. All switches conduct equally well in both directions when on, and block up to the power supply level when off.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

FEATURES

- Low Voltage Operation (1.6 V to 3.6 V)
- Low On-Resistance - $r_{DS(on)}$: 0.4 Ω at 2.7 V
- Off-Isolation: - 57 dB at 1 MHz
- Fast Switching: 25 ns t_{ON}
- Low Charge Injection - Q_{INJ}: 9 pC
- Low Power Consumption: < 1 µW
- SC-70 5-Lead Package

Pb-free
RoHS COMPLIANT

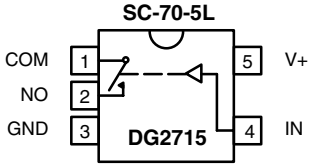
BENEFITS

- High Accuracy
- High Bandwidth
- TTL and Low Voltage Logic Compatibility
- Low Power Consumption
- Reduced PCB Space

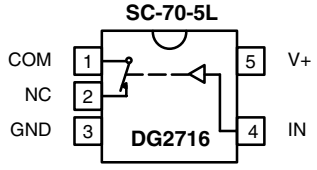
APPLICATIONS

- Mixed Signal Routing
- Portable and Battery Operated Systems
- Low Voltage Data Acquisition
- Modems
- PCMCIA Cards

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View
Device Marking: F7



Top View
Device Marking: F6

TRUTH TABLE - DG2715	
Logic	**Switch**
0	OFF
1	ON

TRUTH TABLE - DG2716	
Logic	**Switch**
0	ON
1	OFF

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	SC70-5	DG2715DL-T1-E3
		DG2716DL-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 4	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC and COM Pins)		± 200	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 300	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Power Dissipation (Packages)[b]	5-Pin SC-70[c]	250	mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 1.8 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, ± 10 %, V_{IN} = 0.4 V or 1.0 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 1.8 V, V_{COM} = 0.9 V, I_{NO}, I_{NC} = 10 mA	Room Full[d]		0.7	1.5 2.0	Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 2.0 V, V_{NO}, V_{NC} = 0.2 V/1.8 V, V_{COM} = 1.8 V/0.2 V	Room Full[d]	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full[d]	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 2.0 V, V_{NO}, V_{NC} = V_{COM} = 0.2 V/1.8 V	Room Full[d]	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.0			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		4		pF
Input Current[f]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF Figures1 and 2	Room Full[d]		24	36	ns
Turn-Off Time[d]	t_{OFF}		Room Full[d]		21	33	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		13		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 57		dB
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		78		pF
Channel-On Capacitance[d]	C_{ON}		Room		93		

SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 V or 1.4 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V I_{NO}, I_{NC} = 100 mA	Room Full		0.4	0.6	Ω
r_{ON} Flatness	r_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0.6 V, 1.5 V, 2.1 V I_{NO}, I_{NC} = 100 mA	Room		0.1	0.2	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance[d]	C_{in}		Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF Figure 1	Room Full		17	29	ns
Turn-Off Time	t_{OFF}		Room Full		14	26	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		9		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 57		dB
NO, NC Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		72		pF
Channel-On Capacitance[d]	C_{ON}		Room		92		
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	V+ = 3.6 V, V_{IN} = 0 or V+			0.01	1.0	µA

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Typical values are for design aid only, not guaranteed nor subject to production testing.

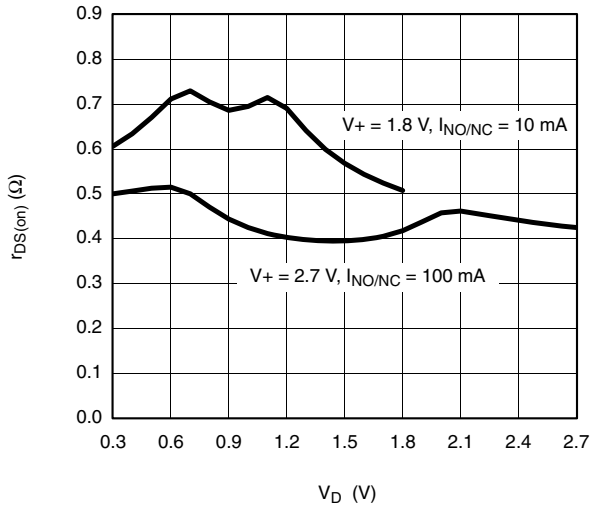
d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

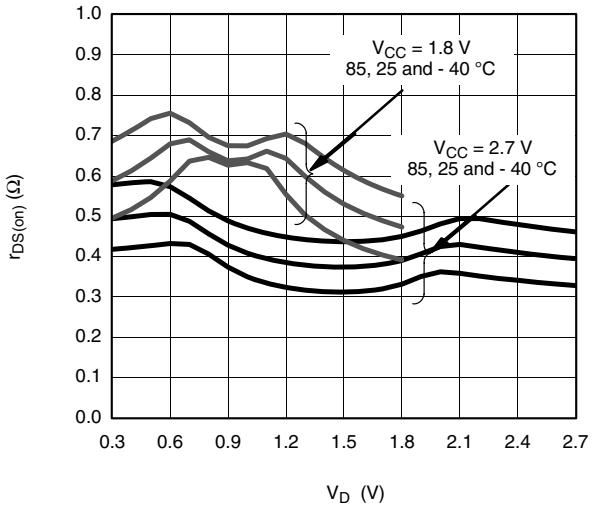
f. Guaranteed by 3 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

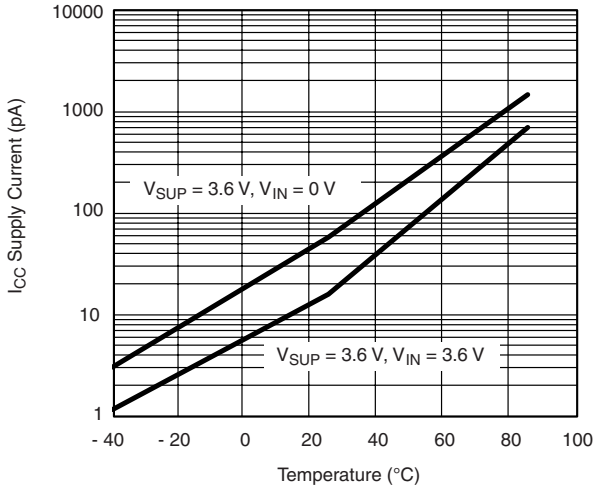
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



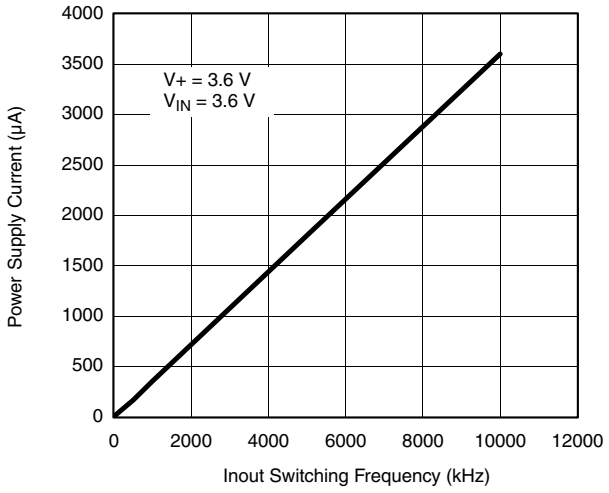
$r_{DS(on)}$ vs. V_{COM} vs. 1 V_{CC}



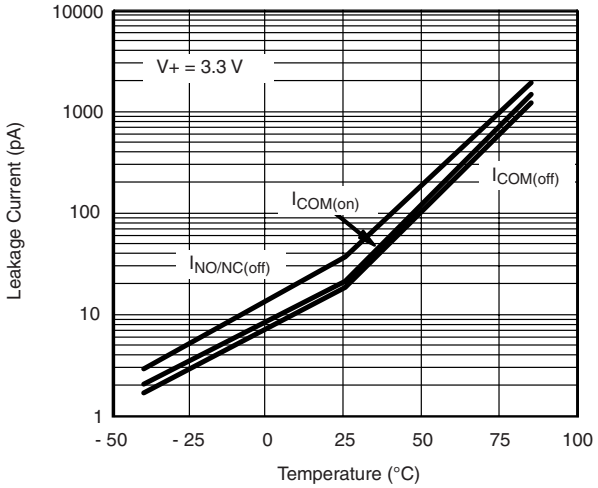
$r_{DS(on)}$ vs. V_D, V_{CC} and Temperature



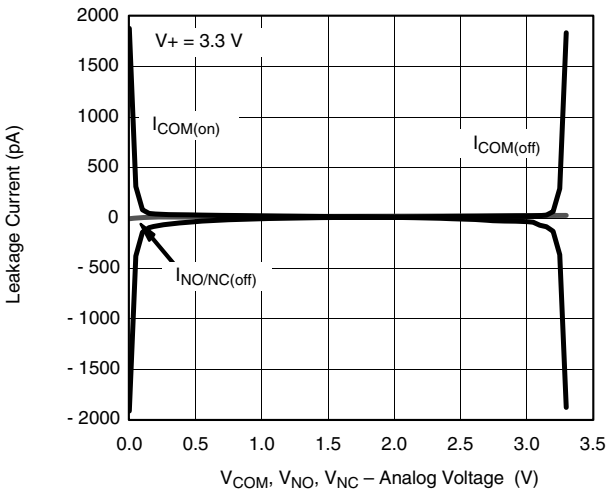
Supply Current vs. Temperature



Switching Frequency vs. Supply Current

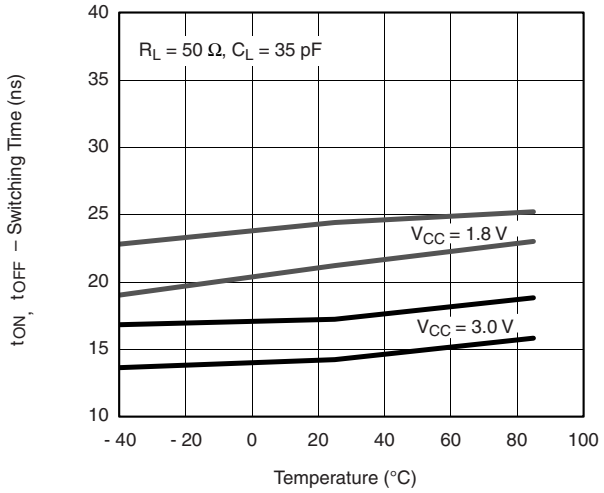


Leakage Current vs. Temperature

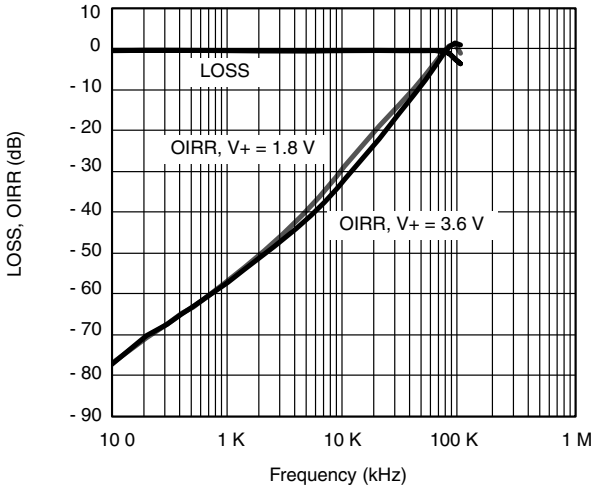


Leakage Current vs. Analog Voltage

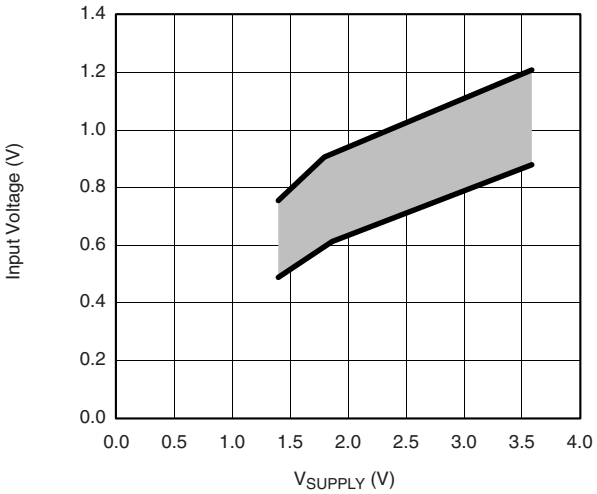
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



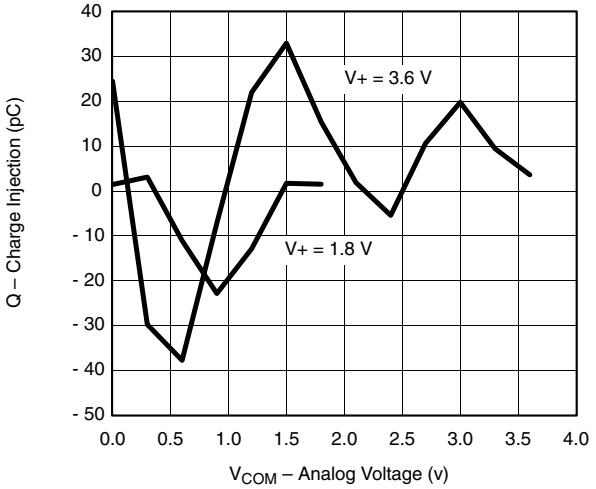
Switching Time vs. V_{CC} and Temperature



Insertion Loss, Off-Isolation vs. Frequency

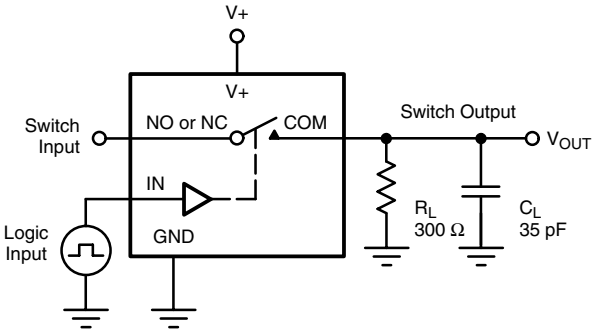


Threshold vs. Supply Voltage



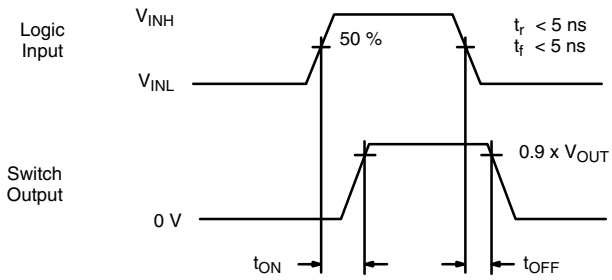
Charge Injection vs. Analog Voltage

TEST CIRCUITS



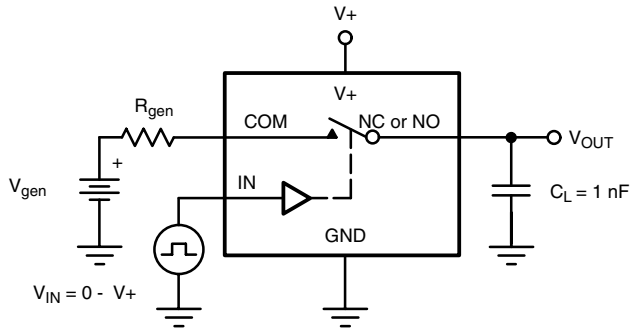
C_L (includes fixture and stray capacitance)

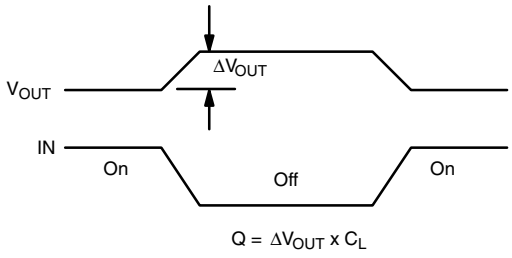
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection

TEST CIRCUITS

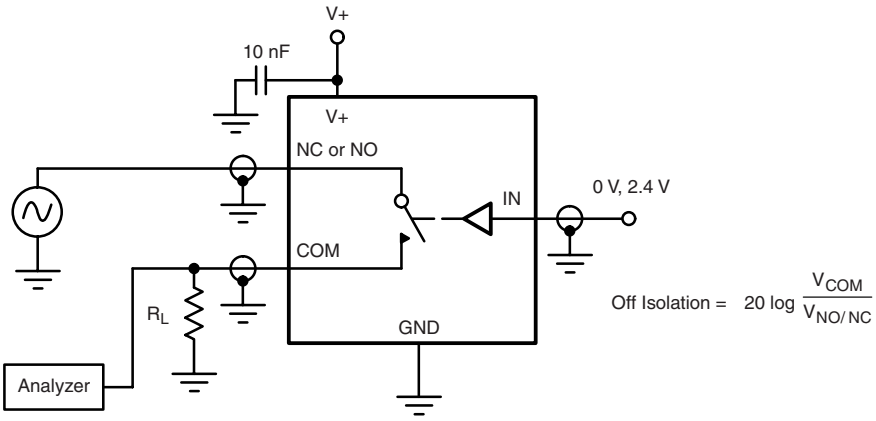


Figure 3. Off-Isolation

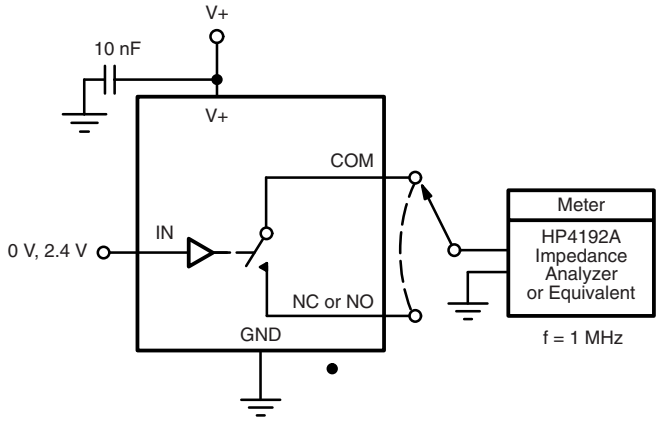


Figure 4. Channel Off/On Capacitance

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