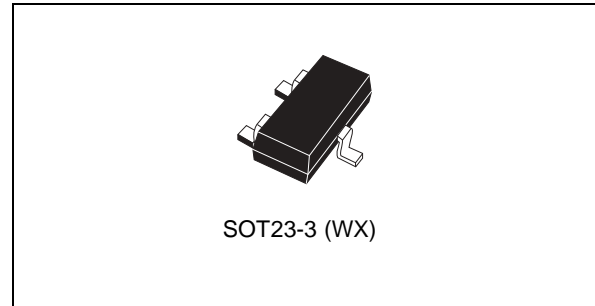


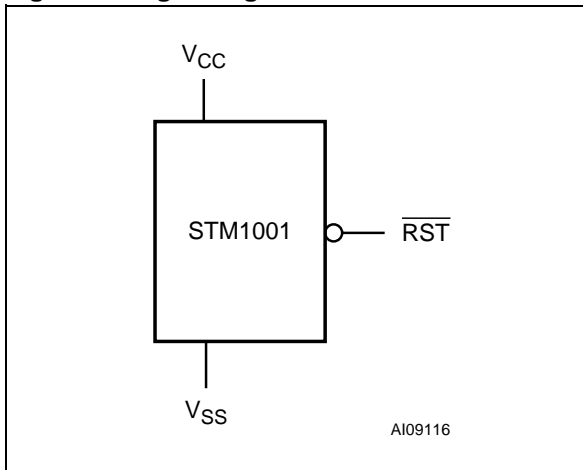
### FEATURES SUMMARY

- PRECISION MONITORING OF 3V, 3.3V, and 5V SUPPLY VOLTAGES
- OPEN DRAIN  $\overline{\text{RST}}$  OUTPUT
- 140ms RESET PULSE WIDTH (min)
- LOW SUPPLY CURRENT - 6 $\mu$ A (typ)
- GUARANTEED  $\overline{\text{RST}}$  ASSERTION DOWN TO  $V_{\text{CC}} = 1.0\text{V}$
- OPERATING TEMPERATURE:  
-40°C to 85°C (Industrial Grade)
- LEAD-FREE, SMALL SOT23 PACKAGE

**Figure 2. Package**



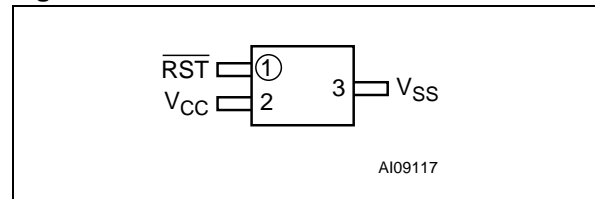
**Figure 1. Logic Diagram**



**Table 1. Signal Names**

$V_{\text{SS}}$	Ground
$\overline{\text{RST}}$	Active-Low RESET Output (Open Drain)
$V_{\text{CC}}$	Supply Voltage

**Figure 3. SOT23-3 Connections**



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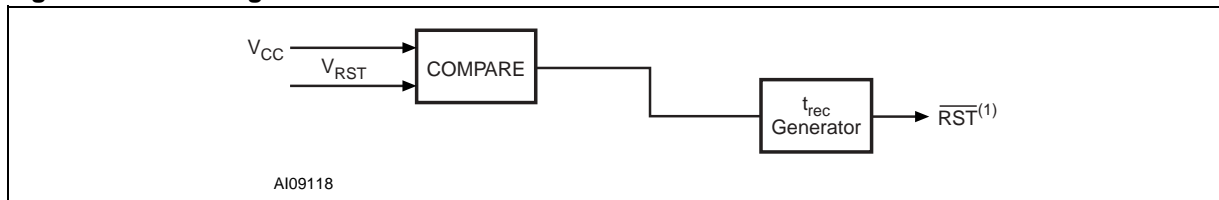
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### SUMMARY DESCRIPTION

The STM1001 MICROPROCESSOR RESET Circuit is a low-power supervisory device used to monitor power supplies. It performs a single function: asserting a reset signal whenever the  $V_{CC}$

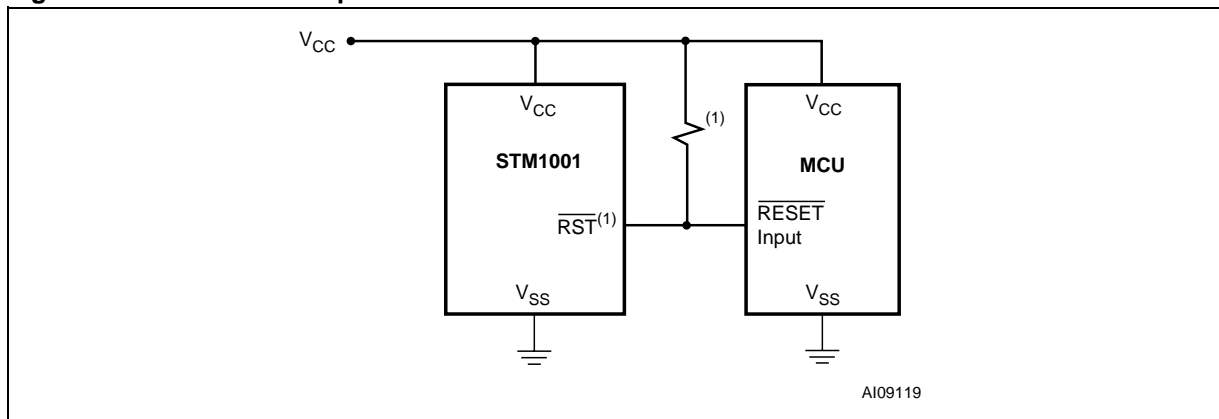
supply voltage drops below a preset value and keeping it asserted until  $V_{CC}$  has risen above the preset threshold for a minimum period of time ( $t_{rec}$ ).

Figure 4. Block Diagram



Note: 1. Open Drain

Figure 5. Hardware Hookup



Note: 1.  $\overline{RST}$  output requires pull-up resistor.

### OPERATION

#### Reset Output

The STM1001 MICROPROCESSOR RESET CIRCUIT asserts a reset signal to the MCU whenever  $V_{CC}$  goes below the reset threshold ( $V_{RST}$ ).  $\overline{RST}$  is guaranteed valid down to  $V_{CC} = 1V$  ( $0^\circ$  to  $70^\circ C$ ).

During power-up, once  $V_{CC}$  exceeds the reset threshold an internal timer keeps  $\overline{RST}$  low for the reset time-out period,  $t_{rec}$ . After this interval,  $\overline{RST}$  returns high.

If  $V_{CC}$  drops below the reset threshold,  $\overline{RST}$  goes low. Each time  $\overline{RST}$  is asserted, it stays low for at least the reset time-out period. Any time  $V_{CC}$  goes below the reset threshold, the internal timer clears. The reset timer starts when  $V_{CC}$  returns above the reset threshold. The active-low reset ( $\overline{RST}$ ) is an open drain output.

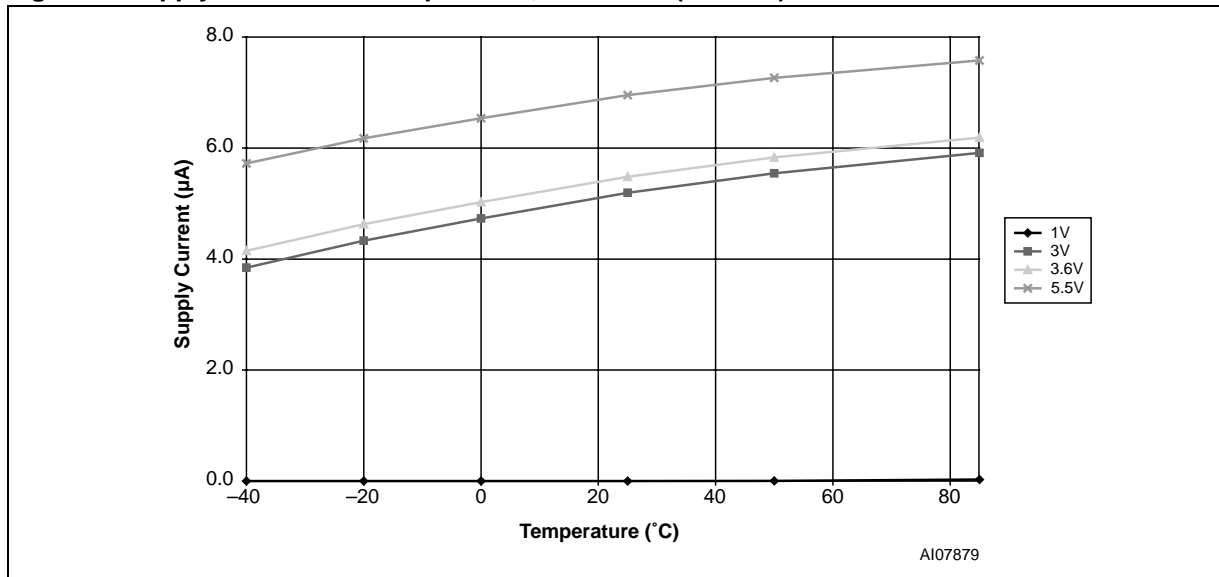
#### Negative-Going $V_{CC}$ Transients

The STM1001 is relatively immune to negative-going  $V_{CC}$  transients (glitches). Figure 11., page 7 shows typical transient duration versus reset comparator overdrive (for which the STM1001 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to  $V_{CC}$ , starting at 0.5V above the actual reset threshold and ending below it by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative  $V_{CC}$  transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts 20 $\mu$ s or less will not cause a reset pulse. A 0.1 $\mu$ F bypass capacitor mounted as close as possible to the  $V_{CC}$  pin provides additional transient immunity.

### TYPICAL OPERATING CHARACTERISTICS

**Note:** Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  for L/M versions,  $V_{CC} = 3.3\text{V}$  for T/S versions, and  $V_{CC} = 3.0\text{V}$  for R versions.

**Figure 6. Supply Current vs. Temperature, L/M/R/S/T (no load)**



**Figure 7. Power-down Reset Delay vs. Temperature -  $V_{OD} = V_{TH} - V_{CC}$  (L/M)**

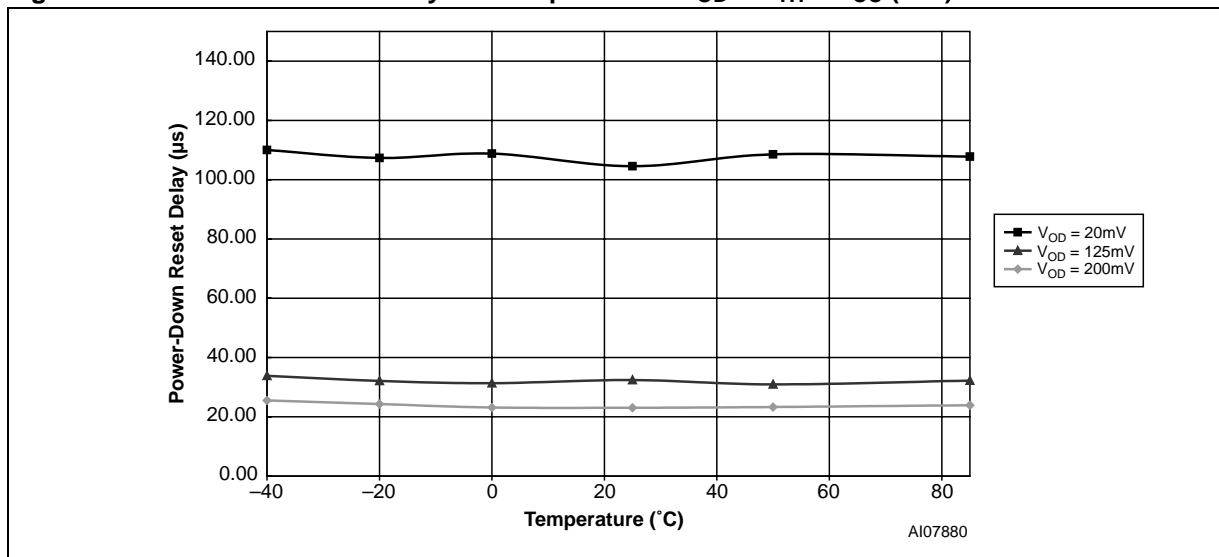


Figure 8. Power-down Reset Delay vs. Temperature -  $V_{OD} = V_{TH} - V_{CC}$  (R/S/T)

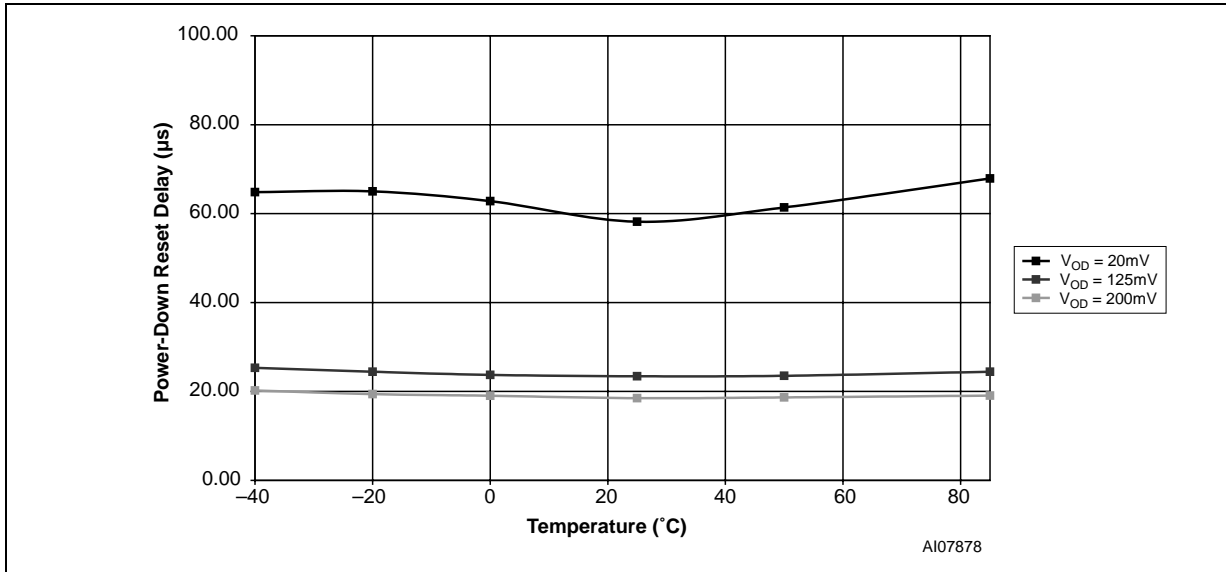


Figure 9. Power-up  $t_{rec}$  vs. Temperature

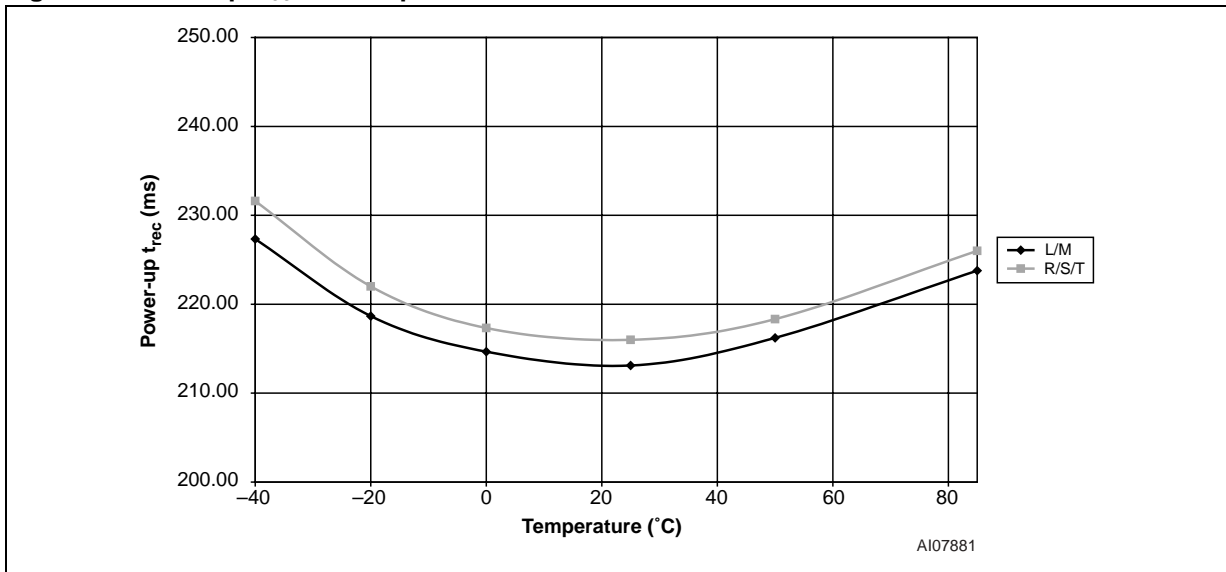


Figure 10. Normalized Reset Threshold vs. Temperature

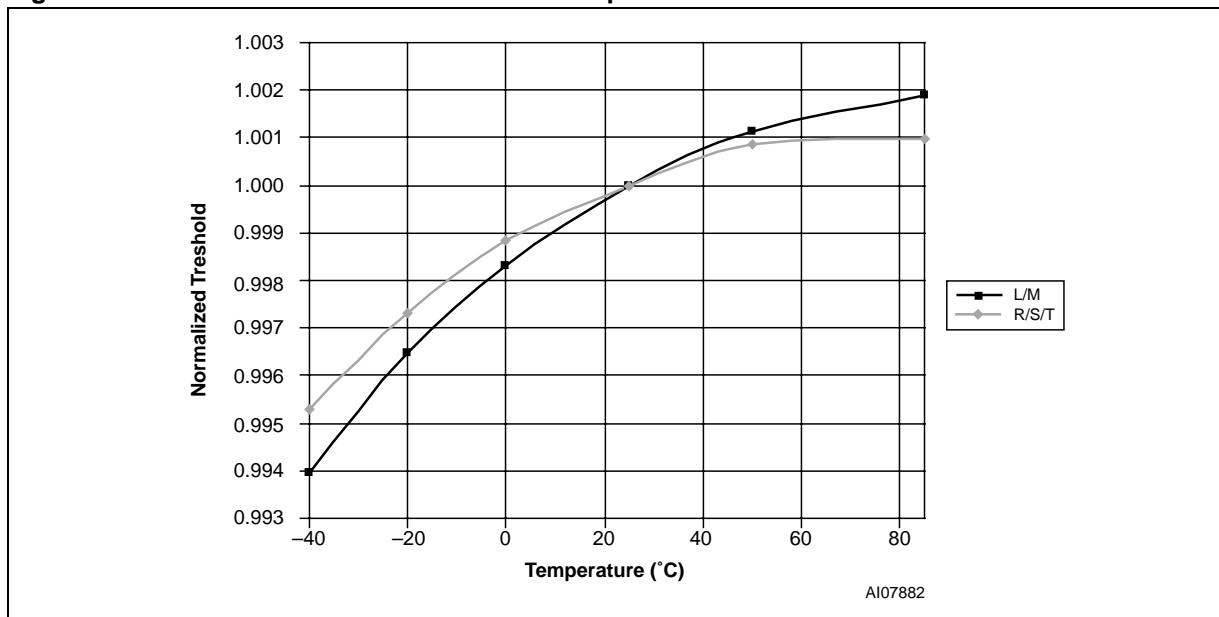
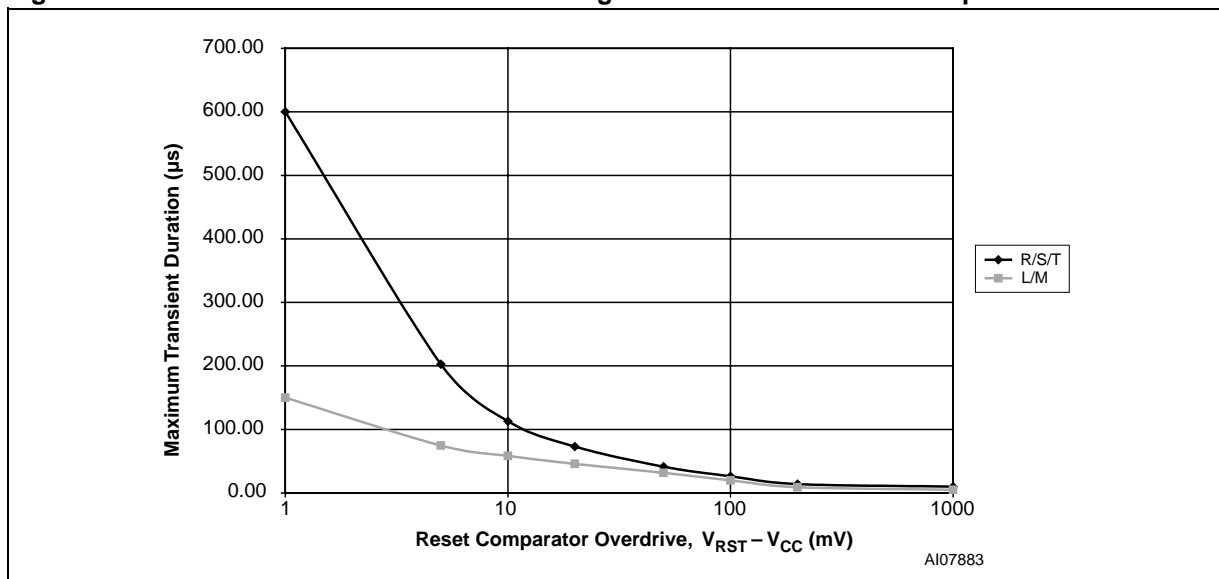


Figure 11. Max Transient Duration NOT Causing Reset Pulse vs. Reset Comparator Overdrive



## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)	-55 to 150	°C
T <sub>SLD</sub> <sup>(1)</sup>	Lead Solder Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>CC</sub>	Supply Voltage	-0.3 to 7.0	V
I <sub>O</sub>	Output Current	20	mA
P <sub>D</sub>	Power Dissipation	320	mW

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

## DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement

Conditions summarized in Table 3, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 3. Operating and AC Measurement Conditions**

Parameter	STM1001	Unit
V <sub>CC</sub> Supply Voltage	1.0 to 5.5	V
Ambient Operating Temperature (T <sub>A</sub> )	-40 to 85	°C
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	0.2 to 0.8V <sub>CC</sub>	V
Input and Output Timing Ref. Voltages	0.3 to 0.7V <sub>CC</sub>	V

**Figure 12. AC Testing Input/Output Waveforms**

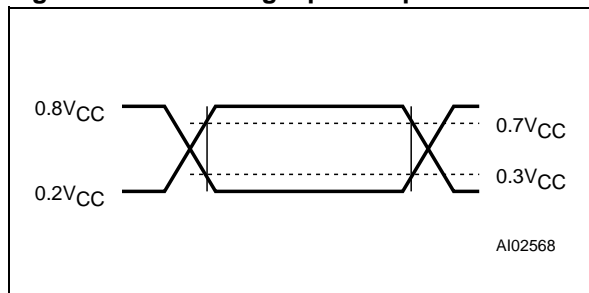




Table 4. DC and AC Characteristics

Sym	Alternative	Description	Test Condition <sup>(1)</sup>	Min	Typ	Max	Unit			
V <sub>CC</sub>		Operating Voltage	T <sub>A</sub> = -40 to +85°C	1.2		5.5	V			
			T <sub>A</sub> = 0 to +70°C	1.0		5.5	V			
I <sub>CC</sub>		V <sub>CC</sub> Supply Current	V <sub>CC</sub> < 3.6V		5.5	10	μA			
			V <sub>CC</sub> < 5.5V		7	15	μA			
I <sub>LO</sub>		Open Drain Reset Output Leakage Current	V <sub>CC</sub> > V <sub>RST</sub> , Reset not asserted	-1		+1	μA			
V <sub>OL</sub>		$\overline{\text{RST}}$ Output Low Voltage	STM1001R/S/T only, I <sub>OL</sub> = 1.2mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.3	V			
			STM1001L/M only, I <sub>OL</sub> = 3.2mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.4	V			
V <sub>OL</sub>		$\overline{\text{RST}}$ Output Low Voltage	I <sub>OL</sub> = 50μA; V <sub>CC</sub> > 1.0V			0.3	V			
<b>RESET Thresholds</b>										
V <sub>RST</sub>		Reset Threshold	STM1001L	25°C	4.56	4.63	4.70	V		
				-40 to 85°C	4.50		4.75	V		
			STM1001M	25°C	4.31	4.38	4.45	V		
				-40 to 85°C	4.25		4.50	V		
			STM1001T	25°C	3.04	3.08	3.11	V		
				-40 to 85°C	3.00		3.15	V		
			STM1001S	25°C	2.89	2.93	2.96	V		
				-40 to 85°C	2.85		3.00	V		
			STM1001R	25°C	2.59	2.63	2.66	V		
				-40 to 85°C	2.55		2.70	V		
					V <sub>RST</sub> Temperature Coefficient	V <sub>CC</sub> = 3.3V		45		ppm/ C
					V <sub>CC</sub> to $\overline{\text{RST}}$ Delay	V <sub>CC</sub> = V <sub>RST</sub> to (V <sub>RST</sub> - 100mV)	STM1001L/M	40		μs
		STM1001R/S/T	20				μs			
	t <sub>rec</sub>	$\overline{\text{RST}}$ Pulse Width		140	210	280	ms			

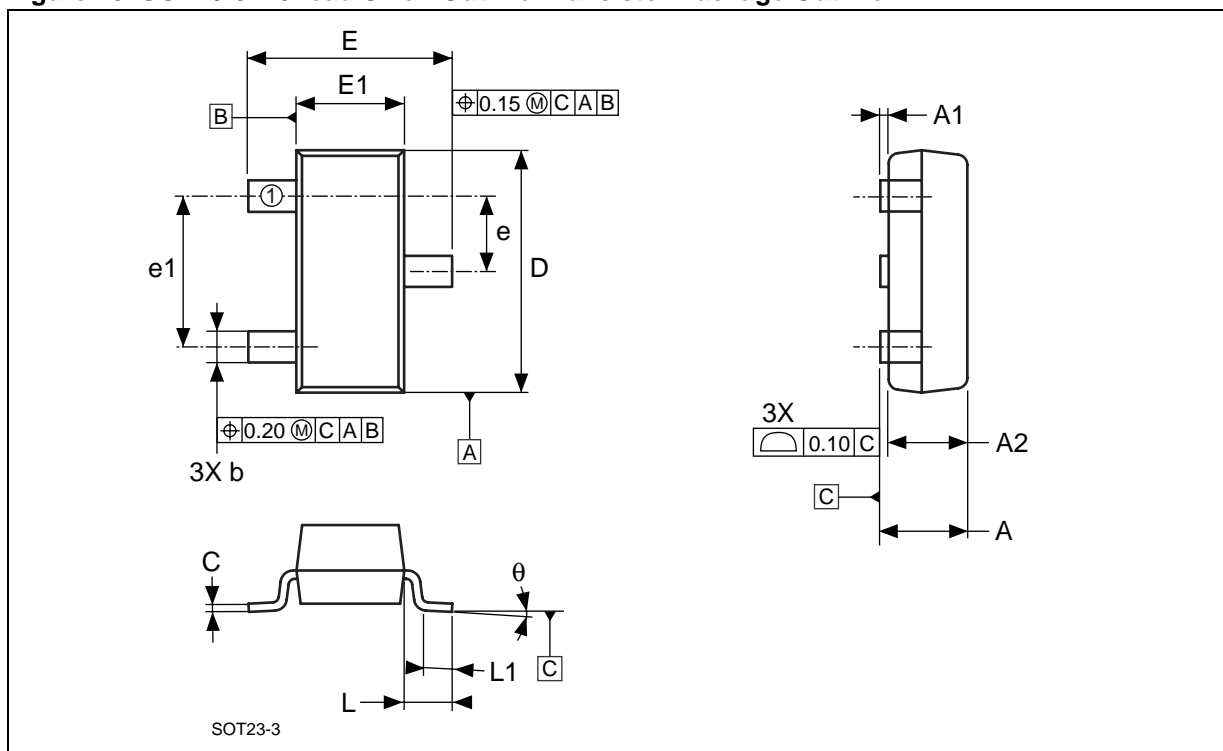
Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = -40 to 85°C; V<sub>CC</sub> = 1.2V to 5.5V (except where noted).  
2. "Glitches" of 100ns or less typically will not generate a RESET pulse.

**PACKAGE MECHANICAL**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 13. SOT23-3 – 3-lead Small Outline Transistor Package Outline



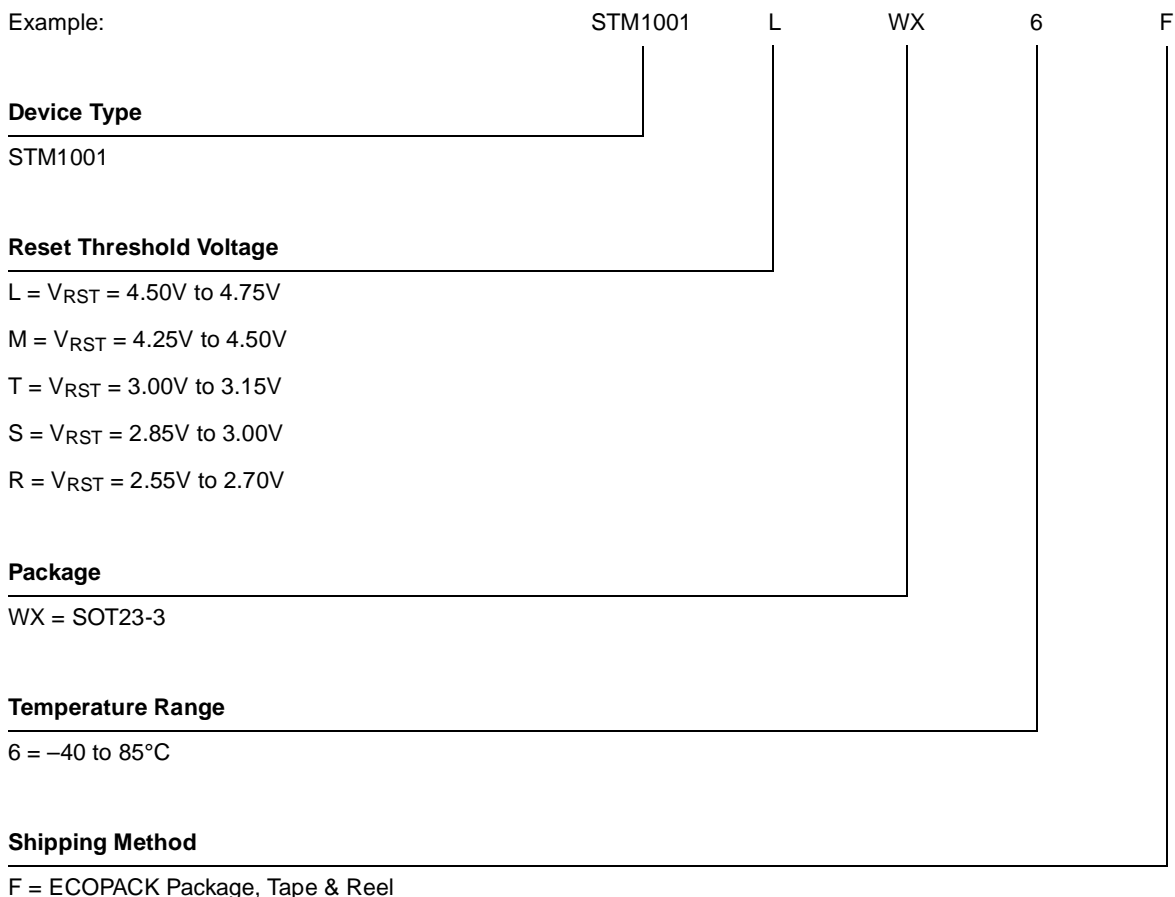
Note: Drawing is not to scale.

Table 5. SOT23-3 – 3-lead Small Outline Transistor Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.30	0.50		0.012	0.020
C		0.08	0.20		0.003	0.008
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e		0.89	1.03		0.035	0.041
e1		1.78	2.05		0.070	0.081
L	0.54			0.021		
L1		0.40	0.60		0.016	0.024
$\theta$		0°	8°		0°	8°
N		3			3	

## PART NUMBERING

**Table 6. Ordering Information Scheme**



For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

**Table 7. Marking Description**

Part Number	Reset Threshold	Output	Topside Marking <sup>(1)</sup>
STM1001L	4.63V	Open Drain $\overline{RST}$	8BAx
STM1001M	4.38V	Open Drain $\overline{RST}$	8BBx
STM1001T	3.08V	Open Drain $\overline{RST}$	8BCx
STM1001S	2.93V	Open Drain $\overline{RST}$	8BDx
STM1001R	2.63V	Open Drain $\overline{RST}$	8BEx

Note: 1. Lowercase "x" indicates date code.

## REVISION HISTORY

**Table 8. Document Revision History**

Date	Version	Revision Details
09-Dec-03	1.0	First Edition
19-Feb-04	2.0	Part number changed from STM6301
22-Mar-04	2.1	Update DC Characteristics (Table 4)
09-Apr-04	3.0	Device promoted; reformatted; marking updated (Table 7)
19-Nov-04	4.0	Update dimensions (Table 5)
19-Sep-05	5.0	Remove "Valid $\overline{RST}$ Output Down to $V_{CC}$ ..." text

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