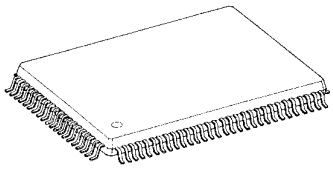
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9446FG

Audio Digital Processor for Decode of Dolby Digital (AC-3), MPEG2 Audio

TC9446FG is the various digital signal processor for decoding. It contains the decode processing program which embraced encoding signals, such as Dolby Digital (AC-3)/Pro Logic (Note 1), MPEG2 audio and DTS (Note 2).

Decoding of Dolby Digital or MPEG2 audio is made with a single chip. Moreover, an external memory can be connected to the TC9446FG to decode DTS.



P-QFP100-1420-0.65Q

Weight: 1.57 g (typ.)

Features

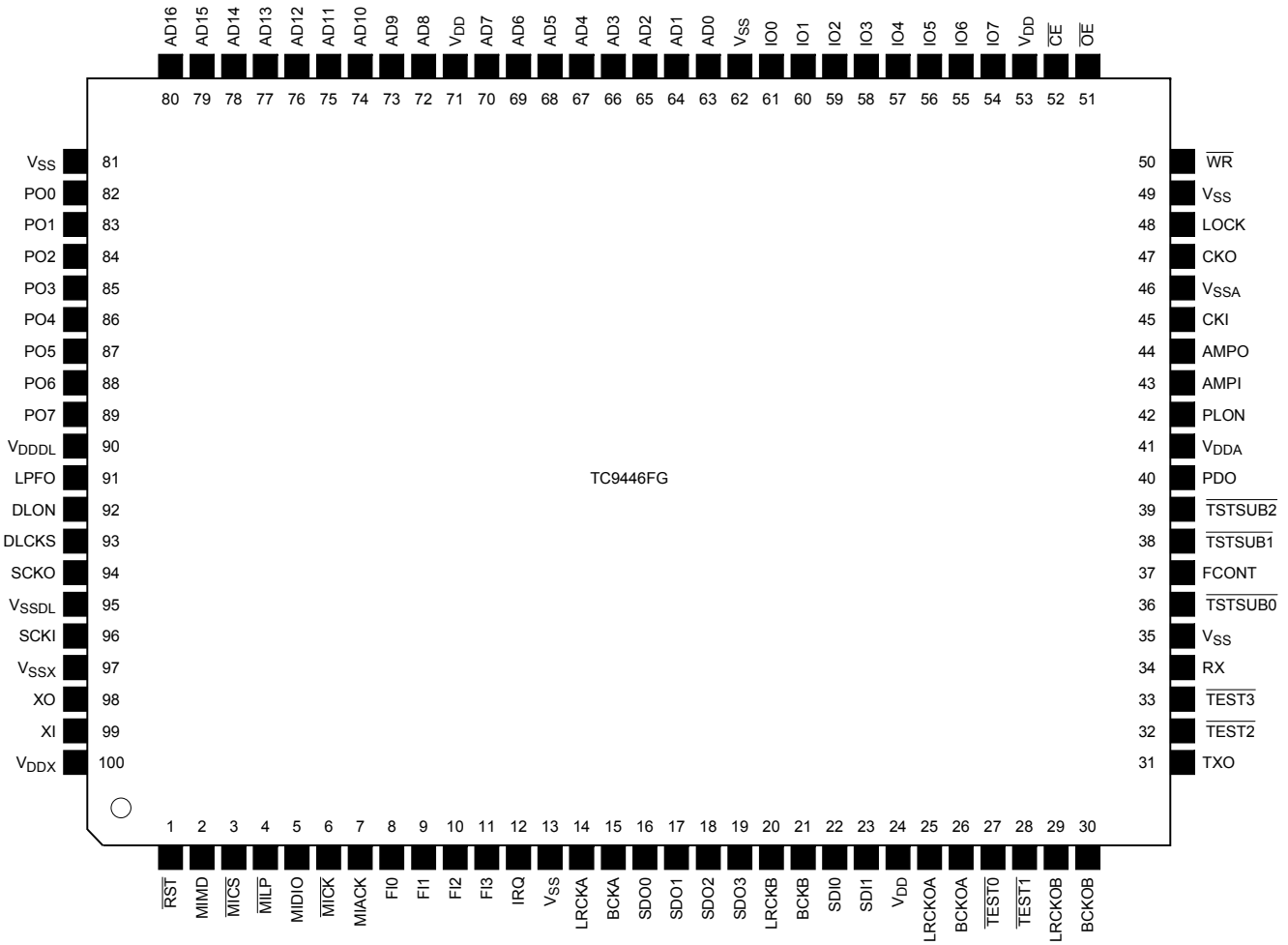
- Dolby digital (AC-3) or MPEG2 audio decode
  Acceptable bit rate upto 640 kbps
- Audio interface
  4 output port, 2 input port (2 port of LRCK and BCK)
  DIR (digital audio interface receiver) built-in
  DIT (digital audio interface transmitter) built-in
  DIR and DIT are available upto 96 kHz sampling of 2 channel
- Operating clock: DLL oscillator upto 6th times for DSP clock
- Instruction cycle: 20 ns/1 instruction at 50 MIPS operation
- DSP
  Processor: 24 bit × 24 bit + 51 bit multiplier and adder, 51 bit ALU
  Data bus: 24 bit × 3
  Data RAM: 12 k word
  Coefficient ROM: 4 k word
  Program ROM: 12 k word
  Program RAM: 128 word
- MCU interface: Serial interface or I^2C bus interface
- Others
  It is possible to connect external RAM, 256 k or 1 M SRAM
  External interruption input terminal
  Flag input terminal: 4 inputs
  General-purpose output port: 8 outputs (The ports can be used as interrupt outputs to MCU and logic control outputs.)
  incorrect operation detect
- Operating Voltage: 3.0 ± 0.3 V
- In CMOS structure and high-speed processing
- 100 pin flat package design

Note 1: “Dolby”, “Pro Logic”, and the double-D symbol are trademarks of Dolby Laboratories.

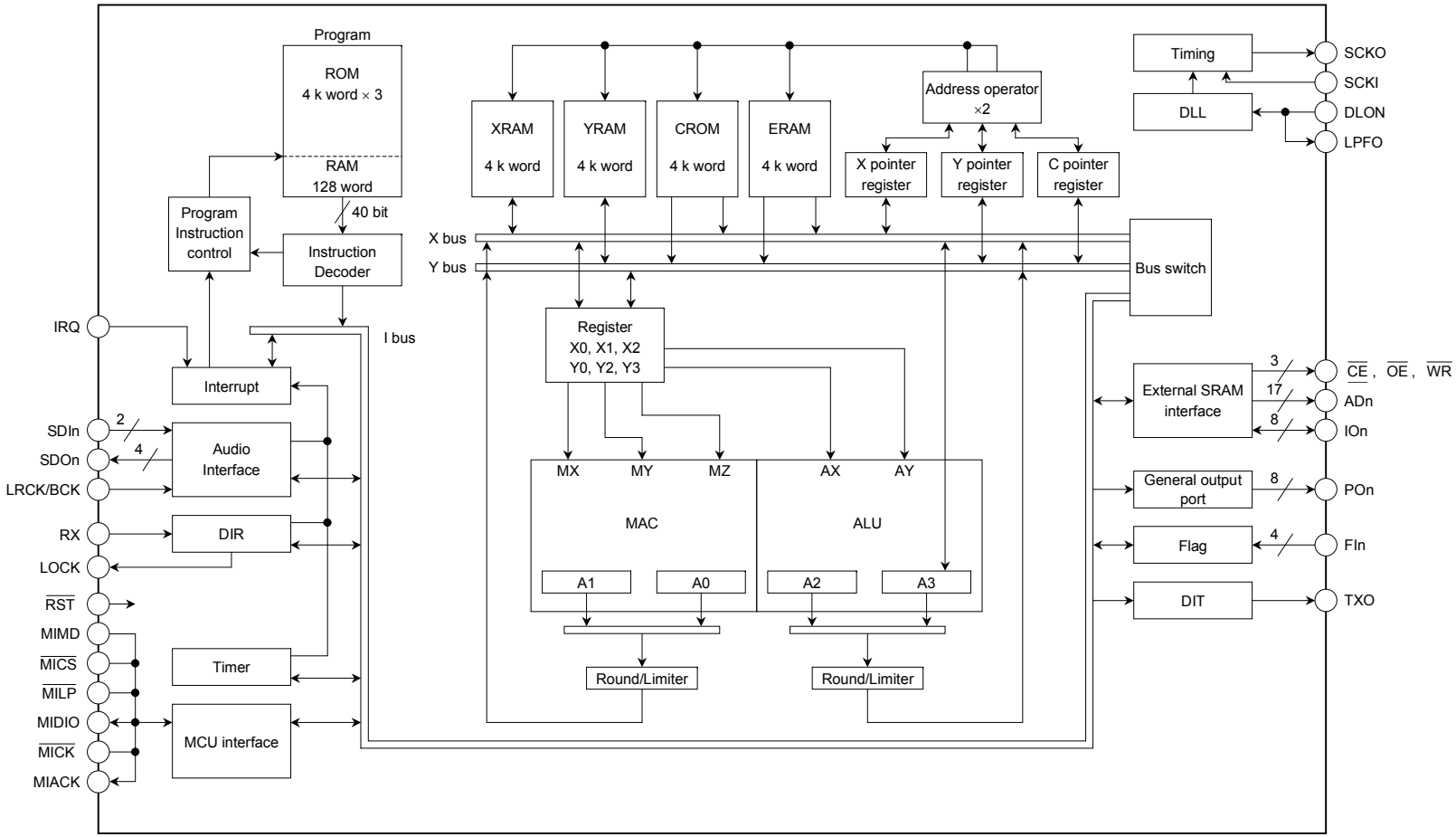
Note 2: “DTS” and “DTS Digital Surround” are registered trademarks of Digital Theater Systems, Inc.

Note 3: Since this product has a weak terminal in serge voltage, please advise handling it enough.

Pin Connection



Block Diagram



Pin Functions

Pin No.	Symbol	I/O	Description of Pin Functions	Remarks
1	$\overline{RST}$	I	Reset signal input terminal (L: reset, H: normal operation)	Pull-up resistor, Schmitt input
2	MIMD	I	Mode select input for MCU interface (L: serial, H: I^2C bus)	Pull-down resistor, Schmitt input
3	$\overline{MICS}$	I	Chip select input for MCU interface	Schmitt input
4	$\overline{MILP}$	I	Latch pulse input for MCU interface	Schmitt input
5	MIDIO	I/O	Data input and output for MCU interface	Schmitt input/ Open-drain output
6	$\overline{MICK}$	I	Clock input for MCU interface	Schmitt input
7	MIACK	O	Acknowledge output for MCU interface	
8	FI0	I	Flag input 0	Pull-up resistor, Schmitt input
9	FI1	I	Flag input 1	Pull-up resistor, Schmitt input
10	FI2	I	Flag input 2	Pull-up resistor, Schmitt input
11	FI3	I	Flag input 3	Pull-up resistor, Schmitt input
12	IRQ	I	Interruption input	Pull-down resistor, Schmitt input
13	V_{SS}	—	Digital ground	
14	LRCKA	I	LR clock input-A for audio interface	Schmitt input
15	BCKA	I	Bit clock input-A for audio interface	Schmitt input
16	SDO0	O	Data output-0 for audio interface	
17	SDO1	O	Data output-1 for audio interface	
18	SDO2	O	Data output-2 for audio interface	
19	SDO3	O	Data output-3 for audio interface	
20	LRCKB	I	LR clock input-B for audio interface	Schmitt input
21	BCKB	I	Bit clock input-B for audio interface	Schmitt input
22	SDI0	I	Data input-0 for audio interface	Schmitt input
23	SDI1	I	Data input-1 for audio interface	Schmitt input
24	V_{DD}	—	Digital power supply	
25	LRCKOA	O	LR clock output-A for audio interface	
26	BCKOA	O	Bit clock output-A for audio interface	
27	$\overline{TEST0}$	I	Test input-0 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
28	$\overline{TEST1}$	I	Test input-1 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
29	LRCKOB	O	LR clock output-B for audio interface	
30	BCKOB	O	Bit clock output-B for audio interface	
31	TXO	O	SPDIF output	
32	$\overline{TEST2}$	I	Test input-2 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
33	$\overline{TEST3}$	I	Test input-3 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
34	RX	I	SPDIF input	Schmitt input
35	V_{SS}	—	Digital ground	

Pin No.	Symbol	I/O	Description of Pin Functions	Remarks
36	$\overline{\text{TSTSUB0}}$	I	Test sub input-0 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
37	FCONT	O	Frequency control output for VCO circuit	Tri-state output
38	$\overline{\text{TSTSUB1}}$	I	Test sub input-1 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
39	$\overline{\text{TSTSUB2}}$	I	Test sub input-2 (L: test, H: normal operation)	Pull-up resistor, Schmitt input
40	PDO	O	Phase detect signal output	Tri-state output
41	V_{DDA}	—	Analog power supply	
42	PLON	I	Clock selection input (L: external clock, H: VCO clock)	Pull-up resistor, Schmitt input
43	AMPI	I	Amplifier input for Low pass filter	
44	AMPO	O	Amplifier output for Low pass filter	
45	CKI	I	External clock input	
46	V_{SSA}	—	Analog ground	
47	CKO	O	DIR clock output	
48	LOCK	O	VCO lock output	
49	V_{SS}	—	Digital ground	
50	$\overline{\text{WR}}$	O	Write signal output for external SRAM	
51	$\overline{\text{OE}}$	O	Enable signal output for external SRAM	
52	$\overline{\text{CE}}$	O	Chip enable signal output for external SRAM	
53	V_{DD}	—	Digital power supply	
54	IO7	I/O	Data I/O-7 for external SRAM	Pull-up resistor
55	IO6	I/O	Data I/O-6 for external SRAM	Pull-up resistor
56	IO5	I/O	Data I/O-5 for external SRAM	Pull-up resistor
57	IO4	I/O	Data I/O-4 for external SRAM	Pull-up resistor
58	IO3	I/O	Data I/O-3 for external SRAM	Pull-up resistor
59	IO2	I/O	Data I/O-2 for external SRAM	Pull-up resistor
60	IO1	I/O	Data I/O-1 for external SRAM	Pull-up resistor
61	IO0	I/O	Data I/O-0 for external SRAM	Pull-up resistor
62	V_{SS}	—	Digital ground	
63	AD0	O	Address output-0 for external SRAM	Pull-up resistor
64	AD1	O	Address output-1 for external SRAM	Pull-up resistor
65	AD2	O	Address output-2 for external SRAM	Pull-up resistor
66	AD3	O	Address output-3 for external SRAM	Pull-up resistor
67	AD4	O	Address output-4 for external SRAM	Pull-up resistor
68	AD5	O	Address output-5 for external SRAM	Pull-up resistor
69	AD6	O	Address output-6 for external SRAM	Pull-up resistor
70	AD7	O	Address output-7 for external SRAM	Pull-up resistor
71	V_{DD}	—	Digital power supply	
72	AD8	O	Address output-8 for external SRAM	Pull-up resistor
73	AD9	O	Address output-9 for external SRAM	Pull-up resistor
74	AD10	O	Address output-10 for external SRAM	Pull-up resistor
75	AD11	O	Address output-11 for external SRAM	Pull-up resistor
76	AD12	O	Address output-12 for external SRAM	Pull-up resistor
77	AD13	O	Address output-13 for external SRAM	Pull-up resistor

Pin No.	Symbol	I/O	Description of Pin Functions	Remarks
78	AD14	O	Address output-14 for external SRAM	Pull-up resistor
79	AD15	O	Address output-15 for external SRAM	Pull-up resistor
80	AD16	O	Address output-16 for external SRAM	Pull-up resistor
81	V_{SS}	—	Digital ground	
82	PO0	O	General output port-0	Pull-up resistor
83	PO1	O	General output port-1	Pull-up resistor
84	PO2	O	General output port-2	Pull-up resistor
85	PO3	O	General output port-3	Pull-up resistor
86	PO4	O	General output port-4	Pull-up resistor
87	PO5	O	General output port-5	Pull-up resistor
88	PO6	O	General output port-6	Pull-up resistor
89	PO7	O	General output port-7	Pull-up resistor
90	V_{DDDL}	—	Power supply for DLL circuit	
91	LPFO	O	Low pass filter output for DLL circuit	
92	DLON	I	DLCKS pin / DLON pin / DLL clock setting	Pull-up resistor
93	DLCKS	I	"L" / "L" / SCKI input (DLL = off) "L" / "H" / 4th times of XI clock "H" / "L" / 3rd times of XI clock "H" / "H" / 6th times of XI clock	Pull-up resistor
94	SCKO	O	ASP clock output	
95	V_{SSDL}	—	Ground for DLL circuit	
96	SCKI	I	External system clock input	
97	V_{SSX}	—	Ground for crystal oscillator	
98	XO	O	Crystal oscillator output	
99	XI	I	Crystal oscillator input	
100	V_{DDX}	—	Digital power supply	

Description of Operation

1. Micro Controller Interface

The TC9446FG can perform transmission and reception of serial data with a micro controller in the serial mode or the I^2C mode.

MIMD terminal performs a change in the serial mode and the I^2C mode, and input and output of data are performed at MSB first.

The use terminal and the function in the serial mode and the I^2C mode are shown in Table 1.

The bit composition of a 24 bit command is shown in Table 2.

Note 4: This data sheet shows the general control method, refer to the program explanation data of an attached sheet for a detailed command list, the control method, etc.

Table 1 Use Terminal and Function in the Serial Mode and the I^2C Mode

Transmission Mode		Serial Mode (MIMD = L)	I^2C Mode (MIMD = H)
Terminal	Input/Output	Functions	Functions
$\overline{\text{MICS}}$	Input (3-5 V)	Chip selection signal input	Not used (fixed “L”)
$\overline{\text{MILP}}$	Input (3-5 V)	Latch pulse signal input	Not used (fixed “L”)
MIDIO	Input (3-5 V)/Output (3 V)	Data input/output	Data input/output (SDA)
$\overline{\text{MICK}}$	Input (3-5 V)	Clock input	Clock input (SCL)
MIACK	Output (3 V)	Acknowledge signal output and out of control detection output	Out of control detection output

Note 5: MIDIO terminal needs pull-up resistance for the terminal exterior because of an open-drain output. When using it by I^2C bus, pull-up resistance is required also for MICK terminal.

Note 6: The addresses of an I^2C bus are write-in address 3Ah and read-out address 3Bh.

Table 2 Bit Composition of 24 Bit Command

Bit Assign	Functions	Remarks
23-8	16 bit address	Refer to the command list of the program explanation data sheet
7	Starting the incorrect operation detection output	Starting the incorrect operation detection output by “1”
6	Starting the program RAM boot	Starting the program RAM boot by “1”
5	Setting the soft reset	Setting the soft reset ON by “1”
4	Setting the Read/Write (R/W)	Setting the read by “1”
3-0	Setting the number of words for transmission	“0h”; a word ↓ “Fh”; 16 words

2. Data Transmission Format

2-1. Serial Mode Setting

2-1-1. Data Transmission Format in the Serial Mode

A data transmission format in the serial mode is shown in Figure 1.

After the data transmission at the time of the serial mode sets $\overline{\text{MICS}}$ signal to "L", fundamentally, it checks that MIACK signal is "L" and transmits a 24 bit command at MSB first.

However, it cannot transmit at the time of MIACK signal = "H".

Then, the word set up by the 24 bit command which the Read or Write (R/W) of 24 bit data of a number (1-16 word) is performed, and, finally, $\overline{\text{MICS}}$ signal is set to "H".

However, since there is a term when MIACK signal after transmission is set to "H" in a 24 bit command, at the time of Read, command transmission back also needs to check that MIACK signal is set to "L".

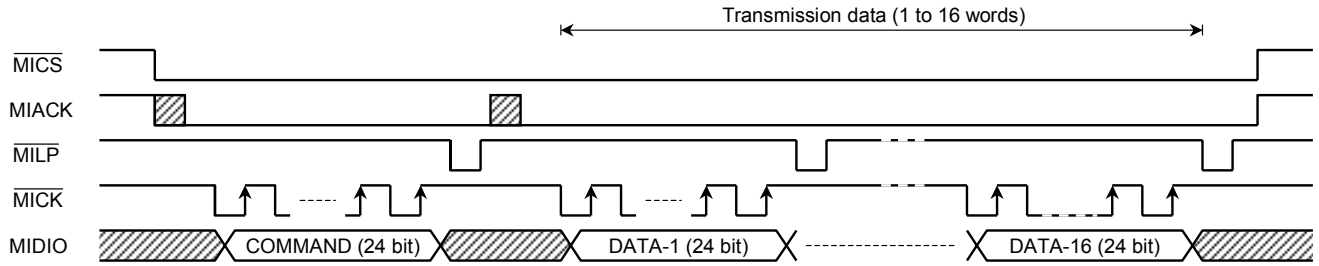


Figure 1 Serial Mode Data Transmission Format

2-1-2. Data Transmission Method in the Serial Transmission Mode

1) Program boot and a program start

As for TC9446FG, RAM is assigned 128 words of program address 0000h-007Fh, and the interruption vector address is become 0000h-0009h.

Therefore, in order to operate TC9446FG, it needs to interrupt and a program needs to be booted to a vector address. In addition, a program load needs to be continuously performed to an interruption vector address to store a program in 000Ah-007Fh.

In order to perform program boot, the program RAM boot start bit and the soft reset bit in the 24 bit command transmitted after reset need to be set to "H". (command = 000060h) And, after command transmission, program data (40 bit) is divided into 20 bit of a higher rank/low rank, and it transmits by the low-rank stuffing of 24 bit data in the order of a higher rank (20 bit) and a low rank (20 bit).

Since a write-in address is made automatic (+1) from 0000h, if it transmits the required number of words and $\overline{\text{MICS}}$ is set to "H", program boot will complete it.

In addition, the write-in address of program boot always starts from 0000h.

A start of a program carries out and transmits the soft reset bit in a 24 bit command to "L", and is performed by setting $\overline{\text{MICS}}$ to "H", without performing data transmission.

The procedure of program boot and a program start is shown in Figure 2.

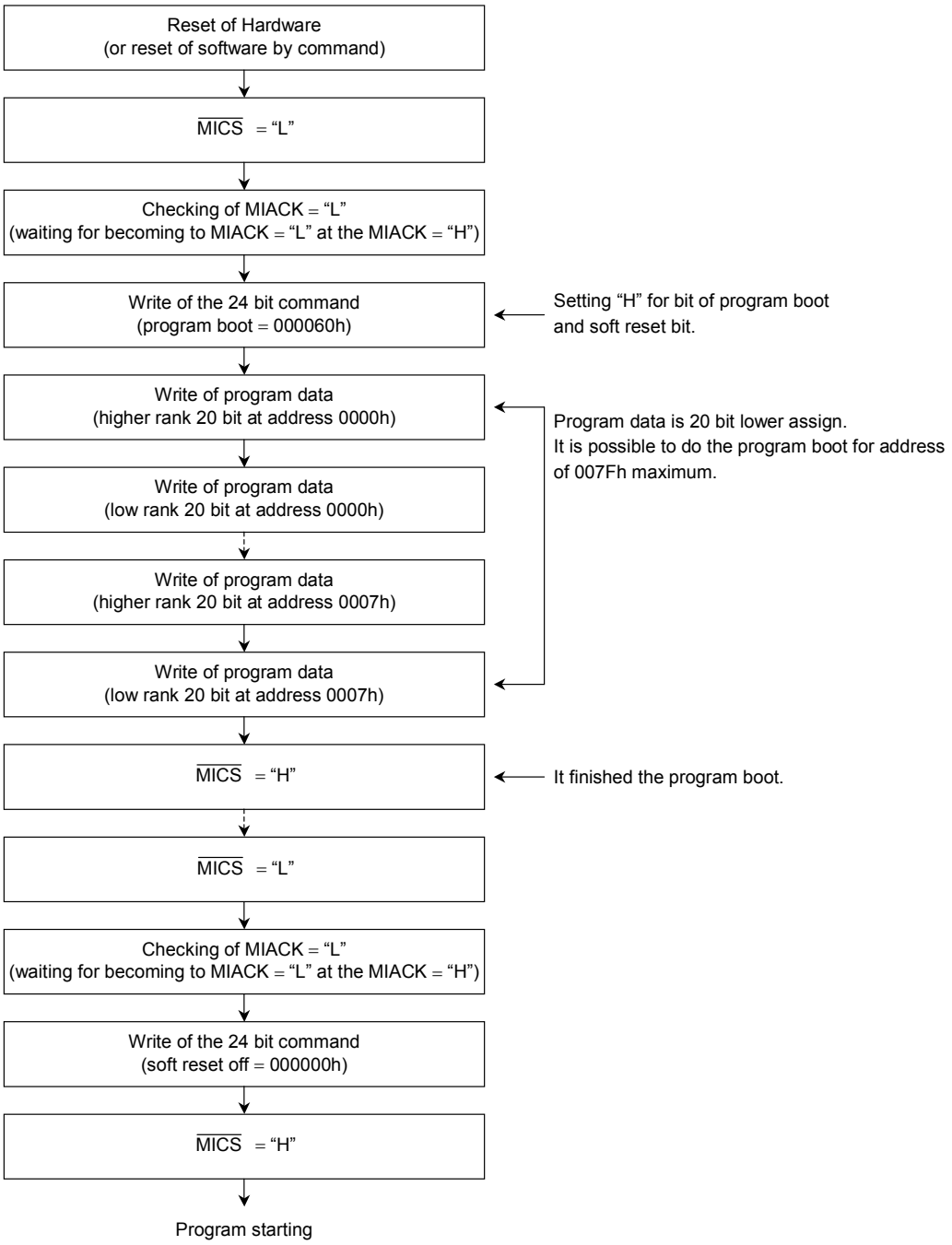


Figure 2 Procedure of Program Boot and Program Start

2) Write of 24 bit data

The number of words of data written in while data required for the 16 bit address in a 24 bit command is set up and R/W bit is set to "L", when writing in data from a MCU to TC9446FG during program operation is set up.

And, 24 bit data of the number required after transmitting a 24 bit command of words is written in.

The procedure of the write of 24 bit data is shown in Figure 3.

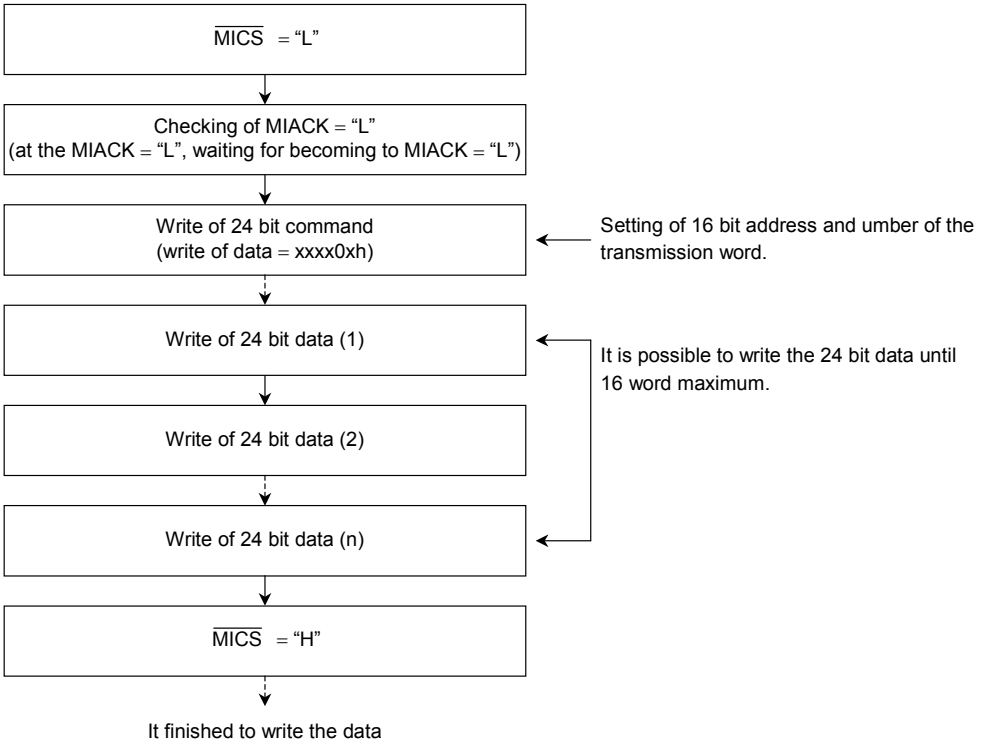


Figure 3 Procedure of Write of 24 Bit Data

3) Read-out of 24 bit data

The number of words of data read while data required for the 16 bit address in a 24 bit command is set up and R/W bit is set to "H", when reading data of TC9446FG from a MCU during program operation is set up.

And, after transmitting a 24 bit command, MIACK = "L" is checked and 24 bit data of the required number of words is read.

MIACK = "L" is checked after command transmission for waiting to set data which should be read to data buffer. The procedure of read-out of 24 bit data is shown in Figure 4.

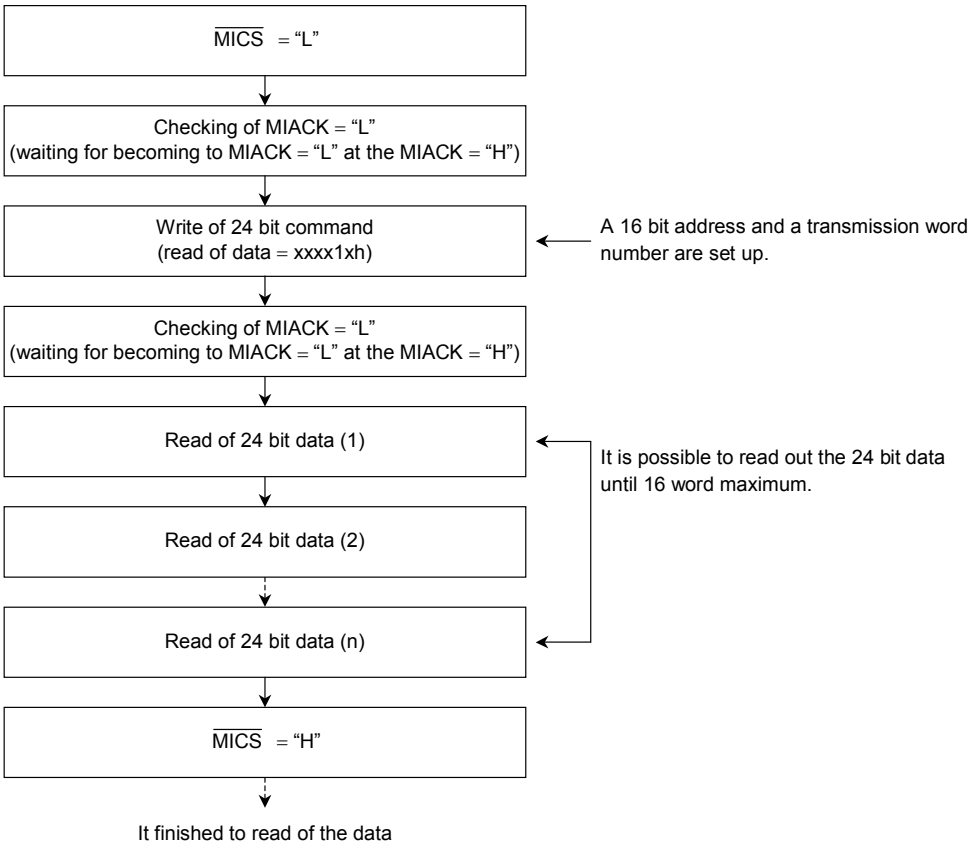


Figure 4 Procedure of Read-Out of 24 Bit Data

4) ON/OFF of soft reset

The case where a program is started after program boot, and in restarting a program, it performs ON/OFF of soft reset.

ON/OFF of soft reset are performed by carrying out and transmitting the bit of the soft reset in a 24 bit command to "H" (ON) and "L" (OFF).

Since data with which ON/OFF of soft reset follow a command is not required, it is made into $\overline{\text{MICS}}$ = "H" after 24 bit command transmission.

In addition, in order to return from a incorrect operation state, when turning ON soft reset, a 24 bit command can be transmitted irrespective of the state of MIACK signal.

The procedure of ON/OFF of soft reset is shown in Figure 5.

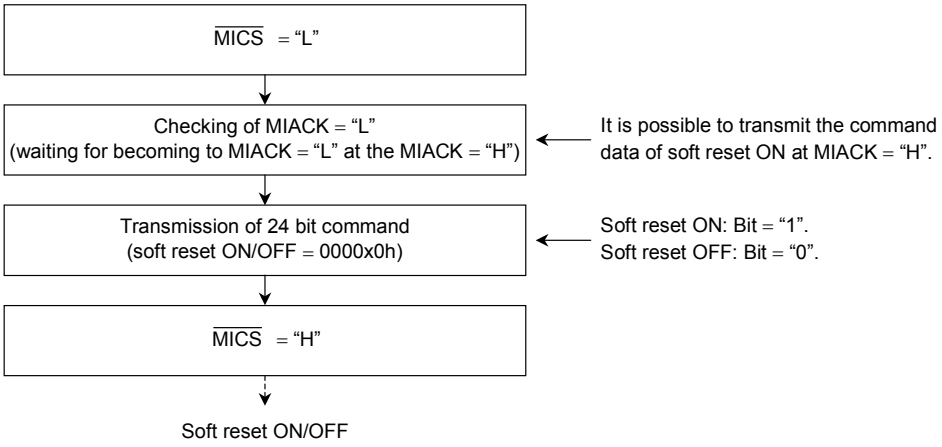


Figure 5 Procedure of ON/OFF of Soft Reset

5) Incorrect operation detection

Incorrect operation detection of the internal program of TC9446FG can be made to perform by setting the incorrect operation detection start bit in a 24 bit command to "H". As for this incorrect operation detection start bit, the reversal output only of the case of $\overline{\text{MICS}}$ terminal = "H" is carried out from MIACK terminal.

And, since this incorrect operation detection start bit is periodically cleared by "L" when an internal program is operating normally, MIACK terminal at the time of $\overline{\text{MICS}}$ terminal = "H" is set to "H" from "L".

However, since it will stop being cleared if an internal program becomes a incorrect operation state, as for MIACK terminal at the time of $\overline{\text{MICS}}$ terminal = "H", the state of "L" will continue.

Thus incorrect operation detection of a program is attained by supervising MIACK terminal at the time of $\overline{\text{MICS}}$ terminal = "H". Moreover, although it checks that MIACK terminal is "L" after setting $\overline{\text{MICS}}$ terminal to "L" in case a MCU starts access to TC9446FG, MCU can judge that an internal program is a incorrect operation state, when the state of MIACK = "H" continues.

In addition, when a incorrect operation state is detected, it can return from a incorrect operation state by initializing by transmitting the soft reset command which the reset terminal was set to "L" or was mentioned above.

The procedure of incorrect operation detection is shown in Figure 6.

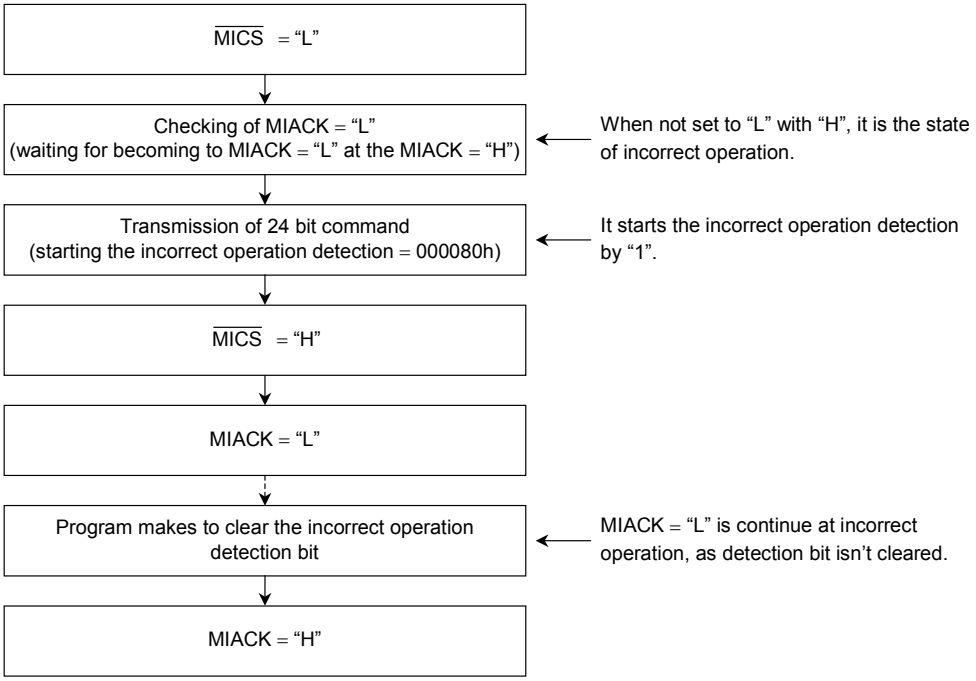


Figure 6 Procedure of Incorrect Operation Detection

2-2. I^2C Mode Setting

2-2-1. Data Transmission Format in I^2C Mode

The foundations of a data transmission format in the I^2C mode are shown in Figure 7.

Fundamentally, the data transmission at the time of the I^2C mode checks that ACK bit is set to "L", after making I^2C Address (write = 3Ah) to transmission.

However, at the time of "H", ACK bit performs Start Condition again, without performing STOP Condition, and transmits I^2C Address (3Ah). I^2C Transmit 24 bit command after Address transmission.

And, at the time of data Write of TC9446FG, Write of 24 bit data of the number (1-16 word) of words set up by 24 bit command is performed from a MCU, and, finally, END Condition is transmitted.

Moreover, it checks that transmit I^2C Address (read = 3Bh) from TC9446FG at the time of Read to a MCU, without performing END Condition after 24 bit command transmission, and ACK bit is set to "L".

However, at the time of "H", ACK bit performs Start Condition again, without performing STOP Condition, and transmits I^2C Address (3Bh).

The word set up by 24 bit command after checking that ACK bit is "L". Although Read of 24 bit data of a number (1-16 word) is performed, as for the inside of Read, a MCU needs to set ACK bit to "L" for every 8-bit Read data.

And, only ACK bit added to the last 8 bits is set to "H", and STOP Condition is transmitted.

Moreover, at the time of transmission of only a 24 bit command which does not perform R/W of data, END Condition is transmitted after 24 bit command transmission.

In addition, in TC9446FG, polling of the access demand from a MCU is carried out every about 6 ms at the time of decode processing. Therefore, R/W of data from a MCU need to be performed at the interval of 6 ms or more.

At the time of Write-in, Read-out and a command only shows the transmission format to Figure 7 to Figure 10.

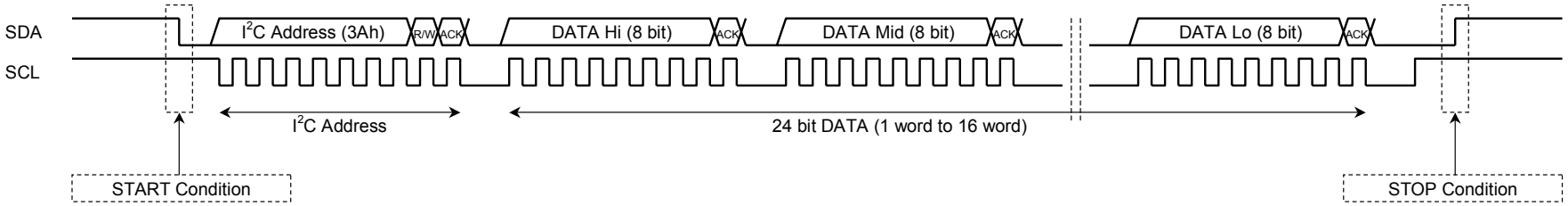


Figure 7 Data Transmission Format in the I^2C Mode

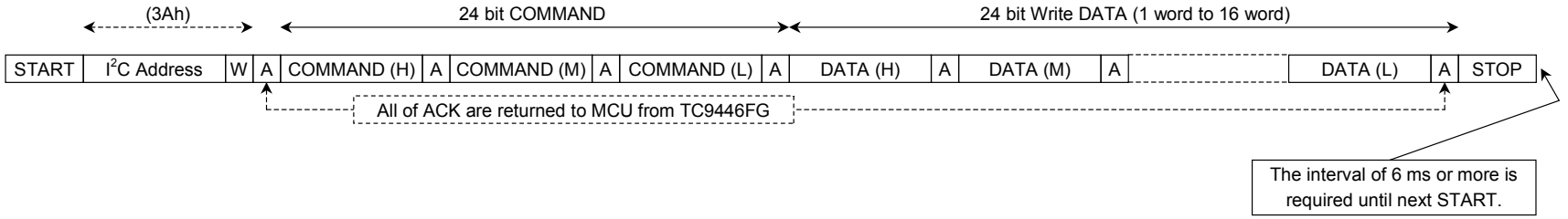


Figure 8 Format at Time of Write

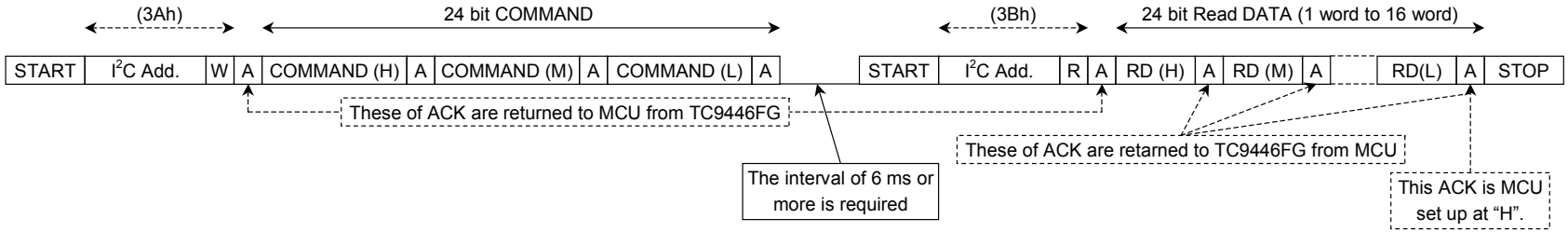


Figure 9 Format at Time of Read

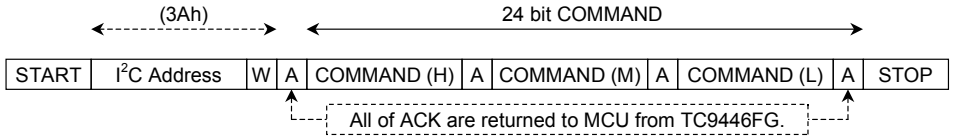


Figure 10 Format Only a Command at the Time of Transmission.

2-2-2. The Data Transmission Method in I^2C Mode

1) Program boot and a program start

As for TC9446FG, RAM is assigned 128 words of program address 0000h-007Fh, and the interruption vector address is become 0000h-0009h.

Therefore, in order to operate TC9446FG, it needs to interrupt at least and a program needs to be booted to a vector address.

In addition, a program load needs to be continuously performed to an interruption vector address to store a program in 000Ah-007Fh.

In order to perform program boot, the program RAM boot start bit and the soft reset bit in the 24 bit command transmitted after reset need to be set to "H". (command = 000060h)

And after command transmission, program data (40 bits) is divided into 20 bits of a higher rank/low rank, and it transmits by the low-rank stuffing of 24 bit data in the order of a higher rank (20 bits) and a low rank (20 bits).

Since a write-in address is made automatic (+1) from 0000h, if it transmits the required number of words and END Condition is transmitted, program boot will complete it.

In addition, the write-in address of program boot always starts from 0000h.

A start of a program is performed by carrying out and transmitting the soft reset bit in a 24 bit command to "L", and transmitting END Condition, without performing data transmission.

The procedure of program boot and a program start is shown in Figure 11.

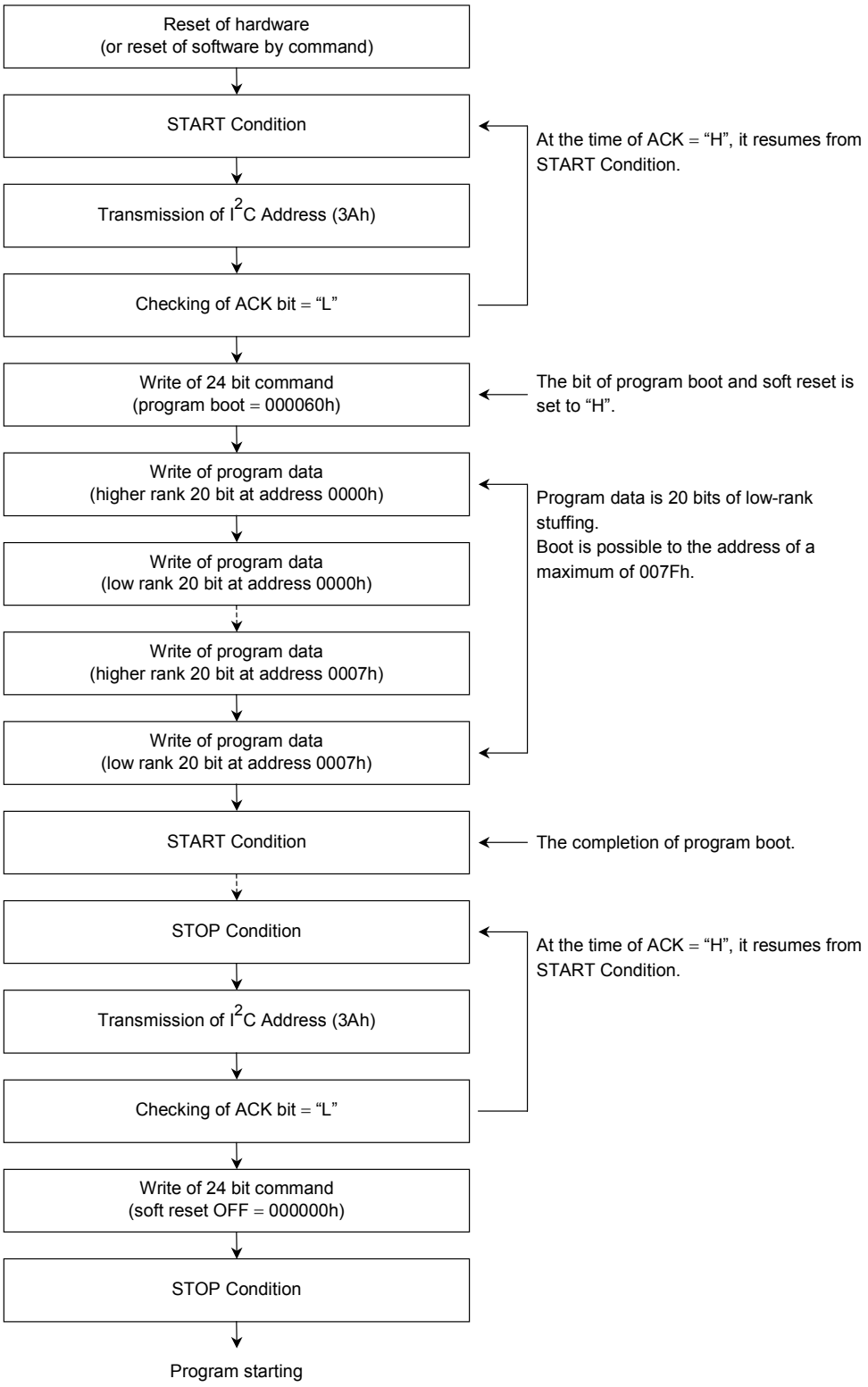


Figure 11 Procedure of Program Boot and Program Start

2) Write of 24 bit data

The number of words of data written in while data required for the 16 bit address in a 24 bit command is set up and R/W bit is set to "L", when writing in data from a MCU to TC9446FG during program operation is set up.

And, 24 bit data of the number required after transmitting a 24 bit command of words is written in.

In addition, completion of internal taking in of write-in data requires the time of about 6 ms of the maximum from END Condition.

Therefore, access of a next MCU needs to keep the term for about 6 ms after END Condition transmission.

The procedure of the write of 24 bit data is shown in Figure 12.

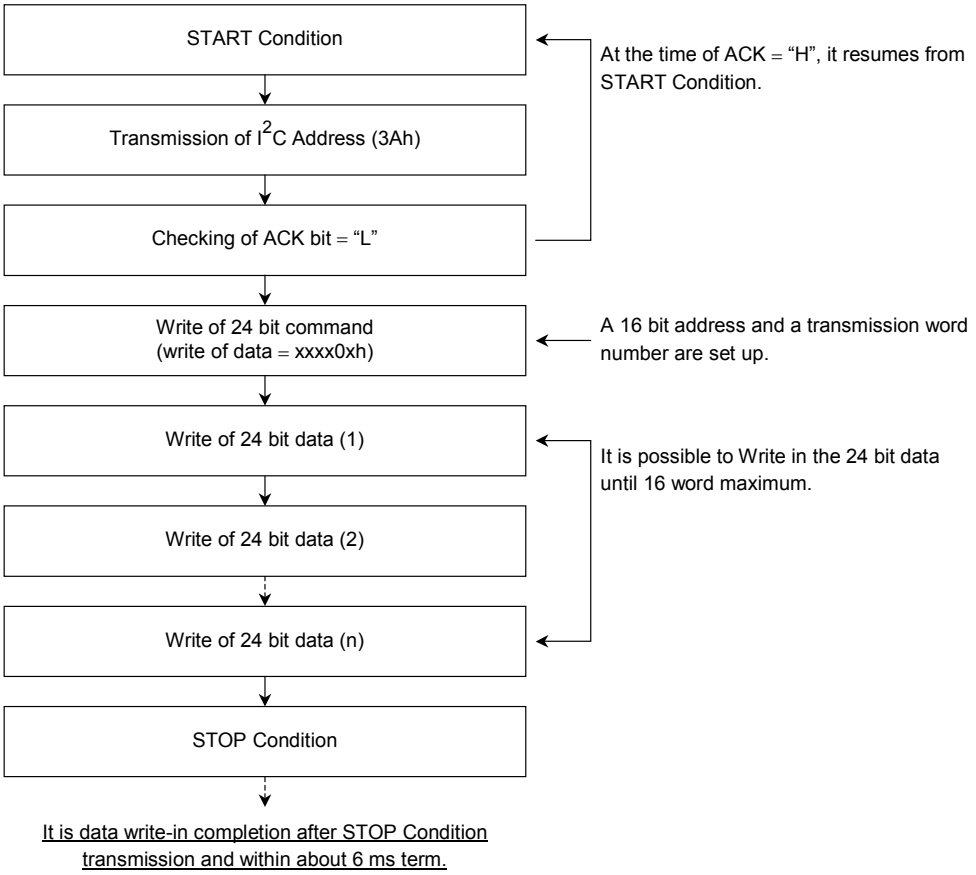


Figure 12 Procedure of Write of 24 Bit Data

3) Read of 24 bit data

The number of words of data read while data required for the 16 bit address in a 24 bit command is set up and R/W bit is set to "L", when reading data of TC9446FG from a MCU during program operation is set up.

And, after transmitting a 24 bit command, I^2C Address is set to 3Bh after the term progress for about 6 ms, and it transmits with START Condition. Then, 24 bit data of the required number of words is read.

Although ACK bit of a data Read term needs to give "L" from a MCU, it needs to set only ACK bit added to last 8 bit data to "H".

This is because the Basra in of SDA where TC9446FG are the master is opened wide and a MCU can transmit STOP Condition.

In addition, the term progress for about 6 ms after command transmission is for waiting to set data which should be read to data buffer of TC9446FG.

The procedure of read-out of 24 bit data is shown in Figure 13.

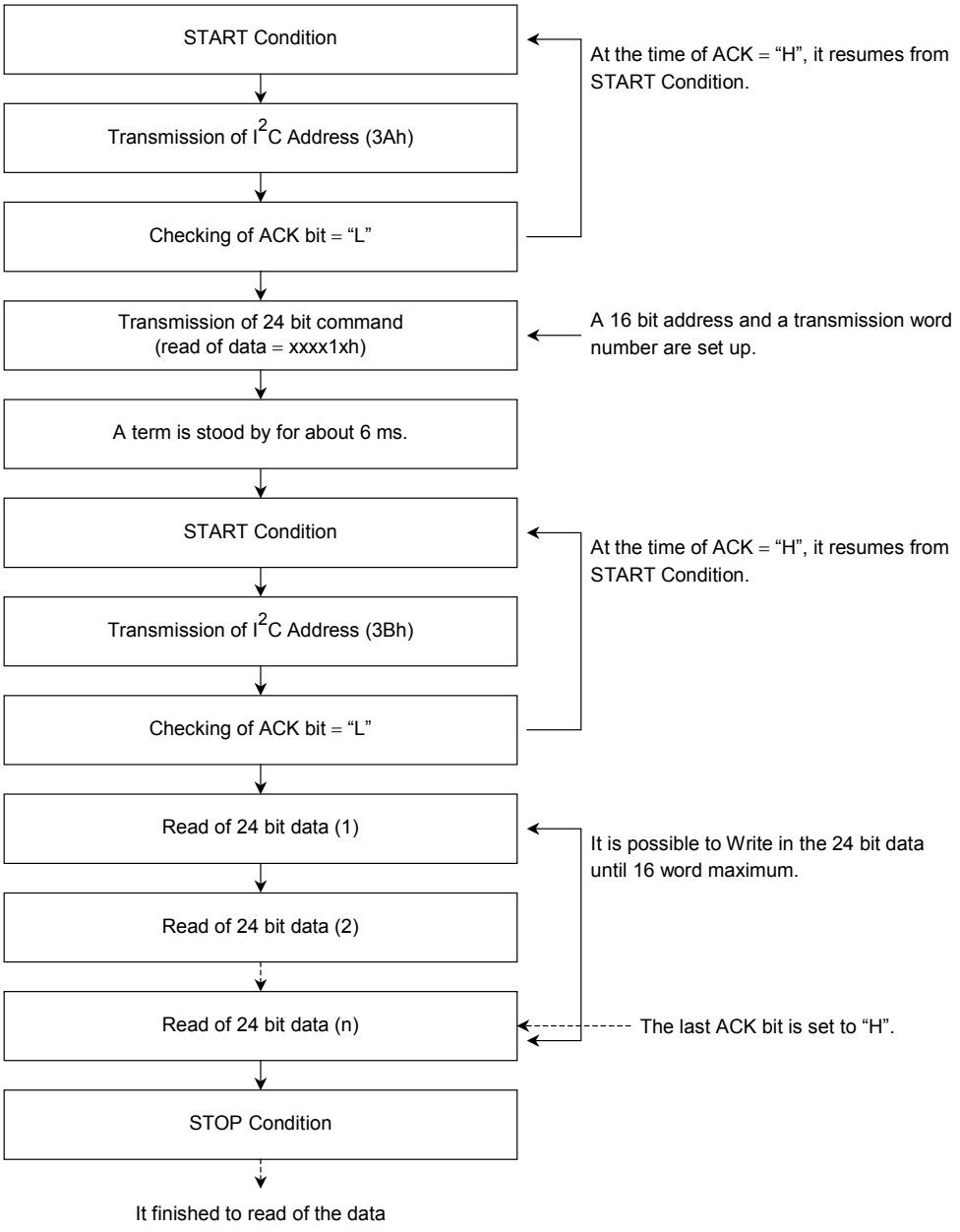


Figure 13 Procedure of Read-Out of 24 Bit Data

4) ON/OFF of soft reset

The case where a program is started after program boot, and in restarting a program, it performs ON/OFF of soft reset. ON/OFF of soft reset are performed by carrying out and transmitting the bit of the soft reset in a 24 bit command to "H" (ON) and "L" (OFF).

Since data with which ON/OFF of soft reset follows a command is not required, STOP Condition is transmitted after 24 bit command transmission.

In addition, in order to return from a incorrect operation state, when turning ON soft reset, it is also possible to transmit a 24 bit command irrespective of the state of ACK bit.

The procedure of ON/OFF of soft reset is shown in Figure 14.

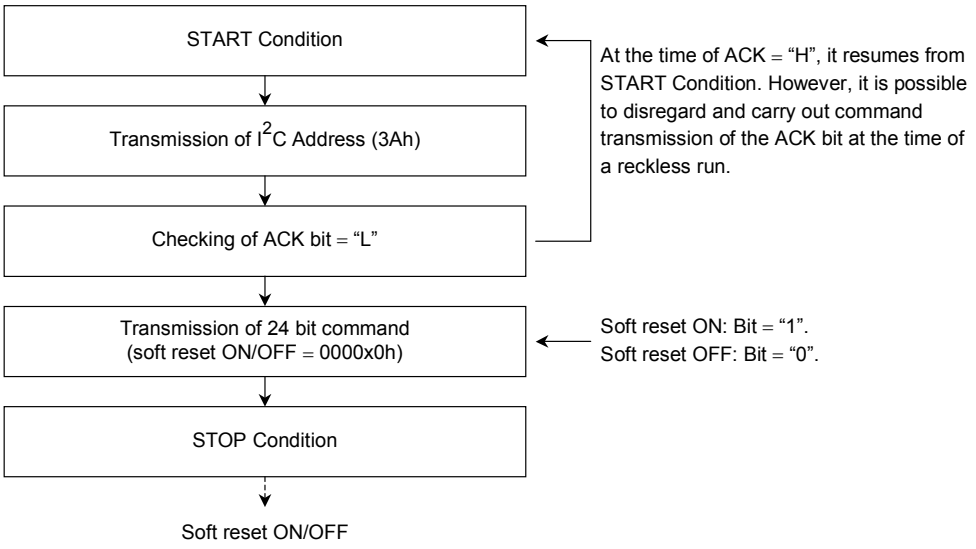


Figure 14 Procedure of ON/OFF of Soft Reset

5) Incorrect operation detection

Incorrect operation detection of the internal program of TC9446FG is judged by the existence of the reaction to the access demand from a MCU. Therefore, R/W of data need to be performed from a MCU to TC9446FG at the interval of about 6 ms or more.

ACK bit is set to "L", when the following access demand opens the interval of about 6 ms or more and is performed, since R/W of data were performed between about 6 ms back to the access demand from a MCU when TC9446FG were operating normally.

However, if TC9446FG become a incorrect operation state, even if it is going to stop receiving the access demand from a MCU, it is going to open the interval of about 6 ms or more and MCU is going to make it access again, it will become a state ACK bit is "H" continued.

A MCU can perform incorrect operation detection by seeing this ACK bit.

That is, since TC9446FG are in a incorrect operation state when it is "H" fixation, even if ACK bit passes about 6 ms or more, ACK bit is disregarded, soft reset is turned ON, and each setup of TC9446FG is performed again.

3. Setting Procedure Until it Starts Decode Program Operation

Setting procedure until it starts operation of the decode program built in TC9446FG is shown below.

First, 10 words program data is transmitted in the program boot mode after release of the power-on reset at the time of a power-supply injection.

However, when there is a program required for others, program data of a maximum of 128 words can be transmitted.

And, if the command of soft reset-off is transmitted, a program will begin to operate and decode will be started by transmitting addresses of the write-in command shown in an attached sheet (the program explanation data) after that 9 words of 0000h-0008h.

Procedure until it starts operation of a decode program to Figure 15 is shown.

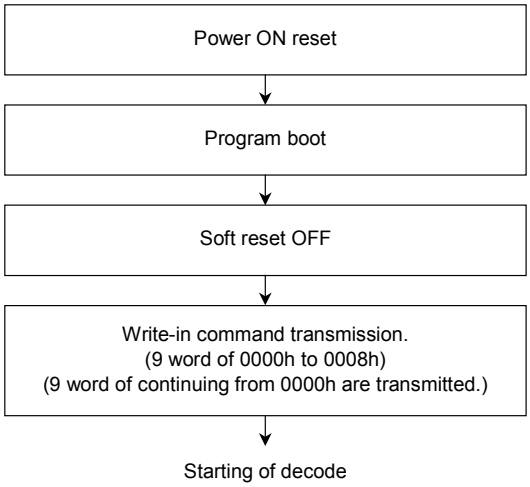


Figure 15 Procedure to Decode Program Operation Start

Note 7: Internal RAM is cleared, in order to muting for output, after transmitting a setup of command 0003h “decode off” in the case of AC-3 decoder program. Please transmit following data after checking that ACK is set to “L” from “H”, since such a case has the time for about 23 ms (maximum) in this processing. If processing of the internal RAM clearance by the “decode off” command is completed, it will return at the waiting time for 1 or less ms.

In addition, according to the kind of decode program, please transmit following data after checking that ACK is set to “L” from “H”, since the waiting time which the data transmission at the time of decode on/off takes differs.

4. Read/Write of Command

Write and a read of command change with decode programs built in.
For details, please refer to program explanation data.

5. Digital Audio Interface (DIR/DIT)

1) A setup of DIR/DIT

The digital reception recovery (DIR) for the audio interfaces and the abnormal-conditions transmission (DIT) based on CEI "IEC958 standard" and the JEITA "CP-1201 standard" are built in. DIR corresponds to the input of 96 kHz sampling (2 channels). Please refer to program explanation data about the various contents of a setting of DIR/DIT.

2) VCO oscillation and PLL

Since VCO oscillation circuit is built in, PLL circuit can consist of connecting an external low path filter simply. VCO oscillation circuit and the example of composition of PLL are shown in Figure 16.

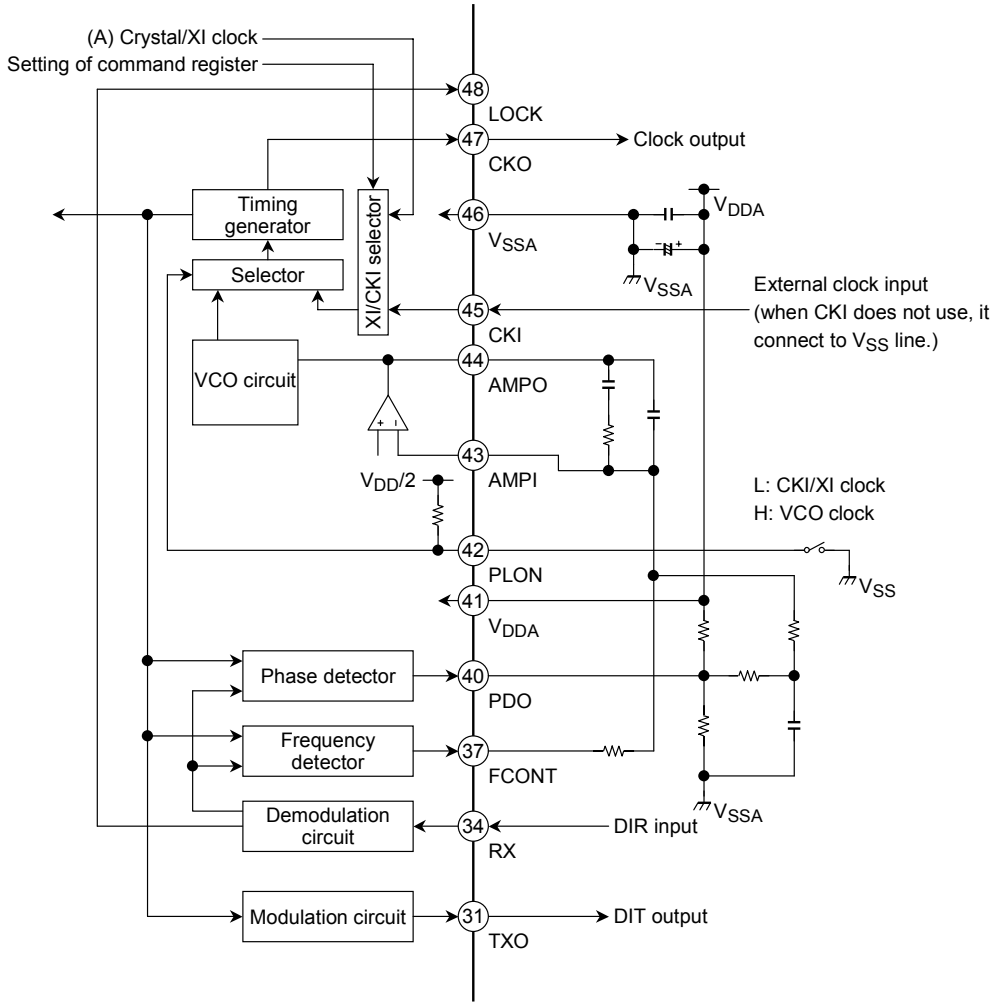


Figure 16 VCO Oscillation Circuit and Example of Composition of PLL

3) DIR input part

When you input a signal into DIR, please be sure to input, as shown in Figure 17 through a signal amplification circuit, a 5 V-3 V conversion circuit, etc.

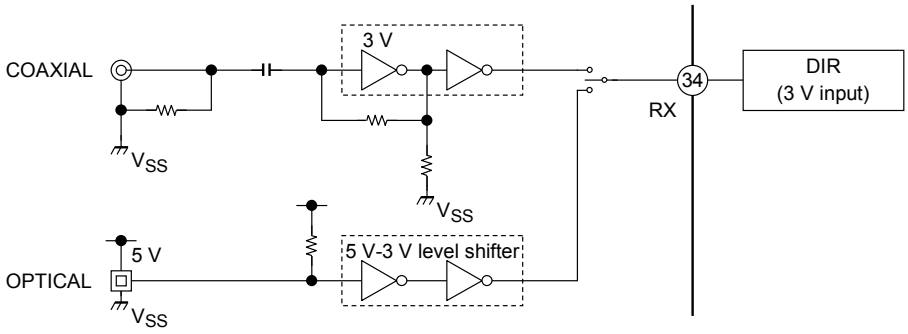


Figure 17 DIR Input Part

4) Lock detection

When VCO circuit locks LOCK terminal and it is operating, "H" level is outputted and "L" level is outputted at the time of the Ann lock. At the time of the Ann lock, latch operation of reception recovery data and channel status is stopped, and it holds last value. If the state of a no error continues the time of the following table, LOCK terminal will be set to "H" level and a reception recovery will be started.

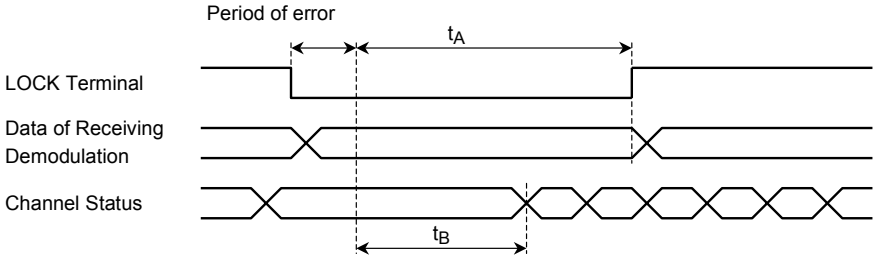


Figure 18 Internal Operation Timing at Time of Error

Table 3 Release Time After the Lock Detection Operation

Sampling Frequency (kHz)	Data of Receiving Demodulation t_A (ms)	Channel Status t_B (ms)
32	384.0	288.0
44.1	278.6	209.0
48	256.0	192.0
96	128.0	96.0

5) Non-inputted detection

When existence of the edge of the input signal from RX terminal is detected and there is no fixed time edge, VCO oscillation operates by free run. Since VCO oscillation frequency and CKO terminal output are set to about 80 MHz, please change it to an external clock automatically by the internal program at the time of less inputting, or choose XI input by setup of command register.

Table 4 Non-Inputted Judgment Time of Input Signal

Sampling Frequency (kHz)	Time of Last Edge (ms)
32	approx. 1000
44.1	approx. 750
48	approx. 700
96	approx. 350

6) Miss lock detection

By comparing the input signal and the oscillation frequency from RX terminal, a Miss lock is detected and the signal for escaping from a miss lock is outputted from FCONT terminal.

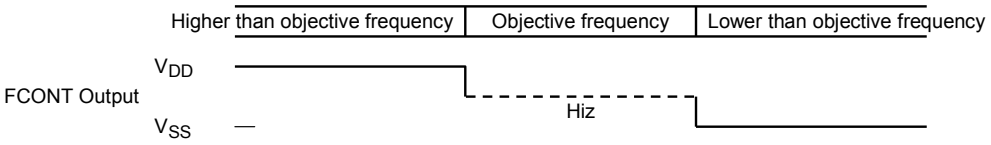


Figure 19 Miss Lock Detection Operation Timing

6. DSP Part Clock Generating Circuit

It is the circuit which generates a clock required in order to operate a decode program. DLL circuit can generate the DLL clock of a crystal oscillation clock.

DLL circuit and a crystal oscillation circuit block are shown in Figure 20.

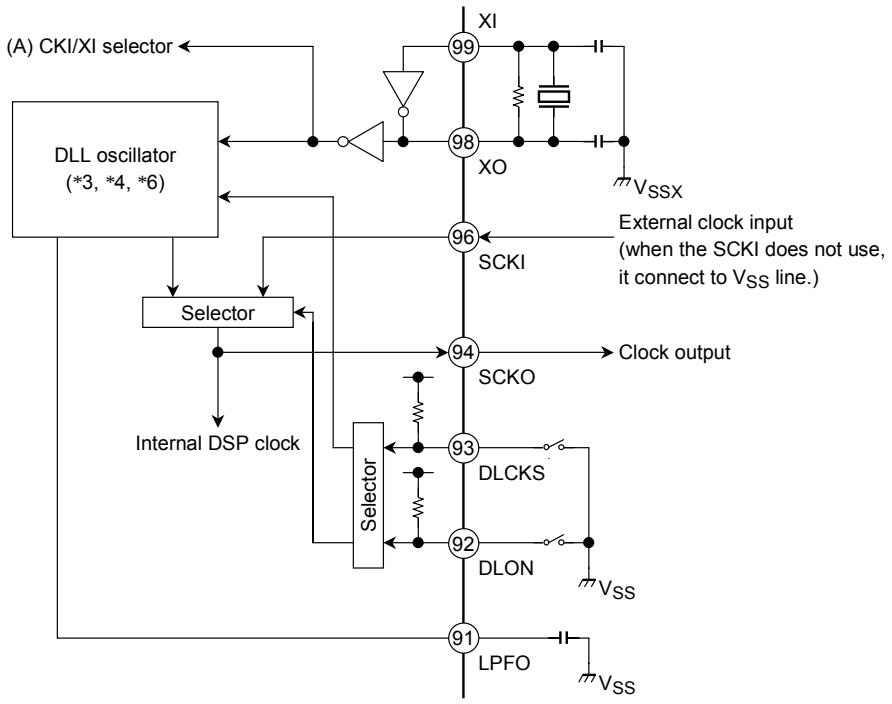


Figure 20 Crystal Oscillation Circuit and DLL Circuit Block

DLL oscillation clock can be chosen with DLCKS terminal and DLON terminal, as shown in Table 5.

Table 5 Setup of DLL Circuit

DLCKS Terminal (93 pin)	DLON Terminal (92 pin)	DLL Oscillation Clock
"L"	"L"	SCKI input (DLL = off)
"L"	"H"	XI input * 4th times
"H"	"L"	XI input * 3rd times
"H"	"H"	XI input * 6th times

When DLCKS terminal and DLON terminal are "L", the external clock input from SCKI terminal is chosen.

An internal clock of operation is a half divided clock of the DLL clock, and processing speed can correspond a maximum of 75 MIPS. The clock outputted from DLL circuit should choose a crystal oscillation clock to be set to less than 150 MHz. The example of DLL clock by the crystal oscillation clock is shown in Table 6.

Table 6 Crystal Oscillation Clock and DLL Clock

Crystal Oscillation Clock	6th Times Clock	4th Times Clock	3rd Times Clock
12.288 MHz (48 kHz*256)	73.728 MHz (36 MIPS operation)	49.152 MHz (24 MIPS operation)	38.864 MHz (18 MIPS operation)
18.432 MHz (48 kHz*384)	110.592 MHz (55 MIPS operation)	73.728 MHz (36 MIPS operation)	55.296 MHz (27 MIPS operation)
24.576 MHz (48 kHz*512)	147.456 MHz (73 MIPS operation)	98.304 MHz (49 MIPS operation)	73.728 MHz (36 MIPS operation)
25.00 MHz (asynchronous)	to 150 MHz (75 MIPS operation)	100.00 MHz (50 MIPS operation)	75.00 MHz (37 MIPS operation)
27.00 MHz (asynchronous)	Not available	108.00 MHz (54 MIPS operation)	81.00 MHz (40 MIPS operation)
30.0 MHz (asynchronous)	Not available	to 120 MHz (60 MIPS operation)	90.00 MHz (45 MIPS operation)
36.864 MHz (48 kHz*768)	Not available	Not available	110.592 MHz (55 MIPS operation)

Note 8: Crystal oscillation clock is as asynchronous as the system clocks (AD converter, DA converter, etc.) of external LSI. A case needs to input the clock oscillated externally into CKI terminal, and needs to synchronize with them.

7. Flag Input (FI0-FI3 terminal)

It is used when inputting a flag from a MCU. However, a function changes with built-in programs. FI0 to FI3 terminal should fix each terminal to "H", or since pull-up resistance is built in, when not being specified by the program, please it be open and be used for it.

8. Interruption Input (IRQ terminal)

It is used when interrupting and inputting from a MCU. However, operation changes with built-in programs. IRQ terminal should fix a terminal to "L", or since pull down resistance is built in, when not being specified by the program, please it be open and be used for it.

9. General-Purpose Output Terminal (PO0-PO7 terminal)

It can be used when carrying out logic control of the case where it is used as an interruption output to the flag and the MCU for detection of internal operation, or the external LSI. However, the function and operation of a terminal change with built-in programs. Since PO0-PO7 terminal contains pull-up resistance, when not being specified by the program, please carry out and use each output terminal for opening.

At the time of a power-supply injection, the output of a general-purpose output terminal becomes unfixed. "L" level will be outputted if it initializes with a reset terminal.

10. External SRAM Connection

It can be used by the ability of able to connect external SRAM to processing of data tables, such as coefficient data, or data delay.

The function of the terminal for external SRAM control is shown in Table 7. Moreover, the example of connection of external SRAM is shown in Figure 21.

Table 7 Function of Terminal for External SRAM Control

Terminal Name	Functions
$\overline{WR}$ terminal	Write signal output terminal for external SRAM
$\overline{OE}$ terminal	Output enable signal output terminal for external SRAM
$\overline{CE}$ terminal	Chip enable signal output terminal for external SRAM
IO0 to IO7 terminal	Data input/output terminal for external SRAM (8 bit I/O) It is 3rd times accessing at 24 bit I/O.
AD0 to AD16 terminal	Address output terminal for external SRAM It can access to address 00000h to 20000h.

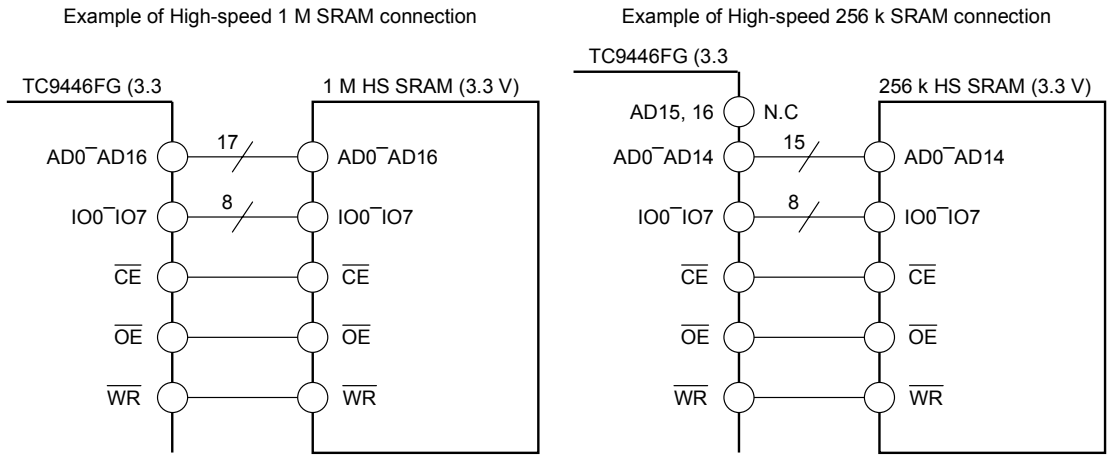


Figure 21 Example of Connection of External SRAM

11. Serial Data Input-and-Output Terminal

Since two terminals (SDI0 and SDI1 terminal) are prepared for an audio serial data input and four terminals (SDO0-SDO3 terminal) are prepared for an output, the connection with external AD/DA converter LSI is easy.

Although an input terminal (SDI0, SDI1, LRCKA, BCKA, LRCKB, and BCKB terminal) can be inputted by 3-5 V, an output terminal (SDO0-3, LRCKOA, BCKOA, LRCKOB, and BCKOB terminal) is outputted by 3 V. Therefore, when the input terminal of external LSI does not correspond to TTL level input, please carry out level conversion using a level shifter circuit etc.

Figure 22 the example of connection of AD/DA converter is shown. However, when an input-and-output signal has the same sampling frequency, it is restricted. Since a sampling frequency differs when the signal of 2 fs is inputted and it outputs a signal by 1 fs, the connection method needs to be changed.

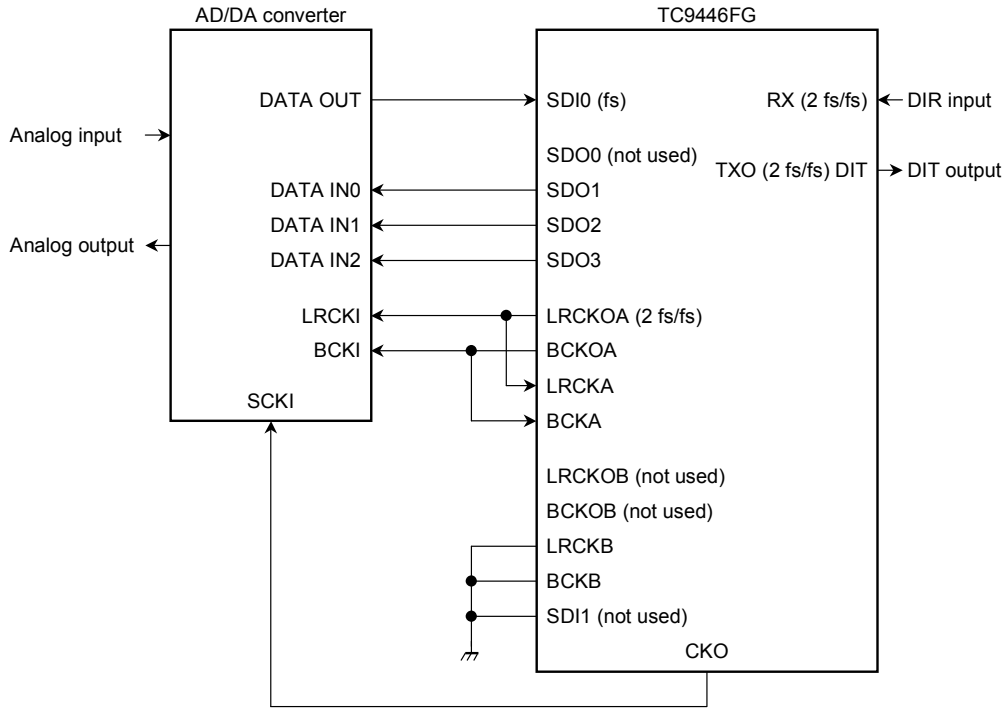
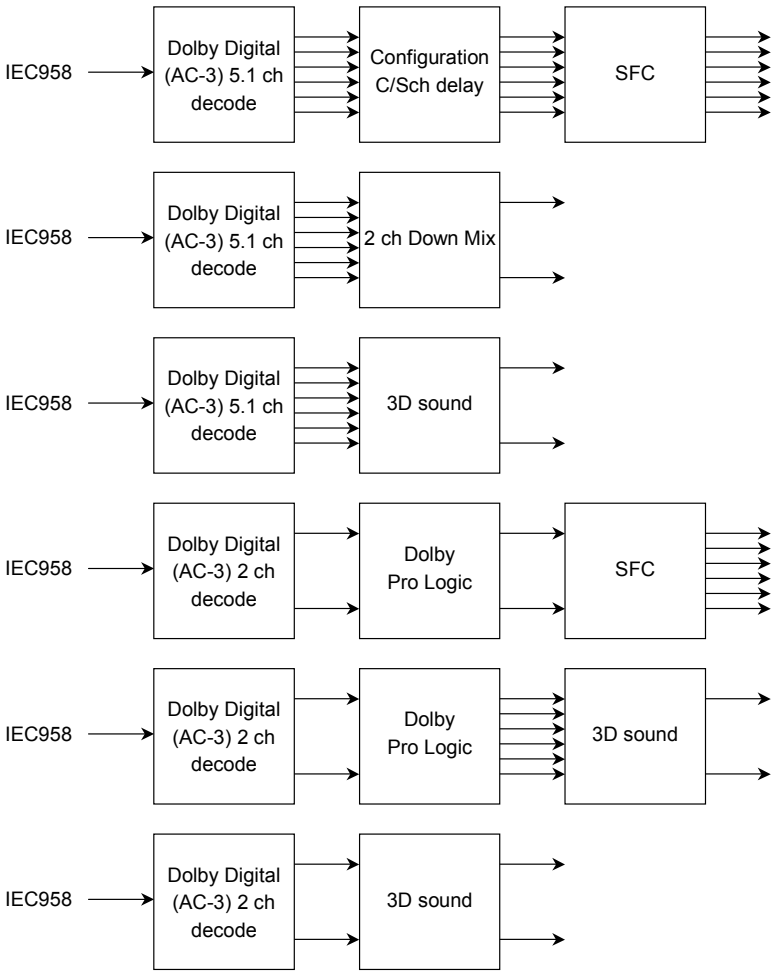


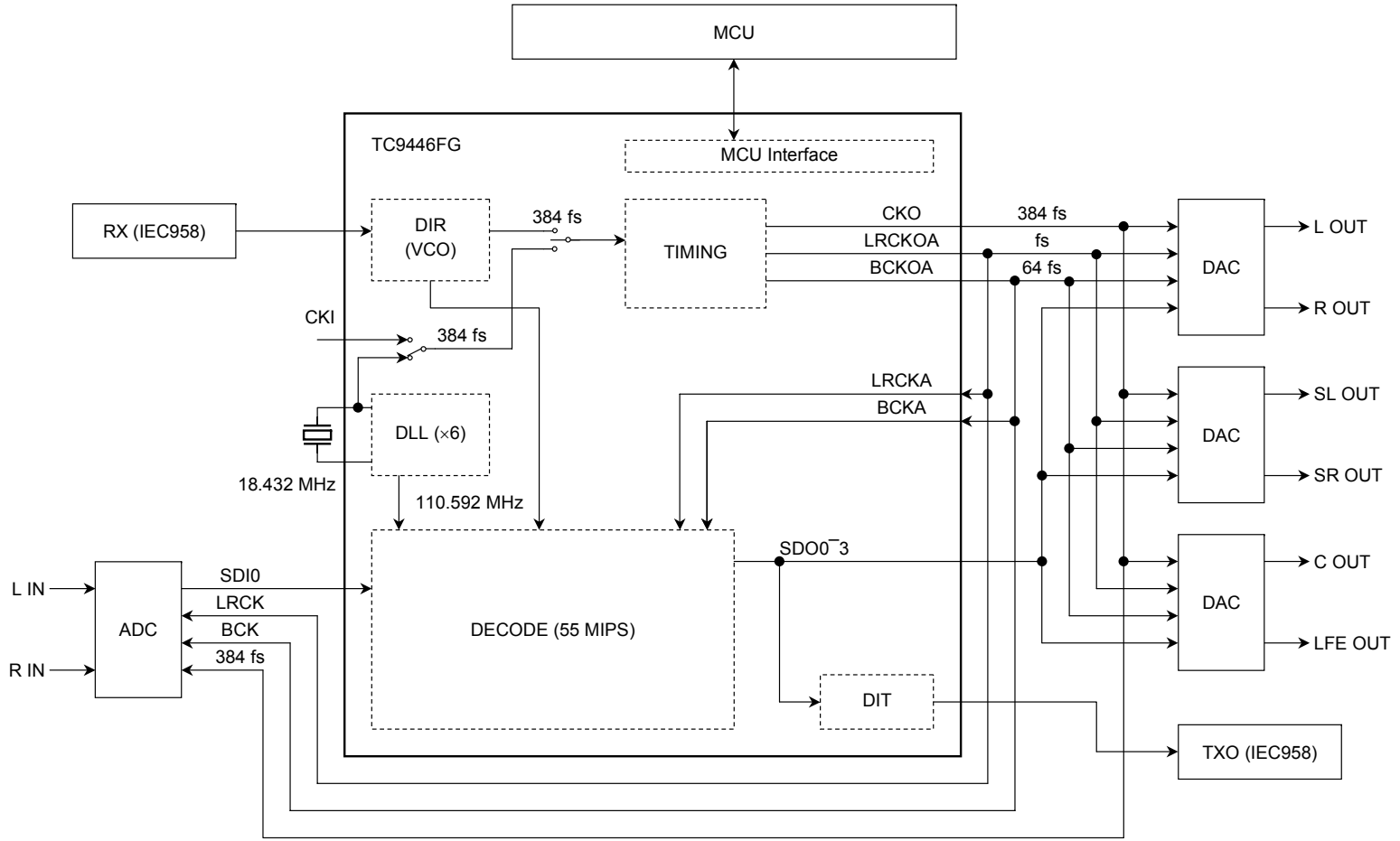
Figure 22 Example of AD/DA Converter Connection

12. Example of Processing of Dolby Digital (AC-3) (Note 9) Decoder

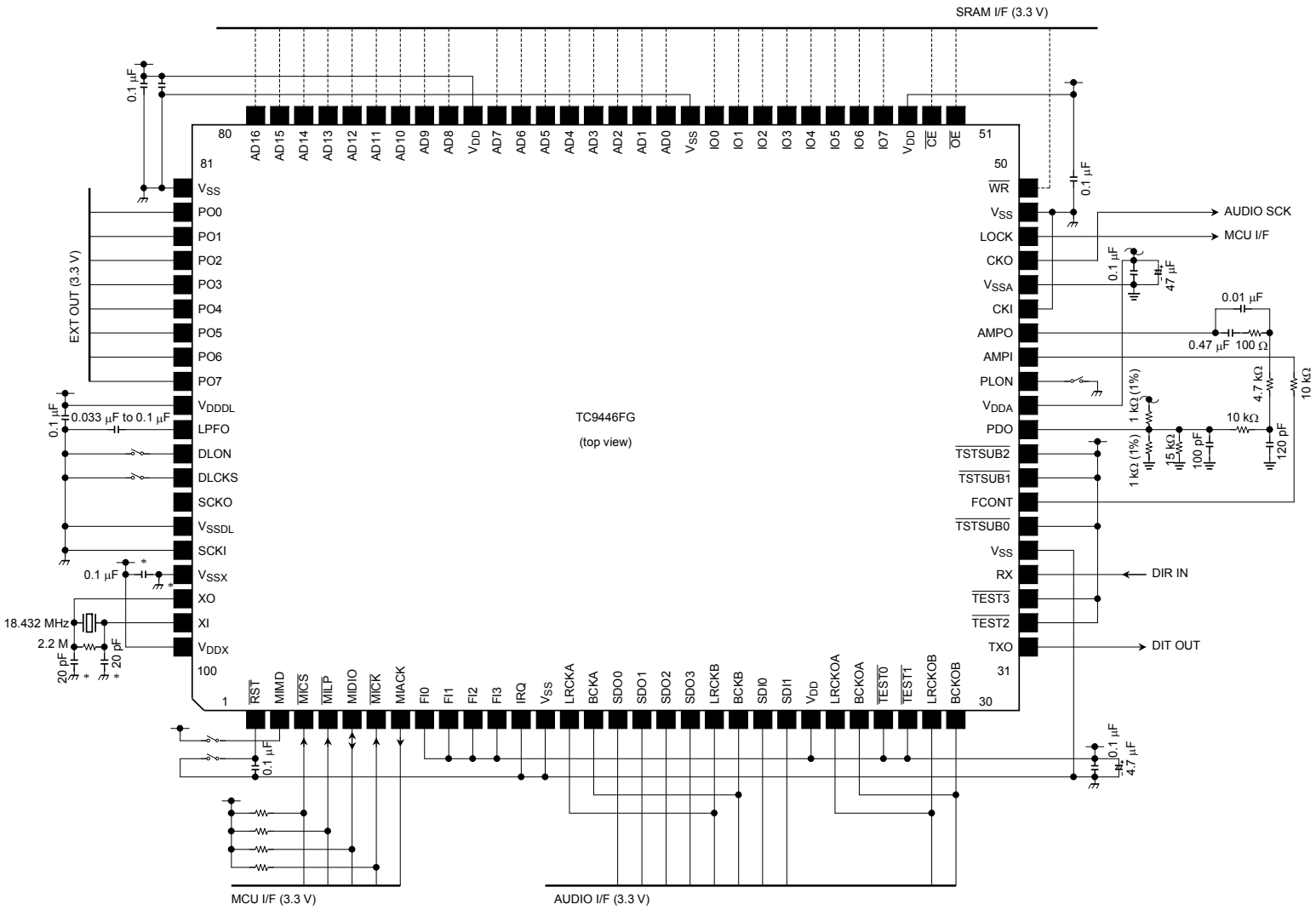


Note 9: “Dolby”,”Pro Logic”, and the double-D symbol are trademarks of Dolby Laboratories.

13. Example of System Application



14. Example of Application Circuit



V_{DDX} and V_{SSX} line which the *-mark attached should dissociate and connect with other V_{DD} and V_{SS} line.

Note 10: According to the diving noise of outside which receives a power supply line and GND line, etc., or jitters of the input signal, and other operating conditions (power-supply voltage, temperature conditions, etc.), the lock of PLL may separate from this product and it may become unstable.
Please determine constant value according to the characteristic of a circuit in the case of use of this product. In addition, the constant value in the example of an application circuit is for explaining operation of this product, and application, and does not offer a guarantee of operation.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to +4.0	V
Input voltage-1	V_{IN1}	−0.3 to V_{DD} + 0.3	V
Input voltage-2	V_{IN2}	−0.3 to V_{DD} + 3.0 (Note 11)	V
Power dissipation	P_D	1500	mW
Operating temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note 11: $\overline{\text{MICS}}$, $\overline{\text{MILP}}$, MIDIO, $\overline{\text{MICK}}$, LRCKA, BCKA, LRCKB, BCKB, SDI0, SDI1, RX (schmitt input terminals)

Electrical Characteristics
(unless otherwise specified, Ta = 25°C, V_{DD} = V_{DDX} = V_{DDA} = V_{DDDL} = 3.3 V)

DC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage-1	V_{DD1}	—	Ta = −40 to +85°C, $f_{opr} \leqq$ 140 MHz	3.0	3.3	3.6	V
Operating power supply voltage-2	V_{DD2}	—	Ta = −40 to +85°C, f_{opr} > 140 MHz	3.1	3.3	3.6	V
Operating frequency range-1	f_{opr1}	—	DLL oscillation frequency (4^{th} times)	—	—	120	MHz
Operating frequency range-2	f_{opr2}	—	DLL oscillation frequency (6^{th} times), At f_{opr} > 140 MHz, V_{DD} = 3.1 to 3.6 V.	—	—	150	MHz
Power supply current	I_{DD}	—	f_{opr} = 150 MHz 75 MIPS operating	—	110	160	mA

Clock Terminals

Input voltage	"H" level	V_{IH1}	—	XI pin, (Note 14)		2.5	—	—	V
	"L" level	V_{IL1}	—			—	—	0.8	
Output current	"H" level	I_{OH1}	—	V_{OH} = 2.8 V	XO pin	—	—	−8	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.5 V		15	—	—	

Note 14: CKI, SCKI (CMOS input terminals)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input Terminals									
Input voltage	"H" level	V_{IH2}	—	(Note 11), (Note 12), (Note 13), (Note 15)		2.8	—	—	V
	"L" level	V_{IL2}	—			—	—	0.5	
Input leakage current	"H" level	I_{IH}	—	$V_{IN} = V_{DD}$	(Note 11), (Note 12), (Note 15), AMPI pin	—	—	±10	μA
	"L" level	I_{IL}	—	$V_{IN} = 0$ V	(Note 11), (Note 13) AMPI pin	—	—	±10	
Output Terminals									
Output current	"H" level	I_{OH2}	—	$V_{OH} = 2.8$ V	(Note 15), (Note 16), (Note 17)	—	—	−8	mA
	"L" level	I_{OL2}	—	$V_{OL} = 0.5$ V		15	—	—	
Output current	"H" level	I_{OH3}	—	$V_{OH} = 2.8$ V	AMPO pin	—	—	−1	mA
	"L" level	I_{OL3}	—	$V_{OL} = 0.5$ V		1	—	—	
3-State Output Terminals									
Output current	"H" level	I_{OH4}	—	$V_{OH} = 2.8$ V	FCONT, P_D pins	—	—	−8	mA
	"L" level	I_{OL4}	—	$V_{OL} = 0.5$ V		15	—	—	
Output off leakage current		I_{OZ4}	—	$V_{OH} = V_{DD}$, $V_{OL} = 0$ V		—	—	±10	μA
Open-Drain Output Terminals									
Output current	"L" level	I_{OL6}	—	$V_{OL} = 0.5$ V	MIDIO pin	20	—	—	mA
Output off leakage current		I_{OL6}	—	$V_{OH} = V_{DD}$, $V_{OL} = 0$ V		—	—	±10	μA
Pull-Up Resistor and Pull-Down Resistor Built-In Terminals									
Pull-up resistor		Rup	—	$V_{IN} = 0$ V	(Note 12), (Note 15), (Note 16)	45	—	75	kΩ
Pull-down resistor		Rdwn	—	$V_{IN} = 3.3$ V	(Note 13)	55	—	85	kΩ

Note 11: $\overline{\text{MICS}}$, $\overline{\text{MILP}}$, MIDIO, $\overline{\text{MICK}}$, LRCKA, BCKA, LRCKB, BCKB, SDI0, SDI1, RX (schmitt input terminals)

Note 12: $\overline{\text{RST}}$, $\overline{\text{TSTSUB0}}$ to 2, $\overline{\text{TEST0}}$ to 3, PLON, DLON, DLCKS, FI0 to 3 (schmitt input terminals with pull-up resistor)

Note 13: MIMD, IRQ (schmitt input terminals with pull-down resistor)

Note 15: IO0 to 7 (input/output terminals with pull-up resistor)

Note 16: PO0 to 7, AD0 to 16, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CE}}$ (output terminals with pull-up resistor)

Note 17: MIACK, SDO0 to 3, LRCKOA, BCKOA, LRCKOB, BCKOB, TXO, CKO, SCKO, LOCK (output terminals)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit

AC Characteristics (1) Timing

Clock Input Terminals (XI)

Clock frequency	f_{XI}	—	DLL oscillation circuit (4th times)	—	—	30	MHz
Clock duty	f_{DTY}	—	—	40	50	60	%

Clock Input Terminals (CKI)

Clock frequency	f_{CI}	—	384 fs, fs = 96 kHz	—	—	37	MHz
Clock “H” duration	t_{CIH}	—	—	13	—	—	ns
Clock “L” duration	t_{CIL}	—	—	13	—	—	ns

Clock Input Terminals (SCKI)

Clock frequency	f_{SI}	—	75 MIPS operating	—	—	150	MHz
Clock “H” duration	t_{SIH}	—	—	3.3	—	—	ns
Clock “L” duration	t_{SIL}	—	—	3.3	—	—	ns

Reset Terminal ($\overline{RST}$)

Stand-by time	t_{RRS}	—	—	10	—	—	ms
Reset pulse width	t_{WRS}	—	—	10	—	—	μs

Audio Serial Interface
(LRCKA to B, BCKA to B, LRCKOA to B, BCKOA to B, SDI0 to 1, SDO0 to 3)

LRCK setup time	t_{LBS}	—	C_L = 30 pF, fs = 96 kHz	20	—	—	ns
LRCK hold time	t_{LBH}	—	C_L = 30 pF, fs = 96 kHz	–60	—	60	ns
SDI setup time	t_{SDI}	—	C_L = 30 pF, fs = 96 kHz	20	—	—	ns
SDI hold time	t_{HDI}	—	C_L = 30 pF, fs = 96 kHz	20	—	—	ns
BCK clock cycle	t_{BCK}	—	C_L = 30 pF, fs = 96 kHz	160	—	—	ns
BCK clock “H” duration	t_{BCH}	—	C_L = 30 pF, fs = 96 kHz	80	—	—	ns
BCK clock “L” duration	t_{BCL}	—	C_L = 30 pF, fs = 96 kHz	80	—	—	ns
SDO output delay time-1	t_{DO1}	—	C_L = 30 pF, fs = 96 kHz	—	—	10	ns
SDO output delay time-2	t_{DO2}	—	C_L = 30 pF, fs = 96 kHz	—	—	10	ns
LRCK output delay time	t_{DCLR}	—	C_L = 30 pF, fs = 96 kHz	—	—	10	ns

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit

Micro Controller Interface

Serial Transmission Mode ($\overline{\text{MICS}}$, $\overline{\text{MICK}}$, MIDIO, $\overline{\text{MILP}}$, MIACK)

Stand-by time	t_{STB}	—	—	25	—	—	ms
MICS fall-MICK rise setup time	t_1	—	—	0.5	—	—	μs
MIACK fall-MICK rise setup time	t_2	—	—	0.5	—	—	μs
MICK clock cycle	t_3	—	—	1.0	—	—	μs
MICK “L” duration	t_4	—	—	0.5	—	—	μs
MICK “H” duration	t_5	—	—	0.5	—	—	μs
MICK rise-MILP fall setup time	t_6	—	—	0.5	—	—	μs
MILP “duration	t_7	—	—	0.5	—	—	μs
MIDIO input data setup time	t_8	—	—	0.5	—	—	μs
MIDIO input data hold time	t_9	—	—	0.5	—	—	μs
MIDIO output data delay time	t_{10}	—	—	—	—	0.5	μs
MICS “H” duration	t_{11}	—	—	0.5	—	—	μs
MIACK output delay time	t_{12}	—	—	—	—	0.1	μs
MILP rise-MICS rise setup time	t_{13}	—	—	0.5	—	—	μs

Note 18: “H” duration of MIACK signal depends on firmware of TC9446FG.

I^2C Mode ($\overline{\text{MICK}}$, MIDIO)

MICK clock frequency	f_{IFCK}	—	C_L = 400 pF	0	—	400	kHz
MICK “H” duration	t_H	—	C_L = 400 pF	0.6	—	—	μs
MICK “L” duration	t_L	—	C_L = 400 pF	1.3	—	—	μs
Data setup time	t_{DS}	—	C_L = 400 pF	0.1	—	—	μs
Data hold time	t_{DH}	—	C_L = 400 pF	0	—	—	μs
Transmission start condition hold time	t_{SCH}	—	C_L = 400 pF	0.6	—	—	μs
Repeat transmission start condition setup time	t_{SCS}	—	C_L = 400 pF	0.6	—	—	μs
Transmission end condition setup time	t_{ECS}	—	C_L = 400 pF	0.6	—	—	μs
Data transmission interval	t_{BUF}	—	C_L = 400 pF	1.3	—	—	μs
I^2C rise time	t_R	—	C_L = 400 pF	—	—	0.1	μs
I^2C fall time	t_F	—	C_L = 400 pF	0.5	—	—	μs

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit

External RAM Memory Interface (WR, OE, CE, IO0 to 7, AD0 to 16)

(1) Memory read input/output

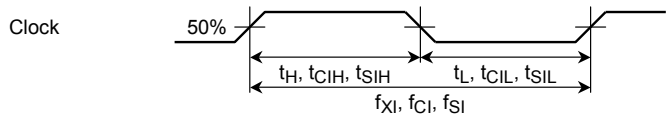
Address setup time	t_{ASR}	—	C_L = 30 pF, 75 MIPS operating	—	14	—	ns
Address hole time	t_{AHR}	—	C_L = 30 pF, 75 MIPS operating	—	0	—	ns
Pre-charge time	t_{PCR}	—	C_L = 30 pF, 75 MIPS operating	14	—	—	ns
Read cycle width	t_{RC}	—	C_L = 30 pF, 75 MIPS operating	27	—	—	ns
Until read end from chip select	t_{CR}	—	C_L = 30 pF, 75 MIPS operating 8 bit, one time access	27	—	—	ns
			C_L = 30 pF, 75 MIPS operating 16 bit, two times access	54	—	—	
			C_L = 30 pF, 75 MIPS operating 24 bit, three times access	80	—	—	
OE access time of external SRAM	t_{OE}	—	C_L = 30 pF, 75 MIPS operating	—	—	15	ns
CE access time of external SRAM	t_{CO}	—	C_L = 30 pF, 75 MIPS operating	—	—	15	ns
Output data hold time of external SRAM	t_{OH}	—	C_L = 30 pF, 75 MIPS operating	—	0	—	ns
Address access time of external SRAM	t_{ACC}	—	C_L = 30 pF, 75 MIPS operating	—	—	15	ns
CE disable time of external SRAM	t_{COD}	—	C_L = 30 pF, 75 MIPS operating	—	—	14	ns

(2) Memory write output

Address setup time	t_{ASW}	—	C_L = 30 pF, 75 MIPS operating	—	14	—	ns
$\overline{WR}$ pulse width	t_{WP}	—	C_L = 30 pF, 75 MIPS operating	17	—	—	ns
Address hold time	t_{AHW}	—	C_L = 30 pF, 75 MIPS operating	—	0	—	ns
Pre-charge time	t_{PCW}	—	C_L = 30 pF, 75 MIPS operating	14	—	—	ns
Write cycle width	t_{WC}	—	C_L = 30 pF, 75 MIPS operating	27	—	—	ns
Until write end from chip select	t_{CW}	—	C_L = 30 pF, 75 MIPS operating 8 bit, one time access	27	—	—	ns
			C_L = 30 pF, 75 MIPS operating 16 bit, two times access	54	—	—	
			C_L = 30 pF, 75 MIPS operating 24 bit, three times access	80	—	—	
Output data setup time	t_{DS}	—	C_L = 30 pF, 75 MIPS operating	—	23	—	ns
Output data hold time	t_{DH}	—	C_L = 30 pF, 75 MIPS operating	—	4	—	ns
OE setup time	t_{OES}	—	C_L = 30 pF, 75 MIPS operating	—	0	—	ns
OE hold time	t_{OEH}	—	C_L = 30 pF, 75 MIPS operating	—	0	—	ns

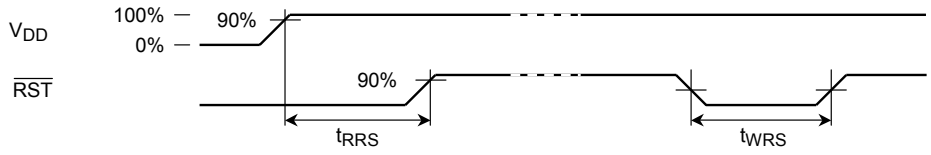
AC Characteristics Measurement Points

(1) Clock terminal (XI, CKI, SCKI)

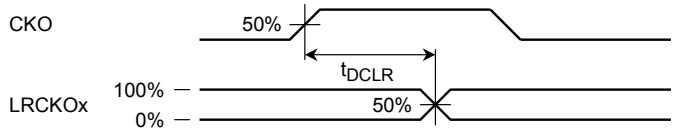


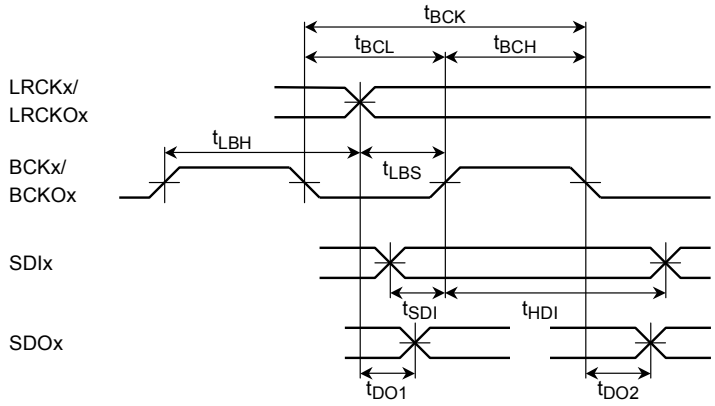
Duty cycle (f_{DTY}) = $t_H/(t_L + t_H) \times 100$ (%)

(2) Reset



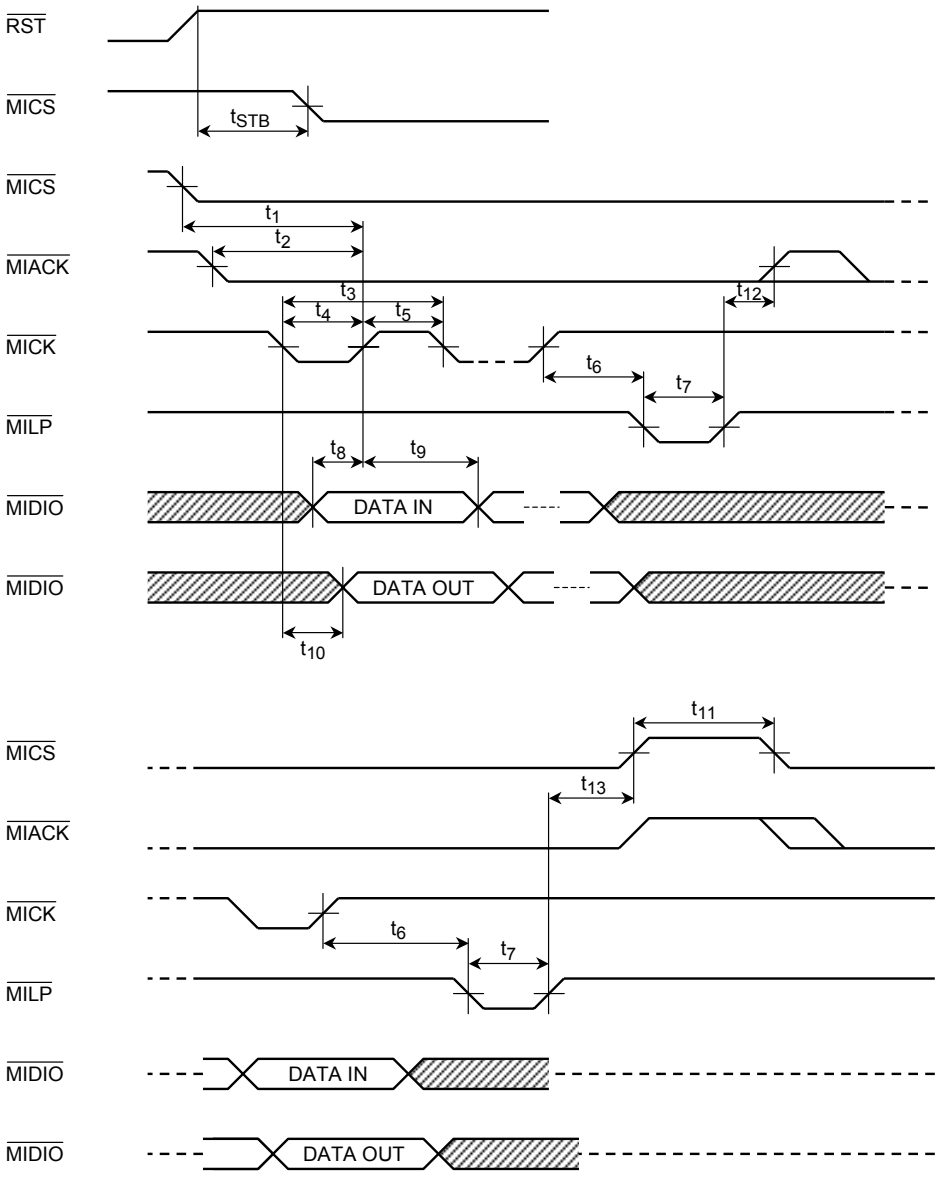
(3) Audio serial interface (LRCKx, BCKx, SDIx, LRCKOx, BCKOx, SDOx, CKO)



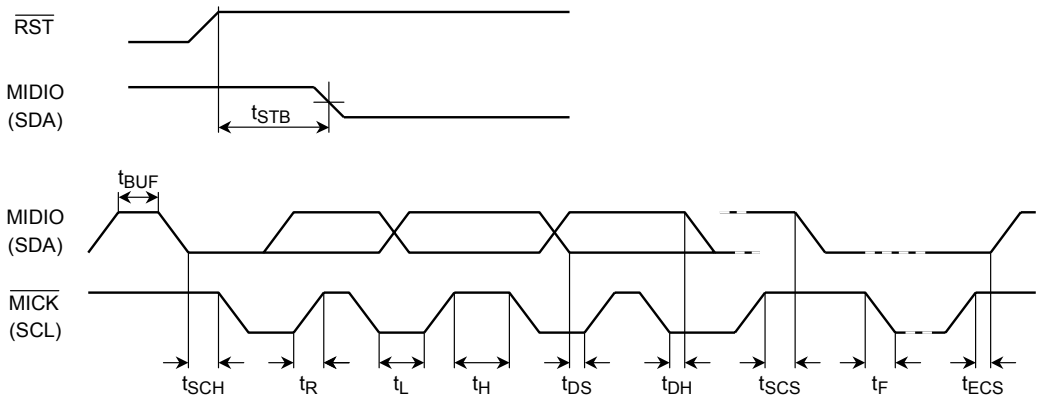


(4) Micro controller interface

(4-1) Serial transmission interface mode ($\overline{\text{MICS}}$, $\overline{\text{MICK}}$, MIDIO, $\overline{\text{MILP}}$, $\overline{\text{MIACK}}$)

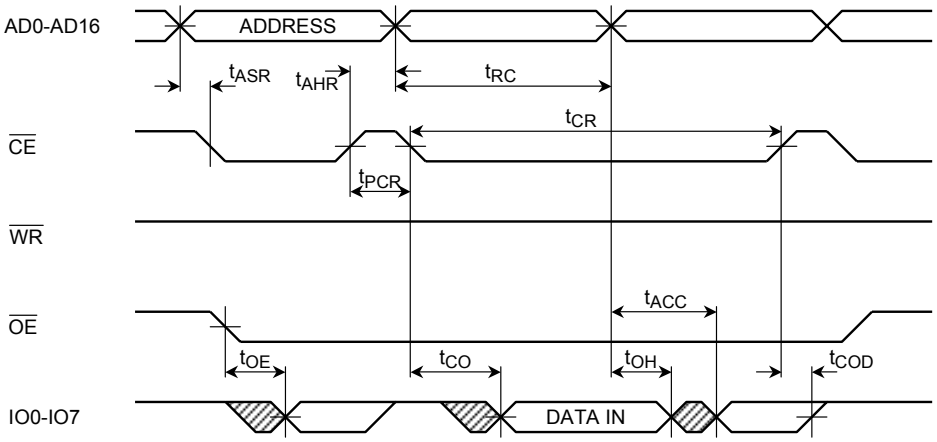


(4-2) I^2C mode ($\overline{MICK}$, MIDIO)

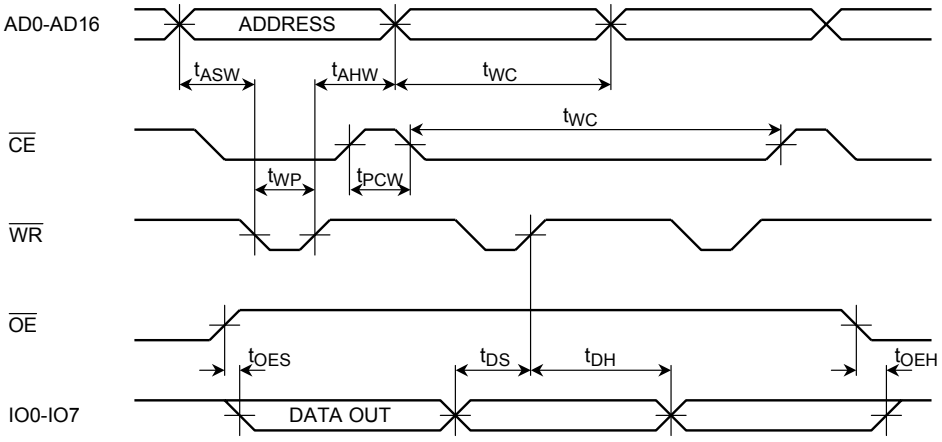


(5) External RAM memory interface

(5-1) READ cycle timing

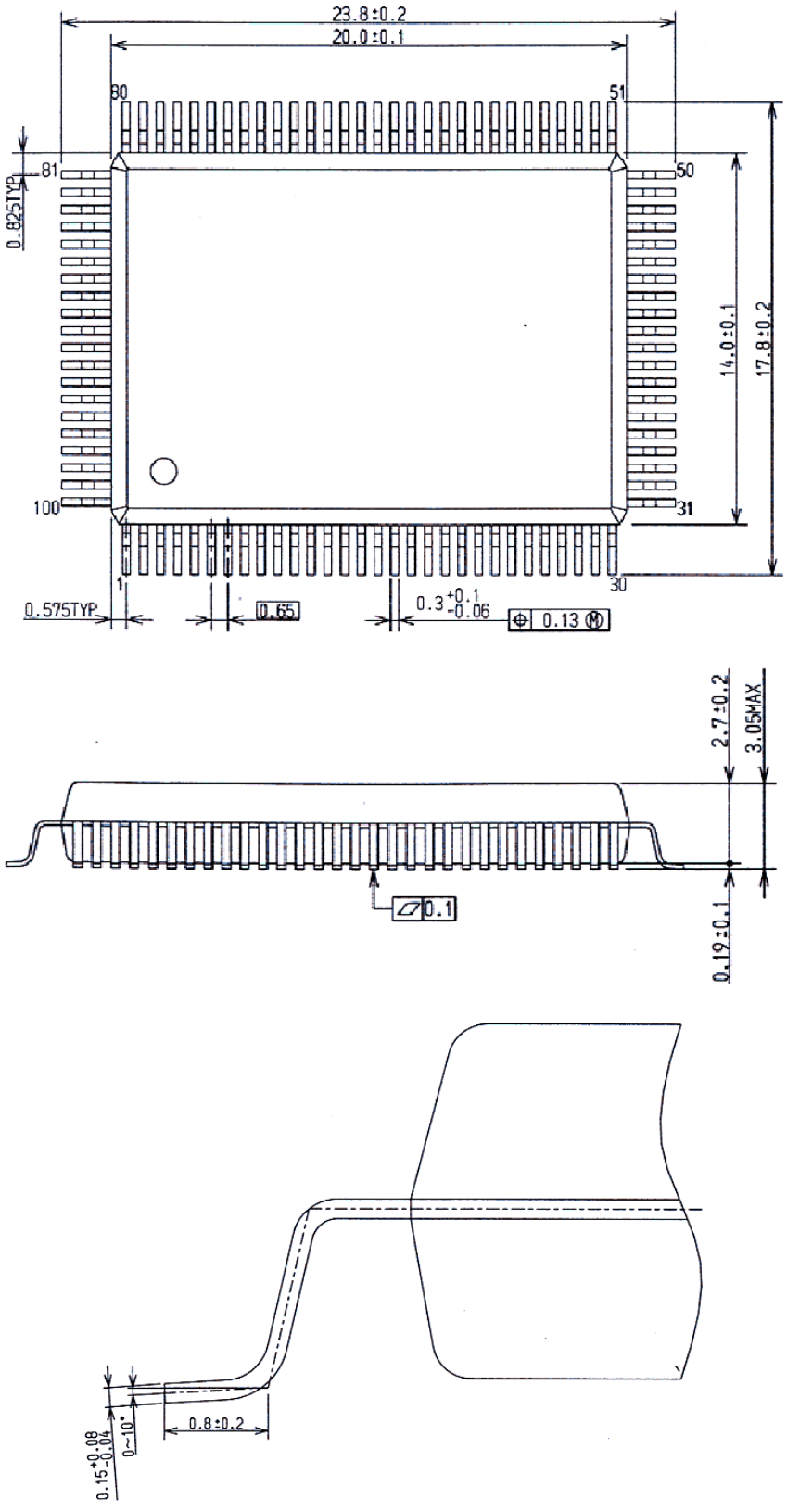


(5-2) WRITE cycle timing



Package Dimensions

P-QFP100-1420-0.65Q Unit : mm



(Note) Palladium plate

Weight: 1.57 g (typ.)

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