

C167CR

C167SR

16-Bit Single-Chip Microcontroller

16bit

Microcontrollers



Never stop thinking.

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C167CR

C167SR

16-Bit Single-Chip Microcontroller

Microcontrollers



Never stop thinking.

16-Bit Single-Chip Microcontroller C166 Family

C167CR/C167SR

C167CR/C167SR

- High Performance 16-bit CPU with 4-Stage Pipeline
 - 80/60 ns Instruction Cycle Time at 25/33 MHz CPU Clock
 - 400/303 ns Multiplication (16×16 bit), 800/606 ns Division (32 / 16 bit)
 - Enhanced Boolean Bit Manipulation Facilities
 - Additional Instructions to Support HLL and Operating Systems
 - Register-Based Design with Multiple Variable Register Banks
 - Single-Cycle Context Switching Support
 - 16 MBytes Total Linear Address Space for Code and Data
 - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40/30 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
 - 2 KBytes On-Chip Internal RAM (IRAM)
 - 2 KBytes On-Chip Extension RAM (XRAM)
 - 128/32 KBytes On-Chip Mask ROM
- On-Chip Peripheral Modules
 - 16-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 μ s
 - Two 16-Channel Capture/Compare Units
 - 4-Channel PWM Unit
 - Two Multi-Functional General Purpose Timer Units with 5 Timers
 - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
 - On-Chip CAN Interface (Rev. 2.0B active) with 15 Message Objects (Full CAN / Basic CAN)
- Up to 16 MBytes External Address Space for Code and Data
 - Programmable External Bus Characteristics for Different Address Ranges
 - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
 - Five Programmable Chip-Select Signals
 - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis

- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C167CR Derivative Synopsis

Derivative ¹⁾	Program Memory	XRAM	CAN Interface
SAK-C167SR-LM SAB-C167SR-LM SAK-C167SR-L33M SAB-C167SR-L33M	---	2 KByte	---
SAK-C167CR-LM SAF-C167CR-LM SAB-C167CR-LM SAK-C167CR-L33M SAB-C167CR-L33M	---	2 KByte	CAN1
SAK-C167CR-4RM SAB-C167CR-4RM SAK-C167CR-4R33M SAB-C167CR-4R33M	32 KByte ROM	2 KByte	CAN1
SAK-C167CR-16RM SAK-C167CR-16R33M	128 KByte ROM	2 KByte	CAN1

¹⁾ This Data Sheet is valid for devices manufactured in 0.5 μm technology, i.e. devices starting with and including design step GA(-T)6.

For simplicity all versions are referred to by the term **C167CR** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CR please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C167CR derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 16.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

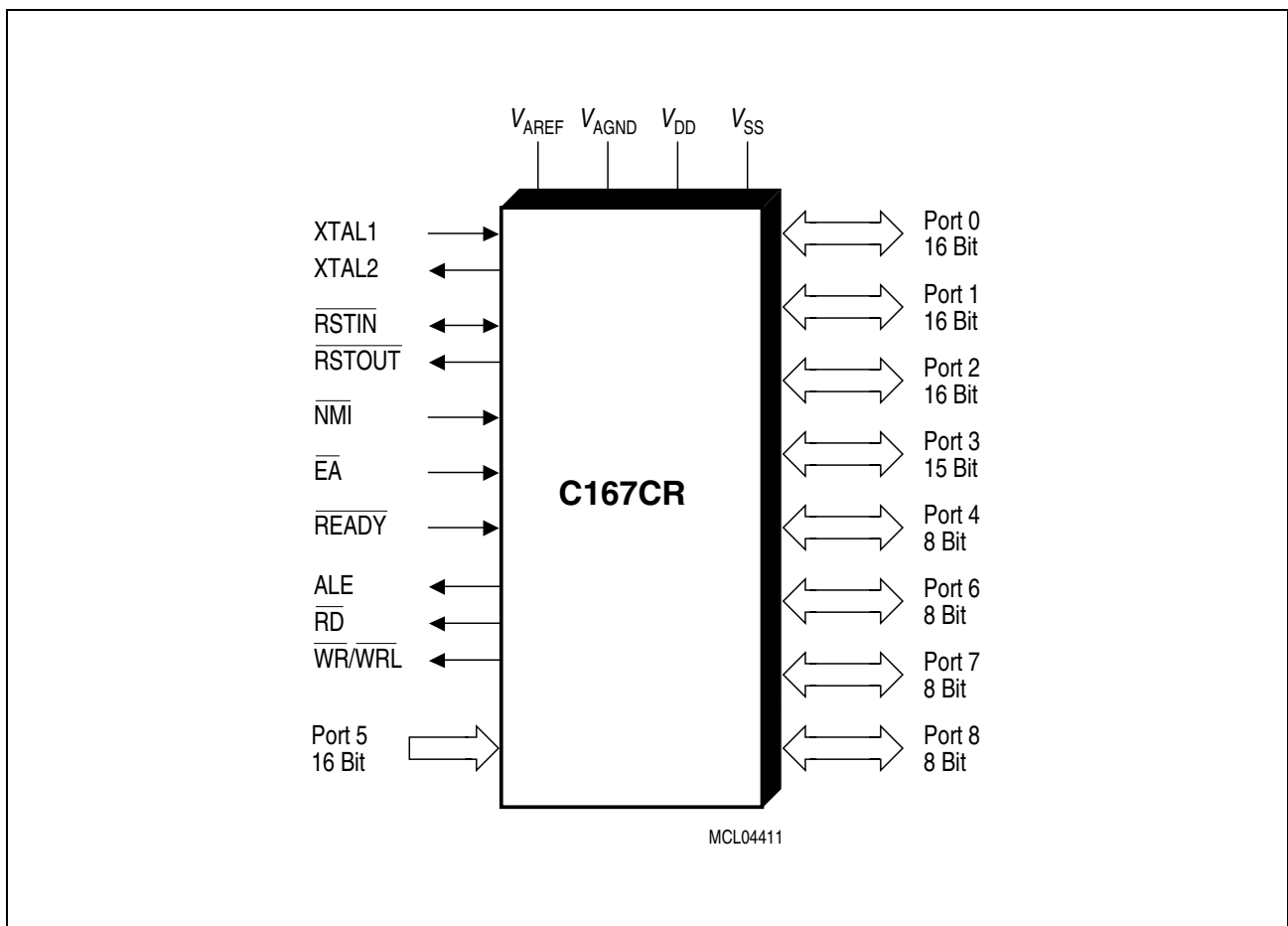


Figure 1 **Logic Symbol**

Pin Configuration
(top view)

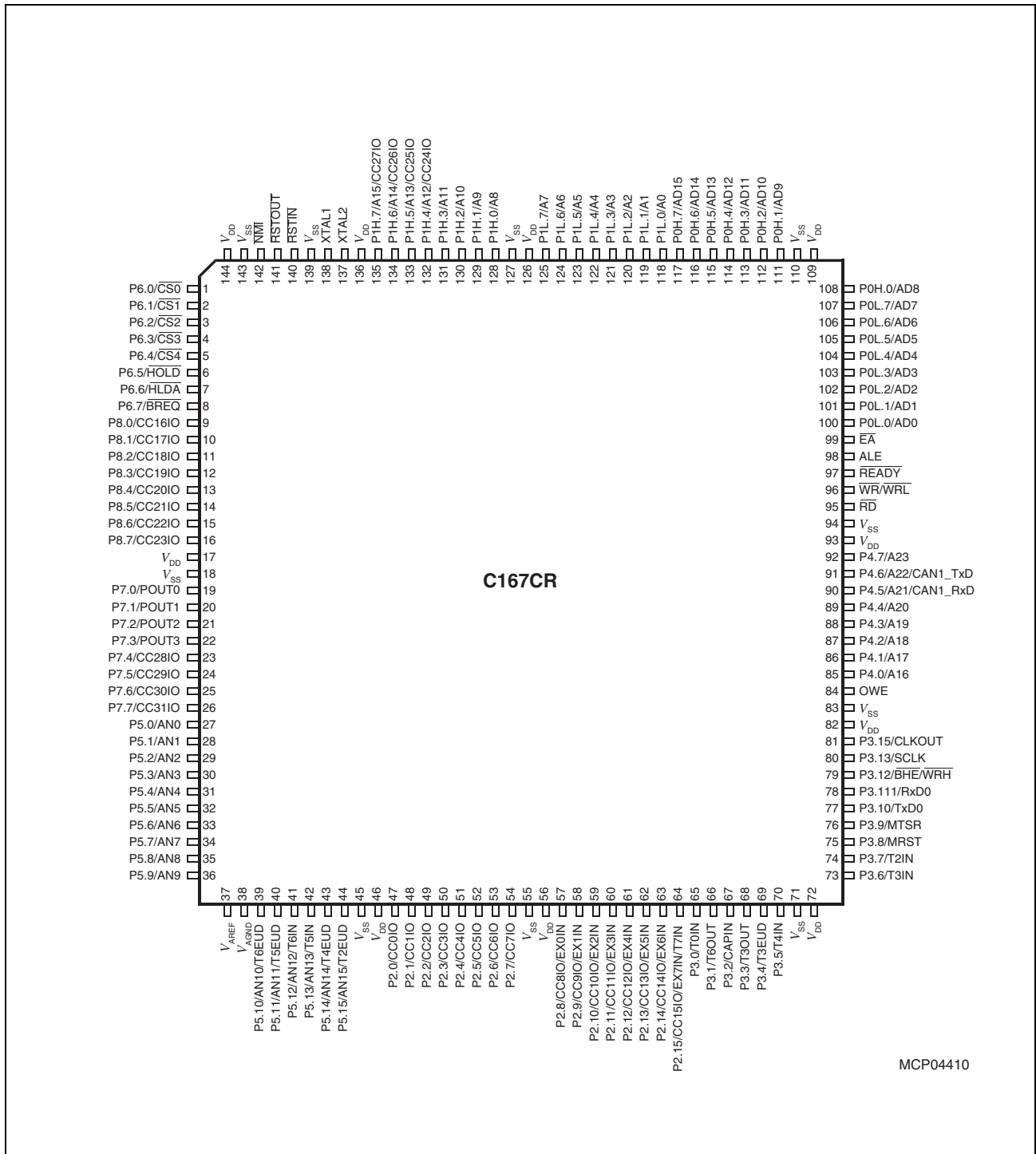


Figure 2

Table 2 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	\overline{HOLD} External Master Hold Request Input
P6.6	7	I/O	\overline{HLDA} Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	\overline{BREQ} Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	9	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	11	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	12	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P2		I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:
P2.0	47	I/O	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	48	I/O	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	49	I/O	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	50	I/O	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	51	I/O	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	52	I/O	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	53	I/O	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	54	I/O	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	57	I/O	CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, I EX0IN Fast External Interrupt 0 Input
P2.9	58	I/O	CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, I EX1IN Fast External Interrupt 1 Input
P2.10	59	I/O	CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., I EX2IN Fast External Interrupt 2 Input
P2.11	60	I/O	CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., I EX3IN Fast External Interrupt 3 Input
P2.12	61	I/O	CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., I EX4IN Fast External Interrupt 4 Input
P2.13	62	I/O	CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., I EX5IN Fast External Interrupt 5 Input
P2.14	63	I/O	CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., I EX6IN Fast External Interrupt 6 Input
P2.15	64	I/O	CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., I EX7IN Fast External Interrupt 7 Input, I T7IN CAPCOM2: Timer T7 Count Input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:
P3.0	65	I	T0IN CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	73	I	T3IN GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	75	I/O	MRST SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	TxD0 ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	RxD0 ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$ External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$ External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT System Clock Output (= CPU Clock)
OWE (V _{PP})	84	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pullup device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 μA .

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	85	O	A16 Least Significant Segment Address Line
P4.1	86	O	A17 Segment Address Line
P4.2	87	O	A18 Segment Address Line
P4.3	88	O	A19 Segment Address Line
P4.4	89	O	A20 Segment Address Line
P4.5	90	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	91	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	92	O	A23 Most Significant Segment Address Line
$\overline{\text{RD}}$	95	O	External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access.
$\overline{\text{WR/}}$ $\overline{\text{WRL}}$	96	O	External Memory Write Strobe. In $\overline{\text{WR}}$ -mode this pin is activated for every external data write access. In $\overline{\text{WRL}}$ -mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
READY	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{\text{EA}}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function																		
PORT0 P0L.0-7 P0H.0-7	100-107 108, 111-117	IO	<p>PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes:</p> <table border="0"> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>D0 – D7</td> <td>D0 – D7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>I/O</td> <td>D8 – D15</td> </tr> </table> <p>Multiplexed bus modes:</p> <table border="0"> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>AD0 – AD7</td> <td>AD0 – AD7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>A8 – A15</td> <td>AD8 – AD15</td> </tr> </table>	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	D0 – D7	D0 – D7	P0H.0 – P0H.7:	I/O	D8 – D15	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	AD0 – AD7	AD0 – AD7	P0H.0 – P0H.7:	A8 – A15	AD8 – AD15
Data Path Width:	8-bit	16-bit																			
P0L.0 – P0L.7:	D0 – D7	D0 – D7																			
P0H.0 – P0H.7:	I/O	D8 – D15																			
Data Path Width:	8-bit	16-bit																			
P0L.0 – P0L.7:	AD0 – AD7	AD0 – AD7																			
P0H.0 – P0H.7:	A8 – A15	AD8 – AD15																			
PORT1 P1L.0-7 P1H.0-7	118-125 128-135	IO	<p>PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.</p> <p>The following PORT1 pins also serve for alternate functions:</p> <table border="0"> <tr> <td>P1H.4</td> <td>132</td> <td>I</td> <td>CC24IO CAPCOM2: CC24 Capture Input</td> </tr> <tr> <td>P1H.5</td> <td>133</td> <td>I</td> <td>CC25IO CAPCOM2: CC25 Capture Input</td> </tr> <tr> <td>P1H.6</td> <td>134</td> <td>I</td> <td>CC26IO CAPCOM2: CC26 Capture Input</td> </tr> <tr> <td>P1H.7</td> <td>135</td> <td>I</td> <td>CC27IO CAPCOM2: CC27 Capture Input</td> </tr> </table>	P1H.4	132	I	CC24IO CAPCOM2: CC24 Capture Input	P1H.5	133	I	CC25IO CAPCOM2: CC25 Capture Input	P1H.6	134	I	CC26IO CAPCOM2: CC26 Capture Input	P1H.7	135	I	CC27IO CAPCOM2: CC27 Capture Input		
P1H.4	132	I	CC24IO CAPCOM2: CC24 Capture Input																		
P1H.5	133	I	CC25IO CAPCOM2: CC25 Capture Input																		
P1H.6	134	I	CC26IO CAPCOM2: CC26 Capture Input																		
P1H.7	135	I	CC27IO CAPCOM2: CC27 Capture Input																		
XTAL2 XTAL1	137 138	O I	<p>XTAL2: Output of the oscillator amplifier circuit.</p> <p>XTAL1: Input to the oscillator amplifier and input to the internal clock generator</p> <p>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.</p>																		

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Output.	Function
$\overline{\text{RSTIN}}$	140	I/O	<p>Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.</p> <p>A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.</p> <p>In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table.</p> <p><i>Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.</i></p>
$\overline{\text{RSTOUT}}$	141	O	<p>Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.</p>
$\overline{\text{NMI}}$	142	I	<p>Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.</p>
V_{AREF}	37	–	Reference voltage for the A/D converter.
V_{AGND}	38	–	Reference ground for the A/D converter.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin \overline{RSTIN} may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C167CR combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CR.

*Note: All time specifications refer to a CPU clock of 33 MHz
(see definition in the AC Characteristics section).*

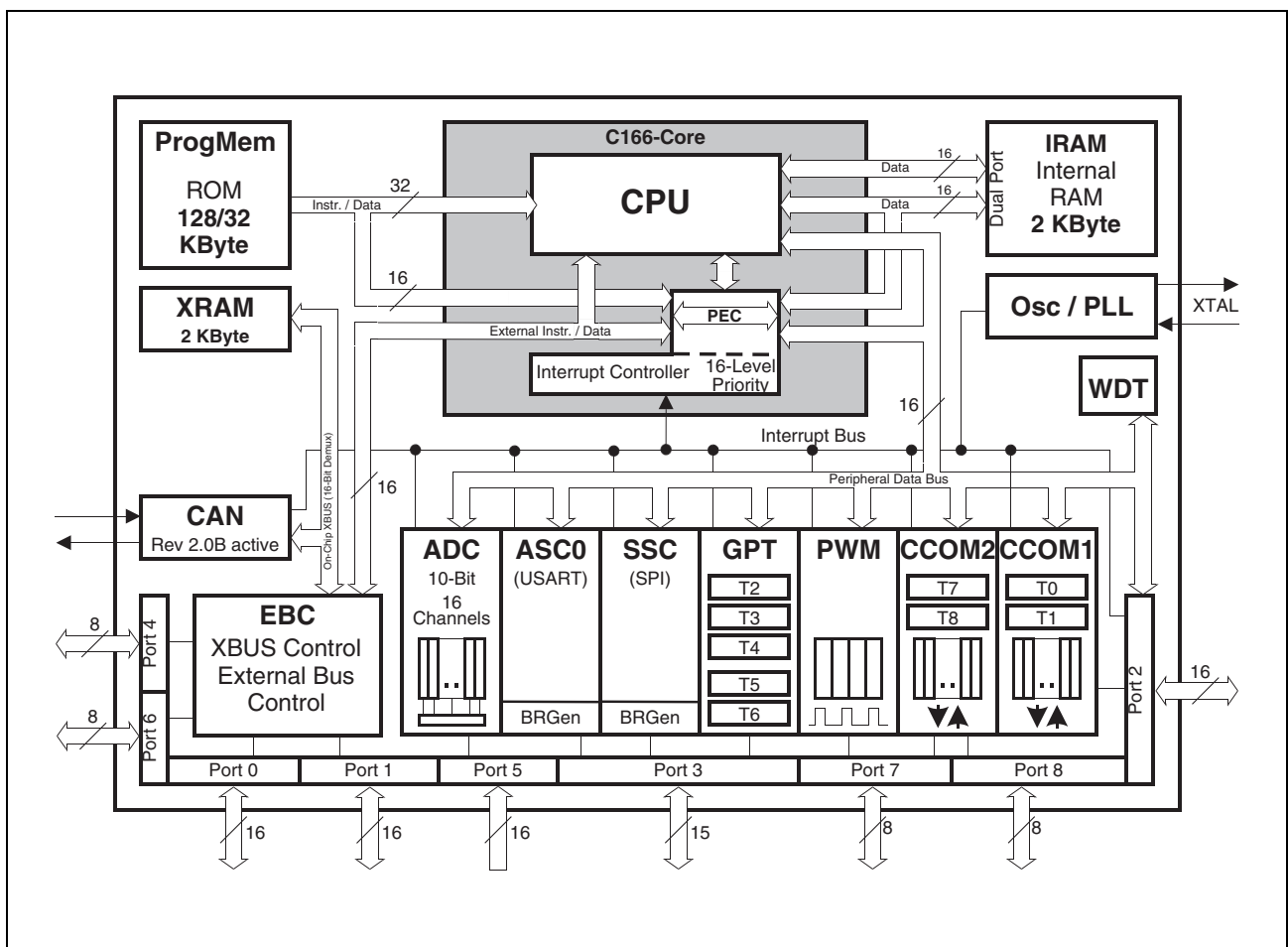


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see [Figure 3](#)).

Memory Organization

The memory space of the C167CR is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have additionally been made directly bit-addressable.

The C167CR incorporates 128/32 KBytes (depending on the derivative) of on-chip mask-programmable ROM for code or constant data. The lower 32 KBytes of the on-chip ROM can be mapped either to segment 0 or segment 1.

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

2 KBytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bit-addressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external \overline{CS} signals (4 windows plus default) can be generated in order to save external glue logic. The C167CR offers the possibility to switch the \overline{CS} outputs to an unlatched mode. In this mode the internal filter logic is switched off and the \overline{CS} signals are directly generated from the address. The unlatched \overline{CS} mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular 'Ready' function.

A $\overline{HOLD}/\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 ... P6.5 (\overline{BREQ} , \overline{HLDA} , \overline{HOLD}) are automatically controlled by the EBC. In Master Mode (default after reset) the \overline{HLDA} pin is an output. By setting bit DP6.7 to '1' the Slave Mode is selected where pin \overline{HLDA} is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Note: When the on-chip CAN Module is to be used the segment address output on Port 4 must be limited to 4 bits (i.e. A19 ... A16) in order to enable the alternate function of the CAN interface pins. CS lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CR's instructions can be executed in just one machine cycle which requires 60 ns at 33 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

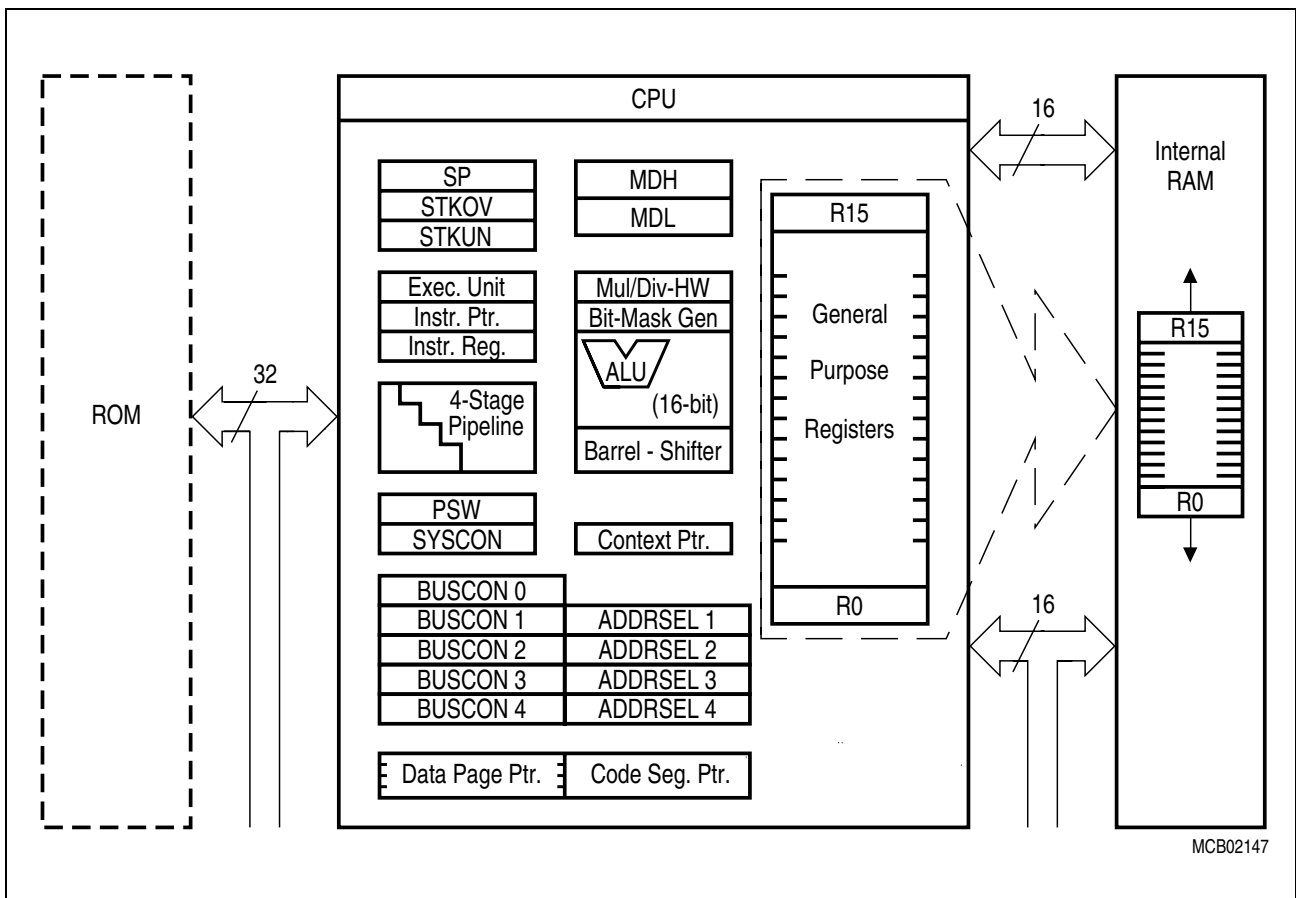


Figure 4 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C167CR instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C167CR is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CR supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CR has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C167CR interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 3 C167CR Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040 _H	10 _H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044 _H	11 _H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048 _H	12 _H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004C _H	13 _H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050 _H	14 _H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054 _H	15 _H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058 _H	16 _H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005C _H	17 _H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060 _H	18 _H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064 _H	19 _H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068 _H	1A _H
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006C _H	1B _H
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070 _H	1C _H
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074 _H	1D _H
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078 _H	1E _H
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007C _H	1F _H
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0 _H	30 _H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4 _H	31 _H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8 _H	32 _H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CC _H	33 _H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0 _H	34 _H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4 _H	35 _H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8 _H	36 _H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DC _H	37 _H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0 _H	38 _H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4 _H	39 _H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8 _H	3A _H
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00EC _H	3B _H
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00E0 _H	3C _H
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110 _H	44 _H

Table 3 C167CR Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114 _H	45 _H
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118 _H	46 _H
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080 _H	20 _H
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084 _H	21 _H
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4 _H	3D _H
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8 _H	3E _H
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088 _H	22 _H
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008C _H	23 _H
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090 _H	24 _H
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094 _H	25 _H
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098 _H	26 _H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	00'009C _H	27 _H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0 _H	28 _H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4 _H	29 _H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8 _H	2A _H
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011C _H	47 _H
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00AC _H	2B _H
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0 _H	2C _H
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4 _H	2D _H
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8 _H	2E _H
SSC Error	SCEIR	SCEIE	SCEINT	00'00BC _H	2F _H
PWM Channel 0 ... 3	PWMIR	PWMIE	PWMINT	00'00FC _H	3F _H
CAN Interface 1	XP0IR	XP0IE	XP0INT	00'0100 _H	40 _H
Unassigned node	XP1IR	XP1IE	XP1INT	00'0104 _H	41 _H
Unassigned node	XP2IR	XP2IE	XP2INT	00'0108 _H	42 _H
PLL/OWD	XP3IR	XP3IE	XP3INT	00'010C _H	43 _H

The C167CR also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: – Hardware Reset – Software Reset – W-dog Timer Overflow	–	RESET RESET RESET	00'0000 _H 00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	III III III
Class A Hardware Traps: – Non-Maskable Interrupt – Stack Overflow – Stack Underflow	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	II II II
Class B Hardware Traps: – Undefined Opcode – Protected Instruction Fault – Illegal Word Operand Access – Illegal Instruction Access – Illegal External Bus Access	UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	BTRAP BTRAP BTRAP BTRAP BTRAP	00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H	0A _H 0A _H 0A _H 0A _H 0A _H	I I I I I
Reserved	–	–	[2C _H – 3C _H]	[0B _H – 0F _H]	–
Software Traps – TRAP Instruction	–	–	Any [00'0000 _H – 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority

Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin (except for CC24 ... CC27) to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 5 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

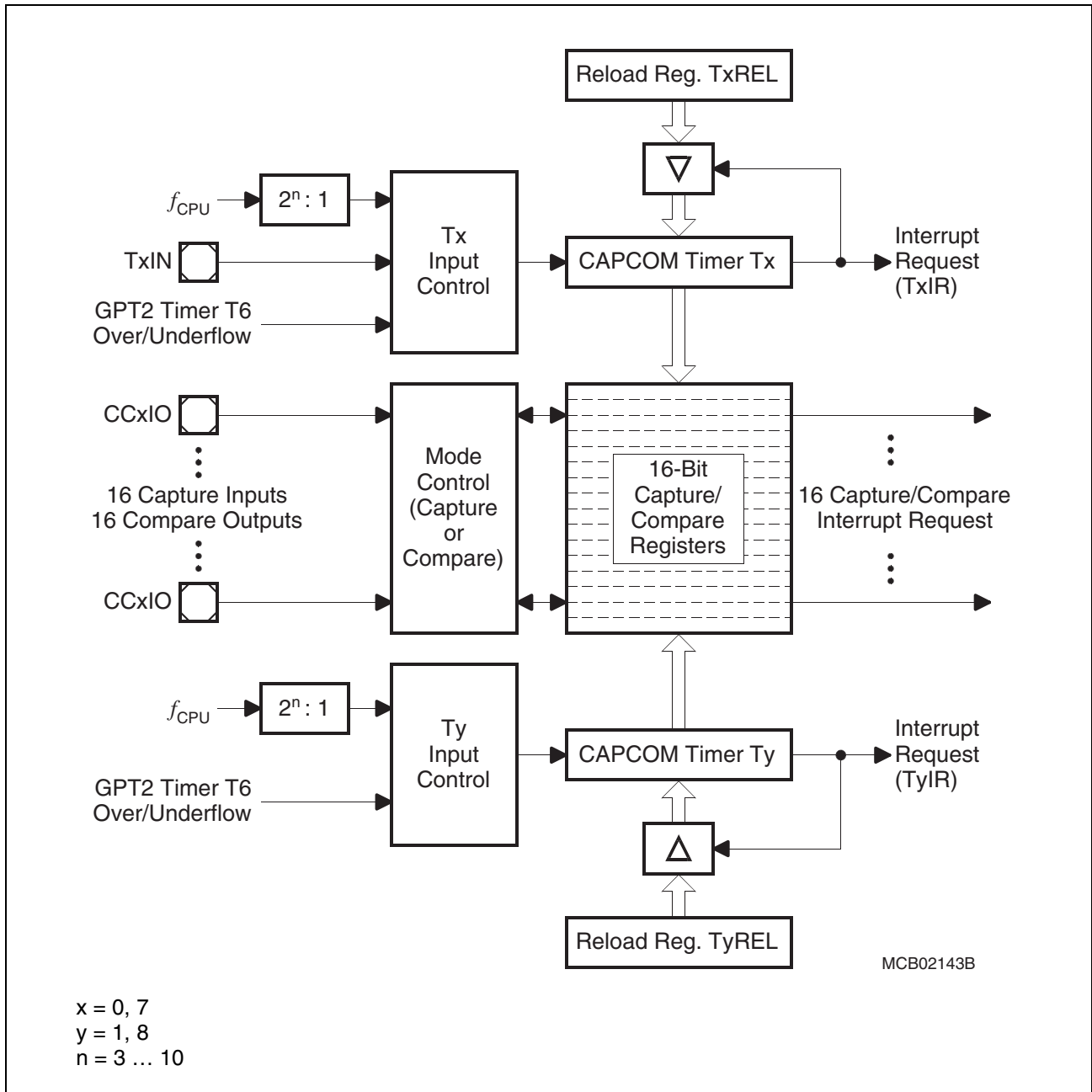


Figure 5 CAPCOM Unit Block Diagram

PWM Module

The Pulse Width Modulation Module can generate up to four PWM output signals using edge-aligned or center-aligned PWM. In addition the PWM module can generate PWM burst signals and single shot outputs. The frequency range of the PWM signals covers 4 Hz to 16.5 MHz (referred to a CPU clock of 33 MHz), depending on the resolution of the PWM output signal. The level of the output signals is selectable and the PWM module can generate interrupt requests.

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

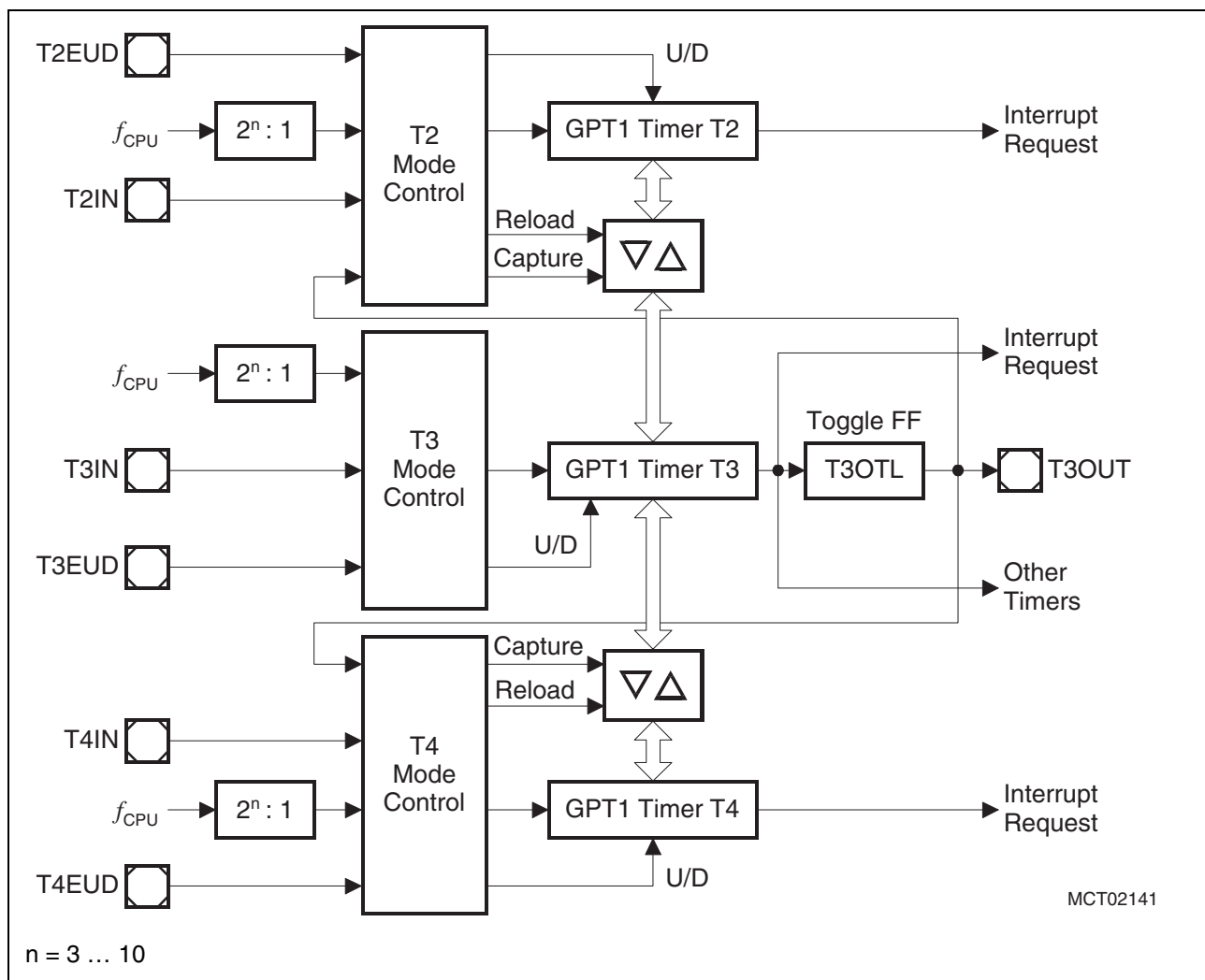
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.



MCT02141

Figure 6 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C167CR to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

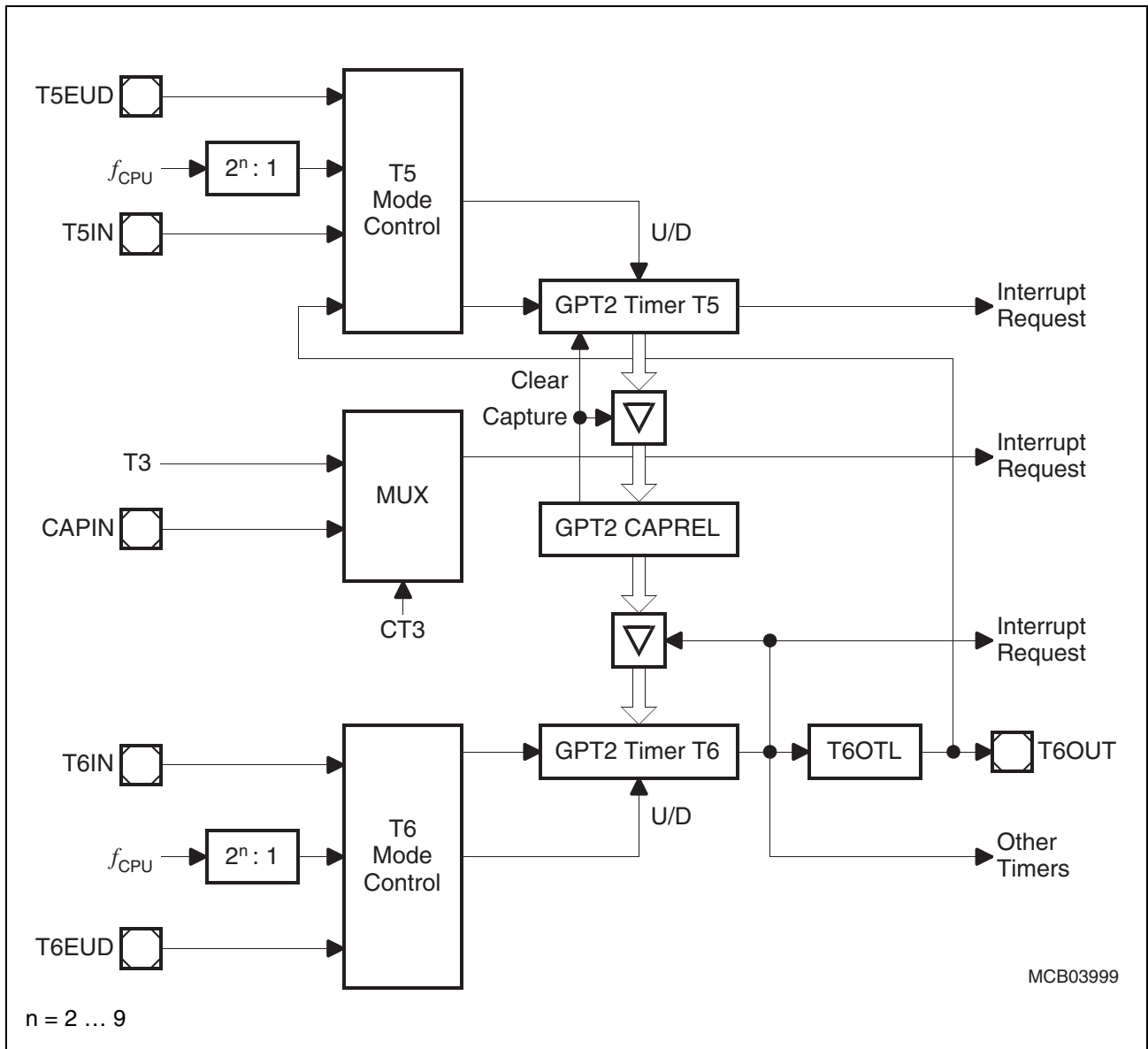


Figure 7 Block Diagram of GPT2

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 Kbit/s/ 1.03 Mbit/s and half-duplex synchronous communication at up to 3.1/4.1 Mbit/s (@ 25/ 33 MHz CPU clock).

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 6.25/8.25 Mbit/s (@ 25/33 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception, and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

CAN-Module

The integrated CAN-Module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip CAN-Module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The module provides Full CAN functionality on up to 15 message objects. Message object 15 may be configured for Basic CAN functionality. Both modes provide separate masks for acceptance filtering which allows to accept a number of identifiers in Full CAN mode and also allows to disregard a number of identifiers in Basic CAN mode. All message objects can be updated independent from the other objects and are equipped for the maximum message length of 8 bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1 Mbit/s. The CAN-Module uses two pins of Port 4 to interface to an external bus transceiver.

Note: When the CAN interface is to be used the segment address output on Port 4 must be limited to 4 bits, i.e. A19 ... A16. This is necessary to enable the alternate function of the CAN interface pins.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 15.5 μs and 254 ms can be monitored (@ 33 MHz).

The default Watchdog Timer interval after reset is 3.97 ms (@ 33 MHz).

Parallel Ports

The C167CR provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7, and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17 ... A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.

Port 2, Port 8 and Port 7 (and parts of PORT1) are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.

Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}/\overline{\text{WRH}}$, and the system clock output (CLKOUT).

Port 5 is used for the analog input channels to the A/D converter or timer control signals.

The edge characteristics (transition time) of the C167CR's port drivers can be selected via the Port Driver Control Register (PDCR). Two bits select fast edges ('0') or reduced edges ('1') for bus interface pins and non-bus pins separately.

PDCR.0 = BIPEC controls PORT0, PORT1, Port 4, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ALE, CLKOUT, $\overline{\text{BHE}}/\overline{\text{WRH}}$.

PDCR.4 = NBPEC controls Port 3, Port 8, $\overline{\text{RSTOUT}}$, $\overline{\text{RSTIN}}$ (bidir. reset mode).

Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock / OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly ($f_{\text{CPU}} = 2 \dots 5 \text{ MHz}$).

In prescaler mode the PLL base frequency is divided by 2 ($f_{\text{CPU}} = 1 \dots 2.5 \text{ MHz}$).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled via hardware by (externally) pulling low pin OWE (internal pullup provides high level if not connected). In this case (OWE = '0') the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler. Also no interrupt request will be generated in case of a missing oscillator clock.

Instruction Set Summary

Table 6 lists the instructions of the C167CR in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**C166 Family Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 6 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Table 6 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$ -pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C167CR in alphabetical order.

Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter “E” in column “Physical Address”. Registers within on-chip X-peripherals are marked with the letter “X” in column “Physical Address”.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Note: Registers within device specific interface modules (CAN) are only present in the corresponding device, of course.

Table 7 C167CR Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	FF98 _H	CC _H	A/D Converter End of Conversion Interrupt Control Register	0000 _H
ADCON b	FFA0 _H	D0 _H	A/D Converter Control Register	0000 _H
ADDAT	FEA0 _H	50 _H	A/D Converter Result Register	0000 _H
ADDAT2	F0A0 _H E	50 _H	A/D Converter 2 Result Register	0000 _H
ADDRSEL1	FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2	FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3	FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4	FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC b	FF9A _H	CD _H	A/D Converter Overrun Error Interrupt Control Register	0000 _H
BUSCON0 b	FF0C _H	86 _H	Bus Configuration Register 0	0XX0 _H
BUSCON1 b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2 b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3 b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4 b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
C1BTR	EF04 _H X	---	CAN1 Bit Timing Register	UUUU _H
C1CSR	EF00 _H X	---	CAN1 Control / Status Register	XX01 _H
C1GMS	EF06 _H X	---	CAN1 Global Mask Short	UFUU _H
C1IR	EF02 _H X	---	CAN1 Interrupt Register	XX _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
C1LGML	EF0A _H X	---	CAN1 Lower Global Mask Long	UUUU _H
C1LMLM	EF0E _H X	---	CAN1 Lower Mask of Last Message	UUUU _H
C1UAR	EFn2 _H X	---	CAN1 Upper Arbitration Register (message n)	UUUU _H
C1UGML	EF08 _H X	---	CAN1 Upper Global Mask Long	UUUU _H
C1UMLM	EF0C _H X	---	CAN1 Upper Mask of Last Message	UUUU _H
CAPREL	FE4A _H	25 _H	GPT2 Capture/Reload Register	0000 _H
CC0	FE80 _H	40 _H	CAPCOM Register 0	0000 _H
CC0IC	b FF78 _H	BC _H	CAPCOM Register 0 Interrupt Ctrl. Reg.	0000 _H
CC1	FE82 _H	41 _H	CAPCOM Register 1	0000 _H
CC10	FE94 _H	4A _H	CAPCOM Register 10	0000 _H
CC10IC	b FF8C _H	C6 _H	CAPCOM Reg. 10 Interrupt Ctrl. Reg.	0000 _H
CC11	FE96 _H	4B _H	CAPCOM Register 11	0000 _H
CC11IC	b FF8E _H	C7 _H	CAPCOM Reg. 11 Interrupt Ctrl. Reg.	0000 _H
CC12	FE98 _H	4C _H	CAPCOM Register 12	0000 _H
CC12IC	b FF90 _H	C8 _H	CAPCOM Reg. 12 Interrupt Ctrl. Reg.	0000 _H
CC13	FE9A _H	4D _H	CAPCOM Register 13	0000 _H
CC13IC	b FF92 _H	C9 _H	CAPCOM Reg. 13 Interrupt Ctrl. Reg.	0000 _H
CC14	FE9C _H	4E _H	CAPCOM Register 14	0000 _H
CC14IC	b FF94 _H	CA _H	CAPCOM Reg. 14 Interrupt Ctrl. Reg.	0000 _H
CC15	FE9E _H	4F _H	CAPCOM Register 15	0000 _H
CC15IC	b FF96 _H	CB _H	CAPCOM Reg. 15 Interrupt Ctrl. Reg.	0000 _H
CC16	FE60 _H	30 _H	CAPCOM Register 16	0000 _H
CC16IC	b F160 _H E	B0 _H	CAPCOM Reg. 16 Interrupt Ctrl. Reg.	0000 _H
CC17	FE62 _H	31 _H	CAPCOM Register 17	0000 _H
CC17IC	b F162 _H E	B1 _H	CAPCOM Reg. 17 Interrupt Ctrl. Reg.	0000 _H
CC18	FE64 _H	32 _H	CAPCOM Register 18	0000 _H
CC18IC	b F164 _H E	B2 _H	CAPCOM Reg. 18 Interrupt Ctrl. Reg.	0000 _H
CC19	FE66 _H	33 _H	CAPCOM Register 19	0000 _H
CC19IC	b F166 _H E	B3 _H	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC1IC b	FF7A _H	BD _H	CAPCOM Reg. 1 Interrupt Ctrl. Reg.	0000 _H
CC2	FE84 _H	42 _H	CAPCOM Register 2	0000 _H
CC20	FE68 _H	34 _H	CAPCOM Register 20	0000 _H
CC20IC b	F168 _H E	B4 _H	CAPCOM Reg. 20 Interrupt Ctrl. Reg.	0000 _H
CC21	FE6A _H	35 _H	CAPCOM Register 21	0000 _H
CC21IC b	F16A _H E	B5 _H	CAPCOM Reg. 21 Interrupt Ctrl. Reg.	0000 _H
CC22	FE6C _H	36 _H	CAPCOM Register 22	0000 _H
CC22IC b	F16C _H E	B6 _H	CAPCOM Reg. 22 Interrupt Ctrl. Reg.	0000 _H
CC23	FE6E _H	37 _H	CAPCOM Register 23	0000 _H
CC23IC b	F16E _H E	B7 _H	CAPCOM Reg. 23 Interrupt Ctrl. Reg.	0000 _H
CC24	FE70 _H	38 _H	CAPCOM Register 24	0000 _H
CC24IC b	F170 _H E	B8 _H	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000 _H
CC25	FE72 _H	39 _H	CAPCOM Register 25	0000 _H
CC25IC b	F172 _H E	B9 _H	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000 _H
CC26	FE74 _H	3A _H	CAPCOM Register 26	0000 _H
CC26IC b	F174 _H E	BA _H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000 _H
CC27	FE76 _H	3B _H	CAPCOM Register 27	0000 _H
CC27IC b	F176 _H E	BB _H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000 _H
CC28	FE78 _H	3C _H	CAPCOM Register 28	0000 _H
CC28IC b	F178 _H E	BC _H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000 _H
CC29	FE7A _H	3D _H	CAPCOM Register 29	0000 _H
CC29IC b	F184 _H E	C2 _H	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000 _H
CC2IC b	FF7C _H	BE _H	CAPCOM Reg. 2 Interrupt Ctrl. Reg.	0000 _H
CC3	FE86 _H	43 _H	CAPCOM Register 3	0000 _H
CC30	FE7C _H	3E _H	CAPCOM Register 30	0000 _H
CC30IC b	F18C _H E	C6 _H	CAPCOM Reg. 30 Interrupt Ctrl. Reg.	0000 _H
CC31	FE7E _H	3F _H	CAPCOM Register 31	0000 _H
CC31IC b	F194 _H E	CA _H	CAPCOM Reg. 31 Interrupt Ctrl. Reg.	0000 _H
CC3IC b	FF7E _H	BF _H	CAPCOM Reg. 3 Interrupt Ctrl. Reg.	0000 _H
CC4	FE88 _H	44 _H	CAPCOM Register 4	0000 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
CC4IC	b	FF80 _H	C0 _H	CAPCOM Reg. 4 Interrupt Ctrl. Reg.	0000 _H
CC5		FE8A _H	45 _H	CAPCOM Register 5	0000 _H
CC5IC	b	FF82 _H	C1 _H	CAPCOM Register 5 Interrupt Control Register	0000 _H
CC6		FE8C _H	46 _H	CAPCOM Register 6	0000 _H
CC6IC	b	FF84 _H	C2 _H	CAPCOM Reg. 6 Interrupt Ctrl. Reg.	0000 _H
CC7		FE8E _H	47 _H	CAPCOM Register 7	0000 _H
CC7IC	b	FF86 _H	C3 _H	CAPCOM Reg. 7 Interrupt Ctrl. Reg.	0000 _H
CC8		FE90 _H	48 _H	CAPCOM Register 8	0000 _H
CC8IC	b	FF88 _H	C4 _H	CAPCOM Reg. 8 Interrupt Ctrl. Reg.	0000 _H
CC9		FE92 _H	49 _H	CAPCOM Register 9	0000 _H
CC9IC	b	FF8A _H	C5 _H	CAPCOM Reg. 9 Interrupt Ctrl. Reg.	0000 _H
CCM0	b	FF52 _H	A9 _H	CAPCOM Mode Control Register 0	0000 _H
CCM1	b	FF54 _H	AA _H	CAPCOM Mode Control Register 1	0000 _H
CCM2	b	FF56 _H	AB _H	CAPCOM Mode Control Register 2	0000 _H
CCM3	b	FF58 _H	AC _H	CAPCOM Mode Control Register 3	0000 _H
CCM4	b	FF22 _H	91 _H	CAPCOM Mode Control Register 4	0000 _H
CCM5	b	FF24 _H	92 _H	CAPCOM Mode Control Register 5	0000 _H
CCM6	b	FF26 _H	93 _H	CAPCOM Mode Control Register 6	0000 _H
CCM7	b	FF28 _H	94 _H	CAPCOM Mode Control Register 7	0000 _H
CP		FE10 _H	08 _H	CPU Context Pointer Register	FC00 _H
CRIC	b	FF6A _H	B5 _H	GPT2 CAPREL Interrupt Ctrl. Register	0000 _H
CSP		FE08 _H	04 _H	CPU Code Segment Pointer Register (read only)	0000 _H
DP0L	b	F100 _H	E 80 _H	P0L Direction Control Register	00 _H
DP0H	b	F102 _H	E 81 _H	P0H Direction Control Register	00 _H
DP1L	b	F104 _H	E 82 _H	P1L Direction Control Register	00 _H
DP1H	b	F106 _H	E 83 _H	P1H Direction Control Register	00 _H
DP2	b	FFC2 _H	E1 _H	Port 2 Direction Control Register	0000 _H
DP3	b	FFC6 _H	E3 _H	Port 3 Direction Control Register	0000 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
DP4	b	FFCA _H	E5 _H	Port 4 Direction Control Register	00 _H
DP6	b	FFCE _H	E7 _H	Port 6 Direction Control Register	00 _H
DP7	b	FFD2 _H	E9 _H	Port 7 Direction Control Register	00 _H
DP8	b	FFD6 _H	EB _H	Port 8 Direction Control Register	00 _H
DPP0		FE00 _H	00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H
DPP1		FE02 _H	01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H
DPP2		FE04 _H	02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H
DPP3		FE06 _H	03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H
EXICON	b	F1C0 _H	E E0 _H	External Interrupt Control Register	0000 _H
MDC	b	FF0E _H	87 _H	CPU Multiply Divide Control Register	0000 _H
MDH		FE0C _H	06 _H	CPU Multiply Divide Reg. – High Word	0000 _H
MDL		FE0E _H	07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H
ODP2	b	F1C2 _H	E E1 _H	Port 2 Open Drain Control Register	0000 _H
ODP3	b	F1C6 _H	E E3 _H	Port 3 Open Drain Control Register	0000 _H
ODP6	b	F1CE _H	E E7 _H	Port 6 Open Drain Control Register	00 _H
ODP7	b	F1D2 _H	E E9 _H	Port 7 Open Drain Control Register	00 _H
ODP8	b	F1D6 _H	E EB _H	Port 8 Open Drain Control Register	00 _H
ONES		FF1E _H	8F _H	Constant Value 1's Register (read only)	FFFF _H
P0H	b	FF02 _H	81 _H	Port 0 High Reg. (Upper half of PORT0)	00 _H
P0L	b	FF00 _H	80 _H	Port 0 Low Reg. (Lower half of PORT0)	00 _H
P1H	b	FF06 _H	83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b	FF04 _H	82 _H	Port 1 Low Reg. (Lower half of PORT1)	00 _H
P2	b	FFC0 _H	E0 _H	Port 2 Register	0000 _H
P3	b	FFC4 _H	E2 _H	Port 3 Register	0000 _H
P4	b	FFC8 _H	E4 _H	Port 4 Register (8 bits)	00 _H
P5	b	FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P5DIDIS	b	FFA4 _H	D2 _H	Port 5 Digital Input Disable Register	0000 _H
P6	b	FFCC _H	E6 _H	Port 6 Register (8 bits)	00 _H
P7	b	FFD0 _H	E8 _H	Port 7 Register (8 bits)	00 _H
P8	b	FFD4 _H	EA _H	Port 8 Register (8 bits)	00 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
PECC0	FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1	FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2	FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3	FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4	FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5	FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6	FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7	FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PICON b	F1C4 _H	E E2 _H	Port Input Threshold Control Register	0000 _H
PDCR	F0AA _H	E 55 _H	Pin Driver Control Register	0000 _H
PP0	F038 _H	E 1C _H	PWM Module Period Register 0	0000 _H
PP1	F03A _H	E 1D _H	PWM Module Period Register 1	0000 _H
PP2	F03C _H	E 1E _H	PWM Module Period Register 2	0000 _H
PP3	F03E _H	E 1F _H	PWM Module Period Register 3	0000 _H
PSW b	FF10 _H	88 _H	CPU Program Status Word	0000 _H
PT0	F030 _H	E 18 _H	PWM Module Up/Down Counter 0	0000 _H
PT1	F032 _H	E 19 _H	PWM Module Up/Down Counter 1	0000 _H
PT2	F034 _H	E 1A _H	PWM Module Up/Down Counter 2	0000 _H
PT3	F036 _H	E 1B _H	PWM Module Up/Down Counter 3	0000 _H
PW0	FE30 _H	18 _H	PWM Module Pulse Width Register 0	0000 _H
PW1	FE32 _H	19 _H	PWM Module Pulse Width Register 1	0000 _H
PW2	FE34 _H	1A _H	PWM Module Pulse Width Register 2	0000 _H
PW3	FE36 _H	1B _H	PWM Module Pulse Width Register 3	0000 _H
PWMCON0 b	FF30 _H	98 _H	PWM Module Control Register 0	0000 _H
PWMCON1 b	FF32 _H	99 _H	PWM Module Control Register 1	0000 _H
PWMIC b	F17E _H	E BF _H	PWM Module Interrupt Control Register	0000 _H
RP0H b	F108 _H	E 84 _H	System Start-up Config. Reg. (Rd. only)	XX _H
S0BG	FEB4 _H	5A _H	Serial Channel 0 Baudrate Generator Reload Register	0000 _H
S0CON b	FFB0 _H	D8 _H	Serial Channel 0 Control Register	0000 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
S0EIC	b FF70 _H	B8 _H	Serial Chan. 0 Error Interrupt Ctrl. Reg.	0000 _H
S0RBUF	FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	XX _H
S0RIC	b FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC	b F19C _H	E CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF	FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Reg. (write only)	00 _H
S0TIC	b FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H
SP	FE12 _H	09 _H	CPU System Stack Pointer Register	FC00 _H
SSCBR	F0B4 _H	E 5A _H	SSC Baudrate Register	0000 _H
SSCCON	b FFB2 _H	D9 _H	SSC Control Register	0000 _H
SSCEIC	b FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB	F0B2 _H	E 59 _H	SSC Receive Buffer	XXXX _H
SSCRIC	b FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB	F0B0 _H	E 58 _H	SSC Transmit Buffer	0000 _H
SSCTIC	b FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV	FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN	FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b FF12 _H	89 _H	CPU System Configuration Register	¹⁾ 0xx0 _H
T0	FE50 _H	28 _H	CAPCOM Timer 0 Register	0000 _H
T01CON	b FF50 _H	A8 _H	CAPCOM Timer 0 and Timer 1 Ctrl. Reg.	0000 _H
T0IC	b FF9C _H	CE _H	CAPCOM Timer 0 Interrupt Ctrl. Reg.	0000 _H
T0REL	FE54 _H	2A _H	CAPCOM Timer 0 Reload Register	0000 _H
T1	FE52 _H	29 _H	CAPCOM Timer 1 Register	0000 _H
T1IC	b FF9E _H	CF _H	CAPCOM Timer 1 Interrupt Ctrl. Reg.	0000 _H
T1REL	FE56 _H	2B _H	CAPCOM Timer 1 Reload Register	0000 _H
T2	FE40 _H	20 _H	GPT1 Timer 2 Register	0000 _H
T2CON	b FF40 _H	A0 _H	GPT1 Timer 2 Control Register	0000 _H

Table 7 C167CR Registers, Ordered by Name (cont'd)

Name		Physical Address	8-Bit Addr.	Description	Reset Value
T2IC	b	FF60 _H	B0 _H	GPT1 Timer 2 Interrupt Control Register	0000 _H
T3		FE42 _H	21 _H	GPT1 Timer 3 Register	0000 _H
T3CON	b	FF42 _H	A1 _H	GPT1 Timer 3 Control Register	0000 _H
T3IC	b	FF62 _H	B1 _H	GPT1 Timer 3 Interrupt Control Register	0000 _H
T4		FE44 _H	22 _H	GPT1 Timer 4 Register	0000 _H
T4CON	b	FF44 _H	A2 _H	GPT1 Timer 4 Control Register	0000 _H
T4IC	b	FF64 _H	B2 _H	GPT1 Timer 4 Interrupt Control Register	0000 _H
T5		FE46 _H	23 _H	GPT2 Timer 5 Register	0000 _H
T5CON	b	FF46 _H	A3 _H	GPT2 Timer 5 Control Register	0000 _H
T5IC	b	FF66 _H	B3 _H	GPT2 Timer 5 Interrupt Control Register	0000 _H
T6		FE48 _H	24 _H	GPT2 Timer 6 Register	0000 _H
T6CON	b	FF48 _H	A4 _H	GPT2 Timer 6 Control Register	0000 _H
T6IC	b	FF68 _H	B4 _H	GPT2 Timer 6 Interrupt Control Register	0000 _H
T7		F050 _H	E 28 _H	CAPCOM Timer 7 Register	0000 _H
T78CON	b	FF20 _H	90 _H	CAPCOM Timer 7 and 8 Ctrl. Reg.	0000 _H
T7IC	b	F17A _H	E BE _H	CAPCOM Timer 7 Interrupt Ctrl. Reg.	0000 _H
T7REL		F054 _H	E 2A _H	CAPCOM Timer 7 Reload Register	0000 _H
T8		F052 _H	E 29 _H	CAPCOM Timer 8 Register	0000 _H
T8IC	b	F17C _H	E BF _H	CAPCOM Timer 8 Interrupt Ctrl. Reg.	0000 _H
T8REL		F056 _H	E 2B _H	CAPCOM Timer 8 Reload Register	0000 _H
TFR	b	FFAC _H	D6 _H	Trap Flag Register	0000 _H
WDT		FEAE _H	57 _H	Watchdog Timer Register (read only)	0000 _H
WDTCON		FFAE _H	D7 _H	Watchdog Timer Control Register	²⁾ 00XX _H
XP0IC	b	F186 _H	E C3 _H	CAN1 Module Interrupt Control Register	0000 _H
XP1IC	b	F18E _H	E C7 _H	Unassigned Interrupt Control Register	0000 _H
XP2IC	b	F196 _H	E CB _H	Unassigned Interrupt Control Register	0000 _H
XP3IC	b	F19E _H	E CF _H	PLL/OWD Interrupt Control Register	0000 _H
ZEROS	b	FF1C _H	8E _H	Constant Value 0's Register (read only)	0000 _H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Absolute Maximum Ratings

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	$V_{DD} + 0.5$	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	100	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 9 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, $f_{CPUmax} = 33$ MHz
		2.5 ¹⁾	5.5	V	Power Down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin ²⁾³⁾
Absolute sum of overload currents	$\Sigma I_{OV} $	–	50	mA	³⁾
External Load Capacitance	C_L	–	50	pF	Pin drivers in fast edge mode (PDCR.BIPEC = '0')
		–	30	pF	Pin drivers in reduced edge mode (PDCR.BIPEC = '1') ³⁾
		–	100	pF	Pin drivers in fast edge mode, $f_{CPUmax} = 25$ MHz ⁴⁾
Ambient temperature	T_A	0	70	°C	SAB-C167CR ...
		-40	85	°C	SAF-C167CR ...
		-40	125	°C	SAK-C167CR ...

¹⁾ Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

²⁾ Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins like XTAL1, \overline{RD} , \overline{WR} , etc.

³⁾ Not 100% tested, guaranteed by design and characterization.

⁴⁾ The increased capacitive load is valid for the 25 MHz-derivatives up to a CPU clock frequency of 25 MHz. Under these circumstances the timing parameters as specified in the "C167CR Data Sheet 1999-06" are valid.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CR and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the C167CR will provide signals with the respective timing characteristics.

SR (System Requirement):

The external system must provide signals with the respective timing characteristics to the C167CR.

DC Characteristics

(Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (TTL, all except XTAL1)	V_{IL} SR	-0.5	$0.2 V_{DD} - 0.1$	V	–
Input low voltage XTAL1	V_{IL2} SR	-0.5	$0.3 V_{DD}$	V	–
Input low voltage (Special Threshold)	V_{ILS} SR	-0.5	2.0	V	–
Input high voltage (TTL, all except \overline{RSTIN} and XTAL1)	V_{IH} SR	$0.2 V_{DD} + 0.9$	$V_{DD} + 0.5$	V	–
Input high voltage \overline{RSTIN} (when operated as input)	V_{IH1} SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	–
Input high voltage XTAL1	V_{IH2} SR	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	–
Input high voltage (Special Threshold)	V_{IHS} SR	$0.8 V_{DD} - 0.2$	$V_{DD} + 0.5$	V	–
Input Hysteresis (Special Threshold)	HYS	400	–	mV	Series resistance = 0Ω
Output low voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTOUT} , $\overline{RSTIN}^{(2)}$)	V_{OL} CC	–	0.45	V	$I_{OL} = 2.4 \text{ mA}$
Output low voltage (all other outputs)	V_{OL1CC}	–	0.45	V	$I_{OL} = 1.6 \text{ mA}$

DC Characteristics (cont'd)
 (Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output high voltage ³⁾ (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTOUT})	V_{OH} CC	2.4	–	V	$I_{OH} = -2.4$ mA
		$0.9 V_{DD}$	–	V	$I_{OH} = -0.5$ mA
Output high voltage ³⁾ (all other outputs)	V_{OH1} CC	2.4	–	V	$I_{OH} = -1.6$ mA
		$0.9 V_{DD}$	–	V	$I_{OH} = -0.5$ mA
Input leakage current (Port 5)	I_{OZ1} CC	–	± 200	nA	$0 V < V_{IN} < V_{DD}$
Input leakage current (all other) ⁴⁾	I_{OZ2} CC	–	± 500	nA	$0.45 V < V_{IN} < V_{DD}$
\overline{RSTIN} inactive current ⁵⁾	I_{RSTH} ⁶⁾	–	-10	μ A	$V_{IN} = V_{IH1}$
\overline{RSTIN} active current ⁵⁾	I_{RSTL} ⁷⁾	-100	–	μ A	$V_{IN} = V_{IL}$
$\overline{READY}/\overline{RD}/\overline{WR}$ inact. current ⁸⁾	I_{RWH} ⁶⁾	–	-40	μ A	$V_{OUT} = 2.4$ V
$\overline{READY}/\overline{RD}/\overline{WR}$ active current ⁸⁾	I_{RWL} ⁷⁾	-500	–	μ A	$V_{OUT} = V_{OLmax}$
ALE inactive current ⁸⁾	I_{ALEL} ⁶⁾	–	40	μ A	$V_{OUT} = V_{OLmax}$
ALE active current ⁸⁾	I_{ALEH} ⁷⁾	500	–	μ A	$V_{OUT} = 2.4$ V
Port 6 inactive current ⁸⁾	I_{P6H} ⁶⁾	–	-40	μ A	$V_{OUT} = 2.4$ V
Port 6 active current ⁸⁾	I_{P6L} ⁷⁾	-500	–	μ A	$V_{OUT} = V_{OL1max}$
PORT0 configuration current ⁹⁾	I_{POH} ⁶⁾	–	-10	μ A	$V_{IN} = V_{IHmin}$
	I_{POL} ⁷⁾	-100	–	μ A	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	± 20	μ A	$0 V < V_{IN} < V_{DD}$
Pin capacitance ¹⁰⁾ (digital inputs/outputs)	C_{IO} CC	–	10	pF	$f = 1$ MHz $T_A = 25$ °C

¹⁾ Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .

²⁾ Valid in bidirectional reset mode only.

³⁾ This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

⁴⁾ This parameter is not valid for pins \overline{READY} , ALE, \overline{RD} , and \overline{WR} while the respective pull device is on.

⁵⁾ These parameters describe the \overline{RSTIN} pullup, which equals a resistance of ca. 50 to 250 k Ω .

⁶⁾ The maximum current may be drawn while the respective signal line remains inactive.

⁷⁾ The minimum current must be drawn in order to drive the respective signal line active.

- 8) This specification is valid during Reset and during Hold-mode or Adapt-mode. During Hold-mode Port 6 pins are only affected, if they are used (configured) for \overline{CS} output and the open drain function is not enabled. The READY-pullup is always active, except for Powerdown mode.
- 9) This specification is valid during Reset and during Adapt-mode.
- 10) Not 100% tested, guaranteed by design and characterization.

Power Consumption C167CR

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	$15 + 2.5 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current	I_{ID}	–	$10 + 1.0 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ¹⁾
Power-down mode supply current	I_{PD}	–	50	μA	$V_{DD} = V_{DDmax}$ ²⁾

- 1) The supply current is a function of the operating frequency. This dependency is illustrated in [Figure 8](#). These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 2) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD} , all outputs (including pins configured as outputs) disconnected.

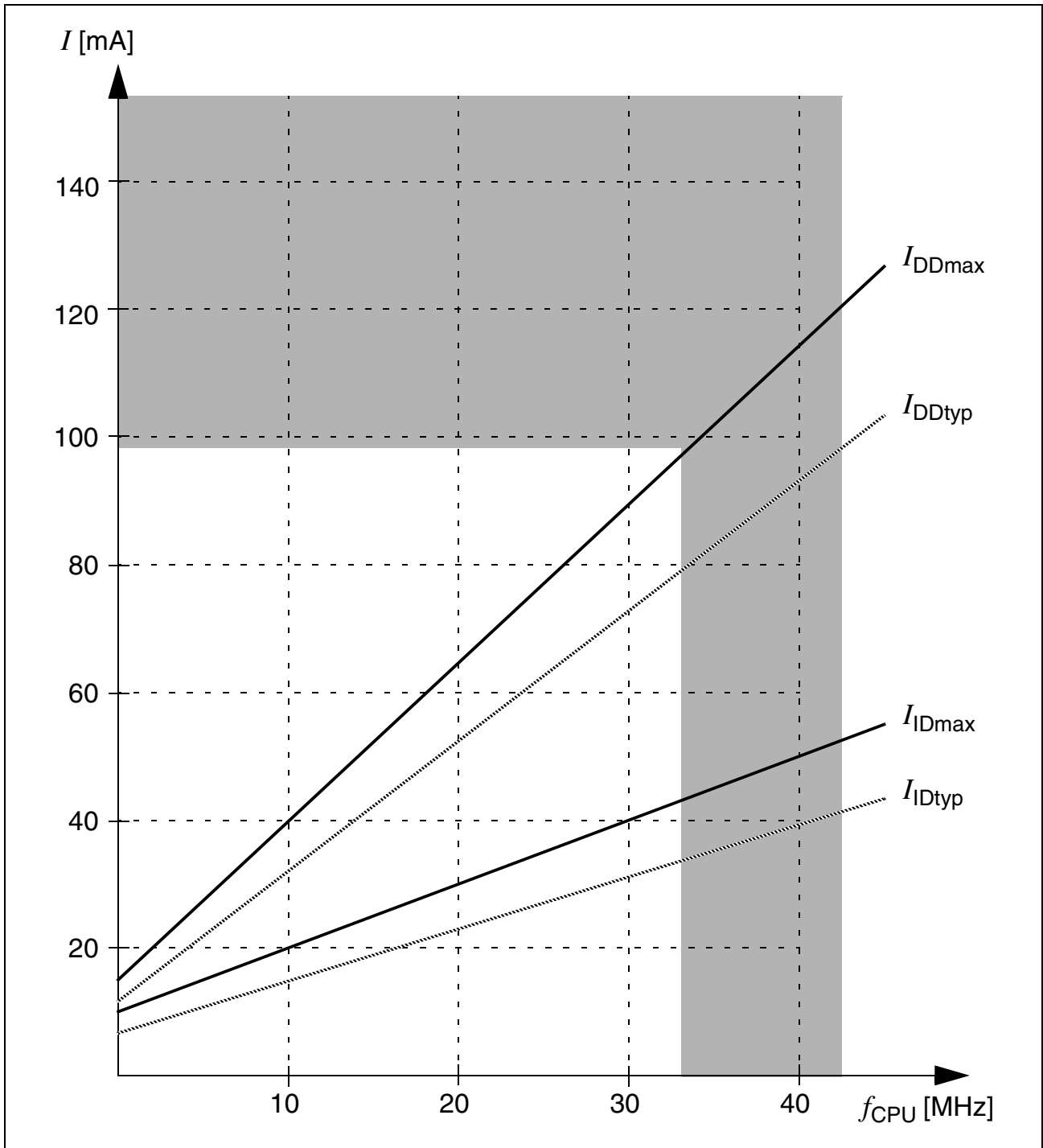


Figure 8 Supply/Idle Current as a Function of Operating Frequency

AC Characteristics

Definition of Internal Timing

The internal operation of the C167CR is controlled by the internal CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see [Figure 9](#)).

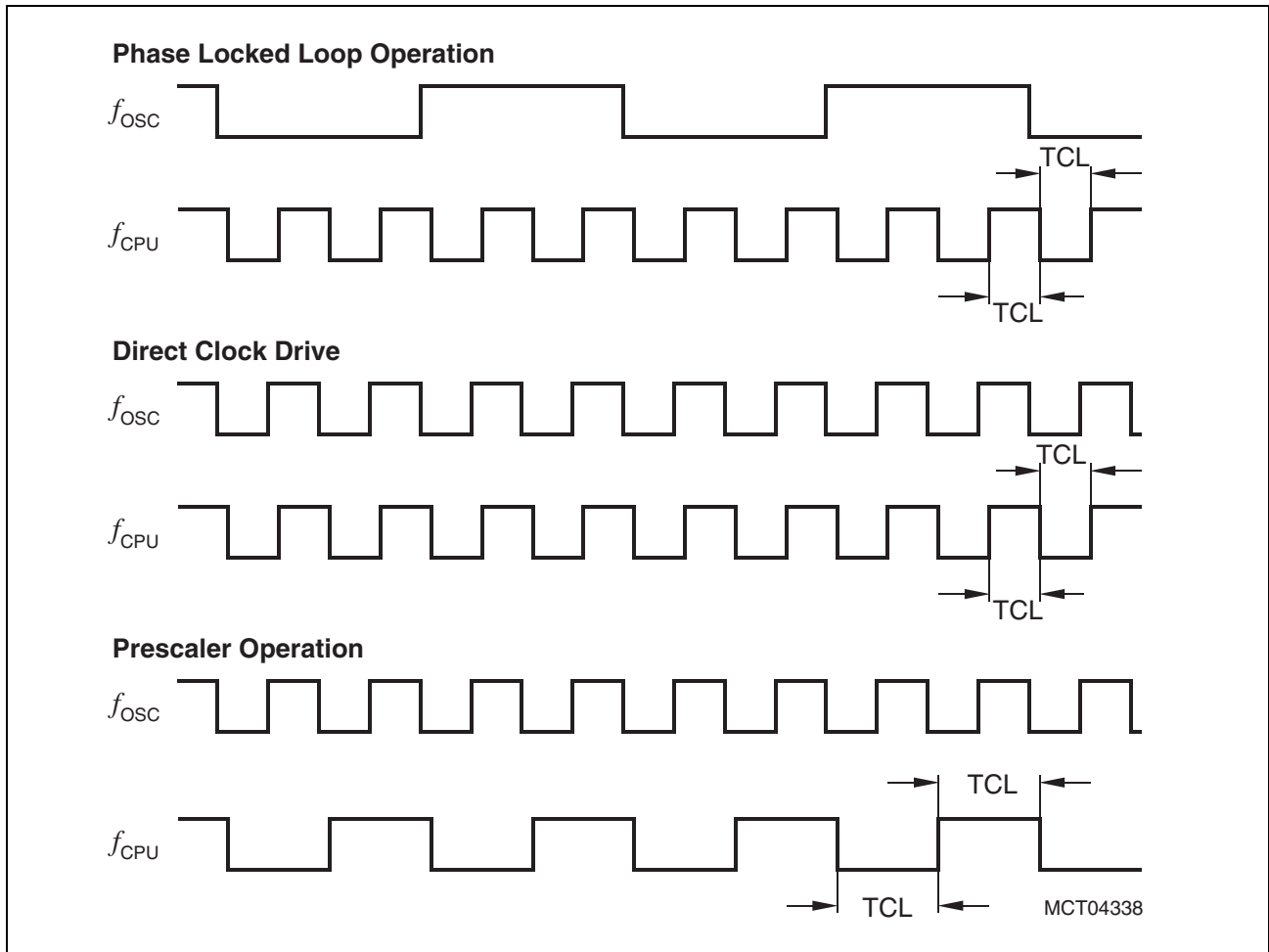


Figure 9 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU} . This influence must be regarded when calculating the timings for the C167CR.

Note: The example for PLL operation shown in [Figure 9](#) refers to a PLL factor of 4.

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5.

Upon a long hardware reset register RP0H is loaded with the logic levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins P0.15-13 (P0H.7-5).

Table 10 associates the combinations of these three bits with the respective clock generation mode.

Table 10 C167CR Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range ¹⁾	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 8.25 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 11 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 16.5 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 6.6 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 33 MHz	Direct drive ²⁾
0 1 0	$f_{OSC} \times 1.5$	6.66 to 22 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 66 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 13.2 MHz	–

¹⁾ The external clock input range refers to a CPU clock range of 10 ... 33 MHz (PLL operation).

²⁾ The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see [Table 10](#)). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times F$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than

for one single TCL (see formula and **Figure 10**).

For a period of $N \times \text{TCL}$ the minimum value is computed using the corresponding deviation D_N :

$$(N \times \text{TCL})_{\min} = N \times \text{TCL}_{\text{NOM}} - D_N \quad D_N [\text{ns}] = \pm(13.3 + N \times 6.3) / f_{\text{CPU}} [\text{MHz}],$$

where N = number of consecutive TCLs and $1 \leq N \leq 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 25 = 1.288 \text{ ns}$, and $(3\text{TCL})_{\min} = 3\text{TCL}_{\text{NOM}} - 1.288 \text{ ns} = 58.7 \text{ ns}$ (@ $f_{\text{CPU}} = 25 \text{ MHz}$).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectable.

*Note: For all periods longer than 40 TCL the $N = 40$ value can be used (see **Figure 10**).*

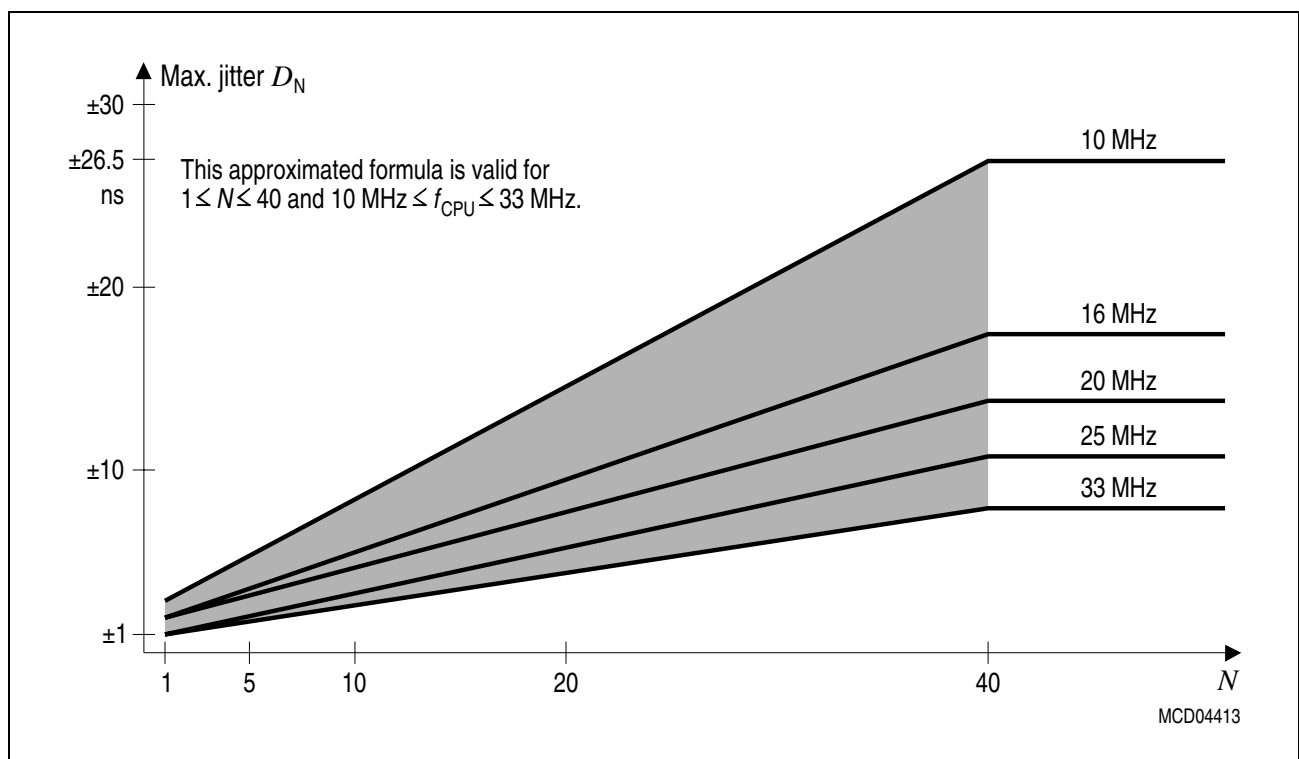


Figure 10 **Approximated Maximum Accumulated PLL Jitter**

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC} .

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$\text{TCL}_{\min} = 1/f_{\text{OSC}} \times \text{DC}_{\min} \quad (\text{DC} = \text{duty cycle})$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{\text{OSC}}$. The minimum value TCL_{\min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, ...). Timings that require an even number of TCLs (2, 4, ...) may use the formula $2\text{TCL} = 1/f_{\text{OSC}}$.

AC Characteristics
External Clock Drive XTAL1

(Operating Conditions apply)

Table 11 External Clock Drive Characteristics

Parameter	Symbol	Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
		min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC} SR	30	–	15	–	45 ¹⁾	500 ¹⁾	ns
High time ²⁾	t_1 SR	15 ³⁾	–	5	–	10	–	ns
Low time ²⁾	t_2 SR	15 ³⁾	–	5	–	10	–	ns
Rise time ²⁾	t_3 SR	–	8	–	5	–	10	ns
Fall time ²⁾	t_4 SR	–	8	–	5	–	10	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .

3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

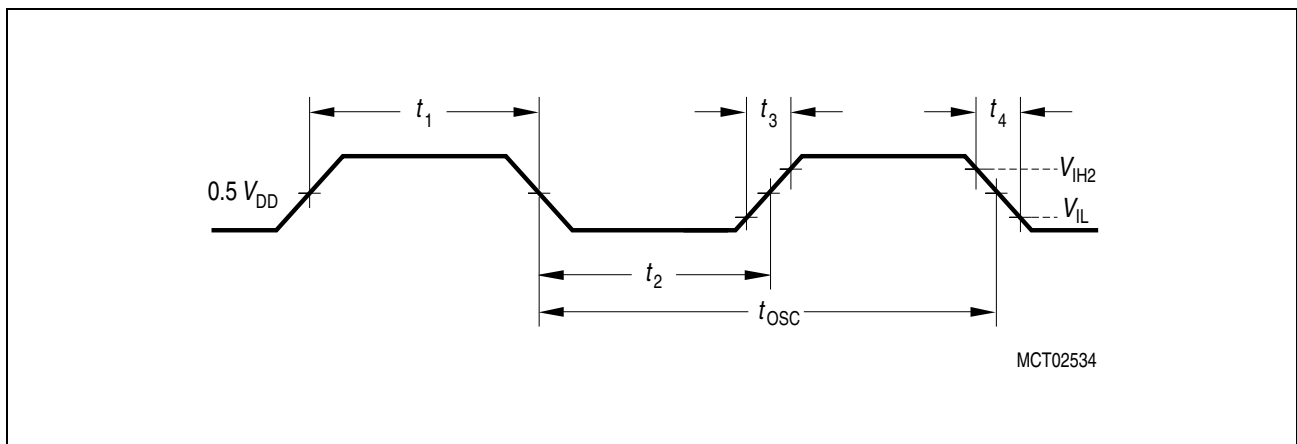


Figure 11 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 40 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is guaranteed by design only (not 100% tested).

A/D Converter Characteristics

(Operating Conditions apply)

Table 12 A/D Converter Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog reference supply	V_{AREF} SR	4.0	$V_{DD} + 0.1$	V	1)
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.1$	$V_{SS} + 0.2$	V	–
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}	0.5	6.25	MHz	3)
Conversion time	t_C CC	–	$40 t_{BC} + t_S + 2t_{CPU}$	–	4) $t_{CPU} = 1/f_{CPU}$
Calibration time after reset	t_{CAL} CC	–	$3328 t_{BC}$	–	5)
Total unadjusted error	TUE CC	–	± 2	LSB	1)
Internal resistance of reference voltage source	R_{AREF} SR	–	$t_{BC} / 60 - 0.25$	k Ω	t_{BC} in [ns] ⁶⁾⁷⁾
Internal resistance of analog source	R_{ASRC} SR	–	$t_S / 450 - 0.25$	k Ω	t_S in [ns] ⁷⁾⁸⁾
ADC input capacitance	C_{AIN} CC	–	33	pF	7)

- 1) TUE is tested at $V_{AREF} = 5.0$ V, $V_{AGND} = 0$ V, $V_{DD} = 4.9$ V. It is guaranteed by design for all other voltages within the defined voltage range.
 If the analog reference supply voltage exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} = V_{DD} + 0.2$ V) the maximum TUE is increased to ± 3 LSB. This range is not 100% tested.
 The specified TUE is guaranteed only if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA.
 During the reset calibration sequence the maximum TUE may be ± 4 LSB.
- 2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.
- 3) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result.
 Values for the basic clock t_{BC} depend on programming and can be taken from [Table 13](#).
 This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.
- 5) During the reset calibration conversions can be executed (with the current accuracy). The time required for these conversions is added to the total reset calibration time.
- 6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.
- 7) Not 100% tested, guaranteed by design and characterization.

- 8) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from [Table 13](#).

Sample time and conversion time of the C167CR's A/D Converter are programmable. [Table 13](#) should be used to calculate the above timings.

The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 13 A/D Converter Computation Table

ADCON.15I14 (ADCTC)	A/D Converter Basic clock f_{BC}	ADCON.13I12 (ADSTC)	Sample time t_S
00	$f_{CPU} / 4$	00	$t_{BC} \times 8$
01	$f_{CPU} / 2$	01	$t_{BC} \times 16$
10	$f_{CPU} / 16$	10	$t_{BC} \times 32$
11	$f_{CPU} / 8$	11	$t_{BC} \times 64$

Converter Timing Example:

Assumptions: $f_{CPU} = 25$ MHz (i.e. $t_{CPU} = 40$ ns), ADCTC = '00', ADSTC = '00'.
 Basic clock $f_{BC} = f_{CPU} / 4 = 6.25$ MHz, i.e. $t_{BC} = 160$ ns.
 Sample time $t_S = t_{BC} \times 8 = 1280$ ns.
 Conversion time $t_C = t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80)$ ns = 7.8 μ s.

Testing Waveforms

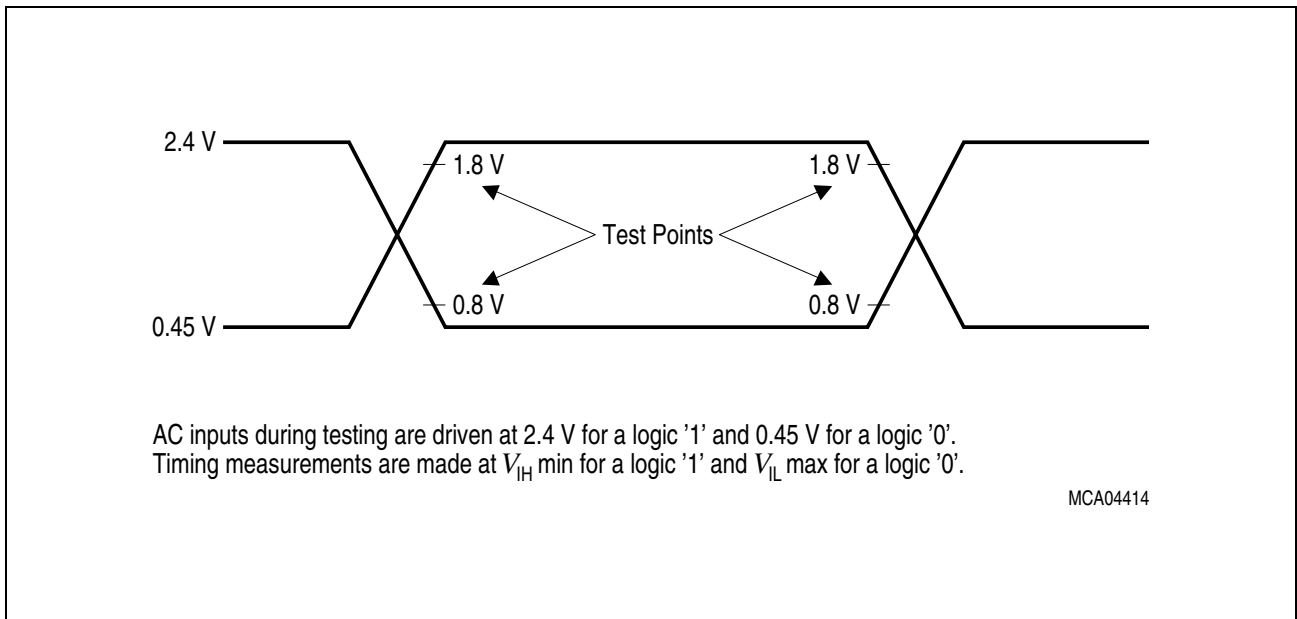


Figure 12 Input Output Waveforms

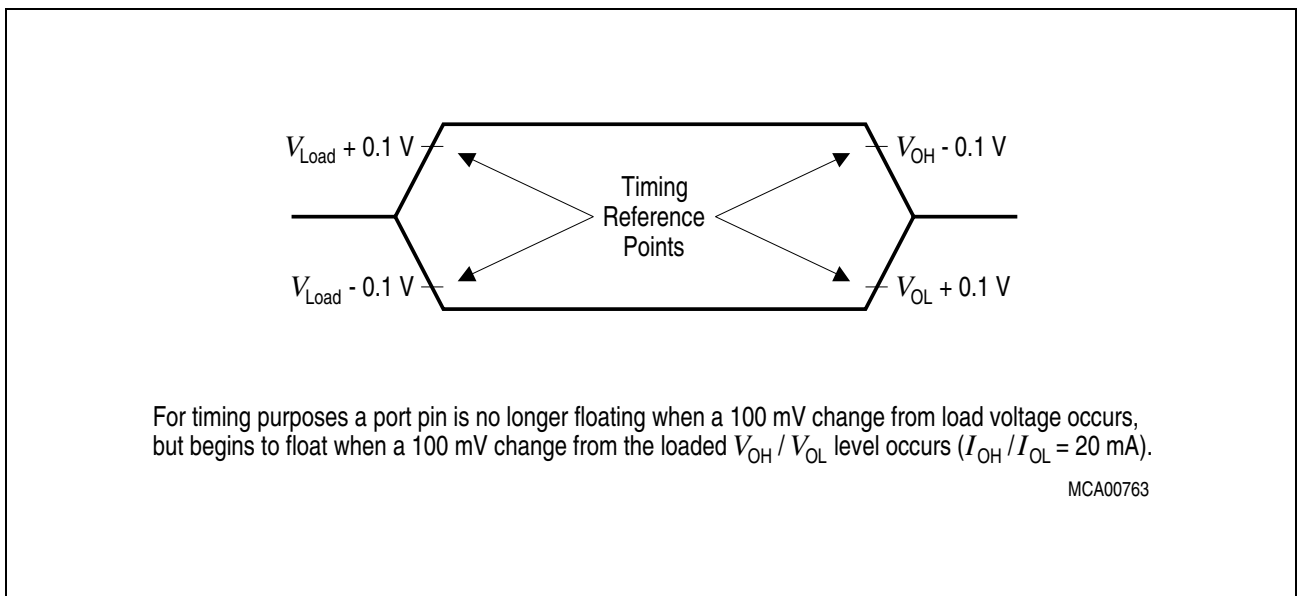


Figure 13 Float Waveforms

AC Characteristics

Table 14 CLKOUT Reference Signal

Parameter	Symbol	Limits		Unit
		min.	max.	
CLKOUT cycle time	t_{C5} CC	30 ¹⁾		ns
CLKOUT high time	t_{C6} CC	8	–	ns
CLKOUT low time	t_{C7} CC	6	–	ns
CLKOUT rise time	t_{C8} CC	–	4	ns
CLKOUT fall time	t_{C9} CC	–	4	ns

¹⁾ The CLKOUT cycle time is influenced by the PLL jitter.
For a single CLKOUT cycle (2 TCL) the deviation caused by the PLL jitter is below 1 ns (for $f_{CPU} > 25$ MHz).
For longer periods the relative deviation decreases (see PLL deviation formula).

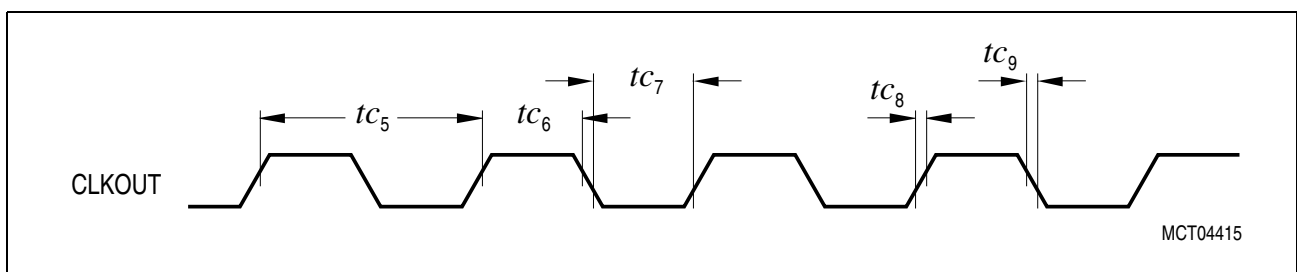


Figure 14 CLKOUT Signal Timing

Variable Memory Cycles

The bus timing shown below is programmable via the BUSCONx registers. The duration of ALE and two types of waitstates can be selected. This table summarizes the possible bus cycle durations.

Table 15 Variable Memory Cycles

Bus Cycle Type	Bus Cycle Duration	Unit	25/33 MHz, 0 Waitstates
Demultiplexed bus cycle with normal ALE	$4 + 2 \times (15 - \langle MCTC \rangle) + 2 \times (1 - \langle MTTC \rangle)$	TCL	80 ns / 60.6 ns
Demultiplexed bus cycle with extended ALE	$6 + 2 \times (15 - \langle MCTC \rangle) + 2 \times (1 - \langle MTTC \rangle)$	TCL	120 ns / 90.9 ns
Multiplexed bus cycle with normal ALE	$6 + 2 \times (15 - \langle MCTC \rangle) + 2 \times (1 - \langle MTTC \rangle)$	TCL	120 ns / 90.9 ns
Multiplexed bus cycle with extended ALE	$8 + 2 \times (15 - \langle MCTC \rangle) + 2 \times (1 - \langle MTTC \rangle)$	TCL	160 ns / 121.2 ns

Table 16 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol	Limits		Unit
		min.	max.	
Output delay from CLKOUT falling edge Valid for: address, $\overline{\text{BHE}}$, early $\overline{\text{CS}}$, write data out, ALE	t_{c10} CC	-2	11	ns
Output delay from CLKOUT rising edge Valid for: latched $\overline{\text{CS}}$, ALE low	t_{c11} CC	-2	6	ns
Output delay from CLKOUT rising edge Valid for: $\overline{\text{WR}}$ low (no RW delay), $\overline{\text{RD}}$ low (no RW delay)	t_{c12} CC	-2	8	ns
Output delay from CLKOUT falling edge Valid for: $\overline{\text{RD}}/\overline{\text{WR}}$ low (with RW delay), $\overline{\text{RD}}$ high (with RW delay)	t_{c13} CC	-2	6	ns
Input setup time to CLKOUT falling edge Valid for: read data in	t_{c14} SR	14	–	ns
Input hold time after CLKOUT falling edge Valid for: read data in ¹⁾	t_{c15} SR	0	–	ns
Output hold time after CLKOUT falling edge Valid for: address, $\overline{\text{BHE}}$, early $\overline{\text{CS}}$ ²⁾	t_{c17} CC	-2	6	ns
Output hold time after CLKOUT edge ³⁾ Valid for: write data out	t_{c18} CC	-2	–	ns
Output delay from CLKOUT falling edge Valid for: $\overline{\text{WR}}$ high	t_{c19} CC	-2	4	ns
Turn off delay after CLKOUT edge ³⁾ Valid for: write data out	t_{c20} CC	–	7	ns
Turn on delay after CLKOUT falling edge ³⁾ Valid for: write data out	t_{c21} CC	-5	–	ns

¹⁾ Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of $\overline{\text{RD}}$. Therefore the read data may be removed immediately after the rising edge of $\overline{\text{RD}}$. Address changes before the end of $\overline{\text{RD}}$ have also no impact on (demultiplexed) read cycles.

²⁾ Due to comparable propagation delays (at comparable capacitive loads) the address does not change before $\overline{\text{WR}}$ goes high. The minimum output delay ($t_{c17\text{min}}$) is therefore the actual value of t_{c19} .

³⁾ Not 100% tested, guaranteed by design and characterization.

General Notes For The Following Timing Figures

These standard notes apply to all subsequent timing figures. Additional individual notes are placed at the respective figure.

- 1) The falling edge of signals \overline{RD} and $\overline{WR}/\overline{WRH}/\overline{WRL}/\overline{WrCS}$ is controlled by the Read/Write delay feature (bit BUSCON.RWDCx).
- 2) A bus cycle is extended here, if MCTC waitstates are selected or if the \overline{READY} input is sampled inactive.
- 3) A bus cycle is extended here, if an MTTC waitstate is selected.

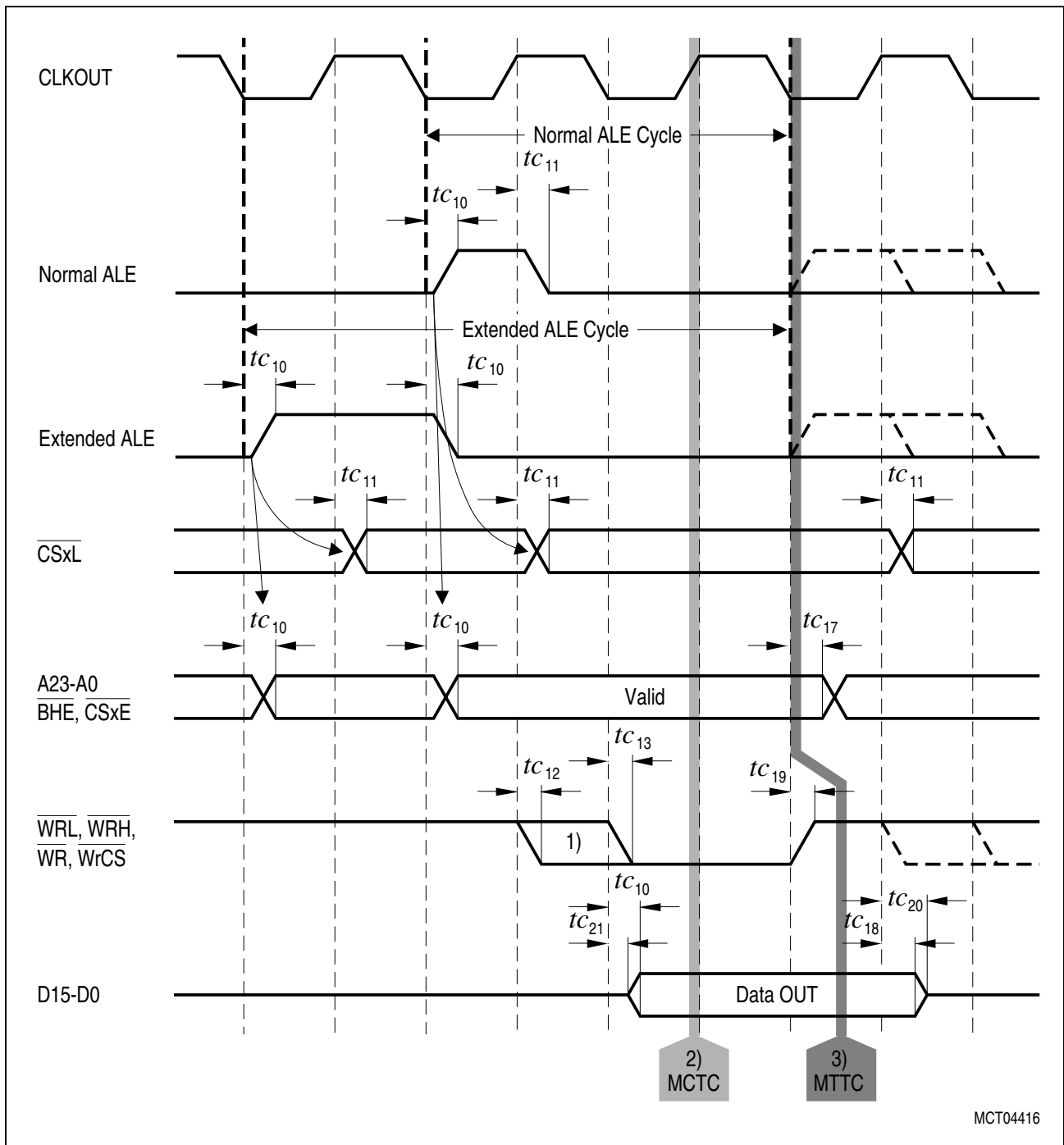
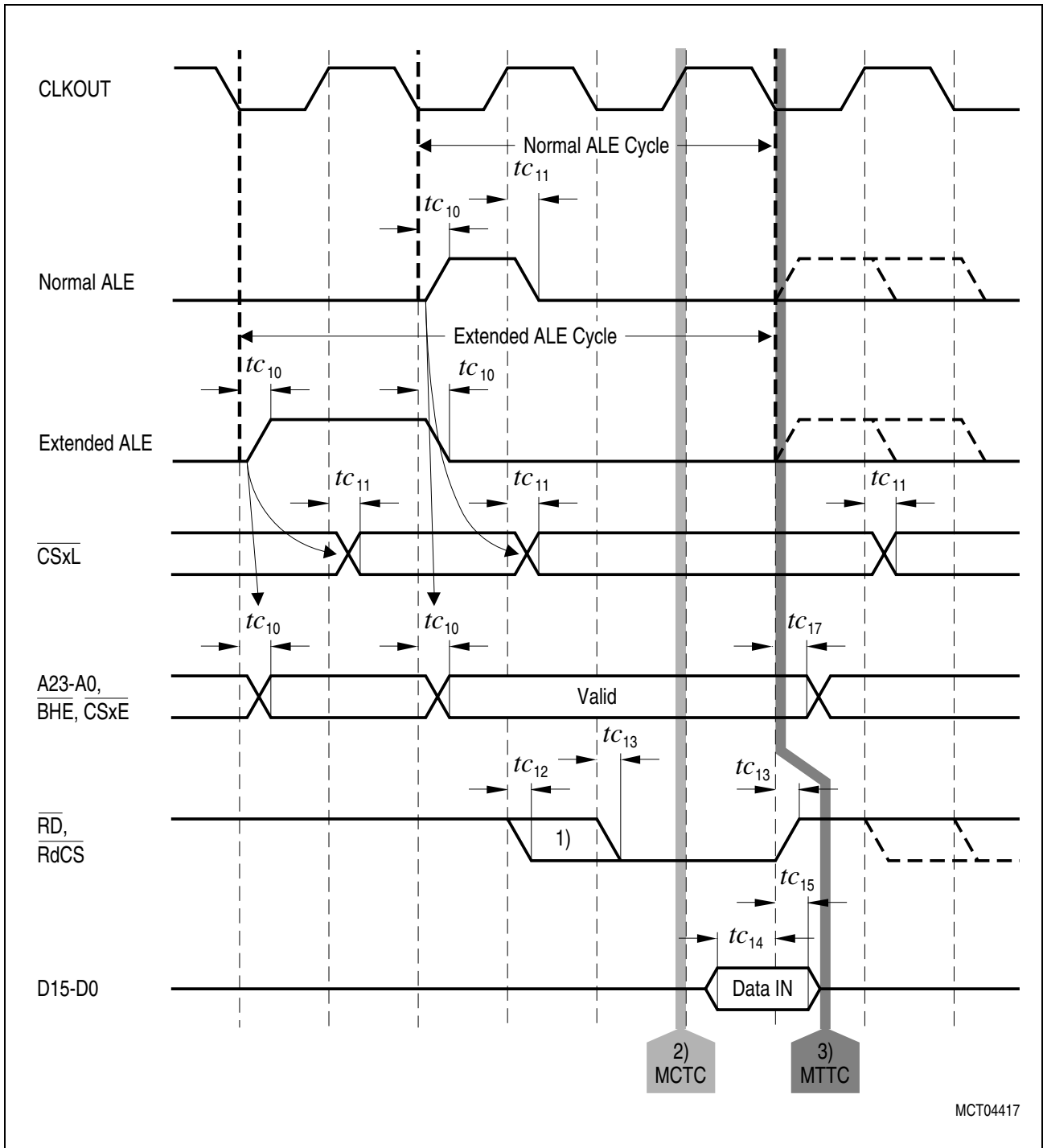


Figure 15 Demultiplexed Bus, Write Access



MCT04417

Figure 16 Demultiplexed Bus, Read Access

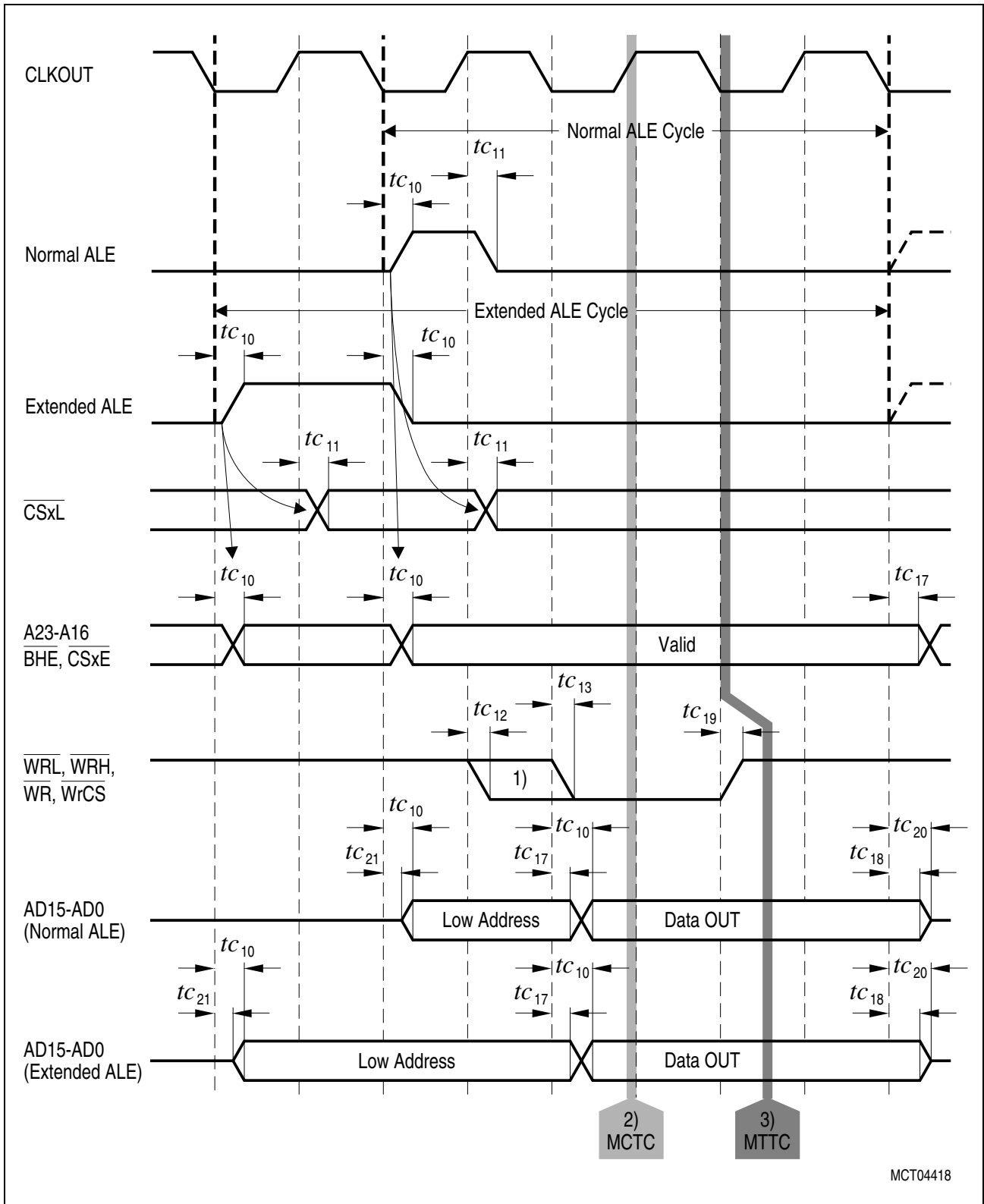


Figure 17 Multiplexed Bus, Write Access

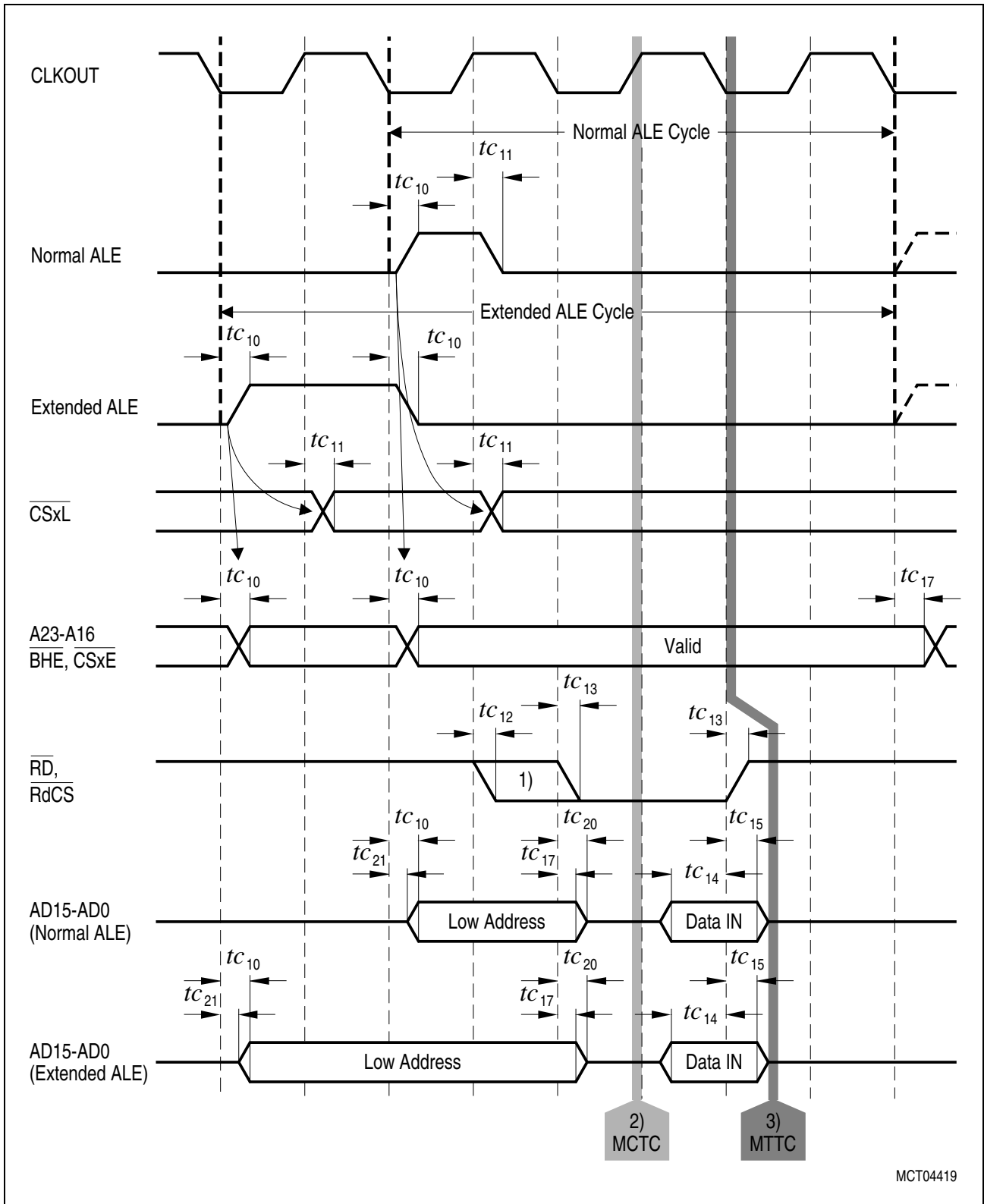


Figure 18 Multiplexed Bus, Read Access

Bus Cycle Control via $\overline{\text{READY}}$ Input

The duration of an external bus cycle can be controlled by the external circuitry via the $\overline{\text{READY}}$ input signal.

Synchronous $\overline{\text{READY}}$ permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous $\overline{\text{READY}}$ puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage.

Table 17 $\overline{\text{READY}}$ Timing (Operating Conditions apply)

Parameter	Symbol	Limits		Unit
		min.	max.	
Input setup time to CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	t_{c25} CC	12	–	ns
Input hold time after CLKOUT rising edge Valid for: $\overline{\text{READY}}$ input	t_{c26} CC	0	–	ns
Asynchronous $\overline{\text{READY}}$ input low time ⁶⁾	t_{c27} CC	$t_{c5} + t_{c25}$	–	ns

Notes (Valid also for [Figure 19](#))

- 4) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 5) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a $\overline{\text{READY}}$ controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
- 6) These timings are given for test purposes only, in order to assure recognition at a specific clock edge. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT, it must fulfill t_{c27} in order to be safely synchronized. Proper deactivation of $\overline{\text{READY}}$ is guaranteed if $\overline{\text{READY}}$ is deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
- 7) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus **with** MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus **without** MTTC waitstate this delay is zero.
- 8) If the next following bus cycle is $\overline{\text{READY}}$ controlled, an active $\overline{\text{READY}}$ signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the MTTC waitstate of the current cycle, and on the MCTC waitstates and the ALE mode of the next following cycle. If the current cycle uses a multiplexed bus the intrinsic MUX waitstate adds another CLKOUT cycle to the $\overline{\text{READY}}$ deactivation time.

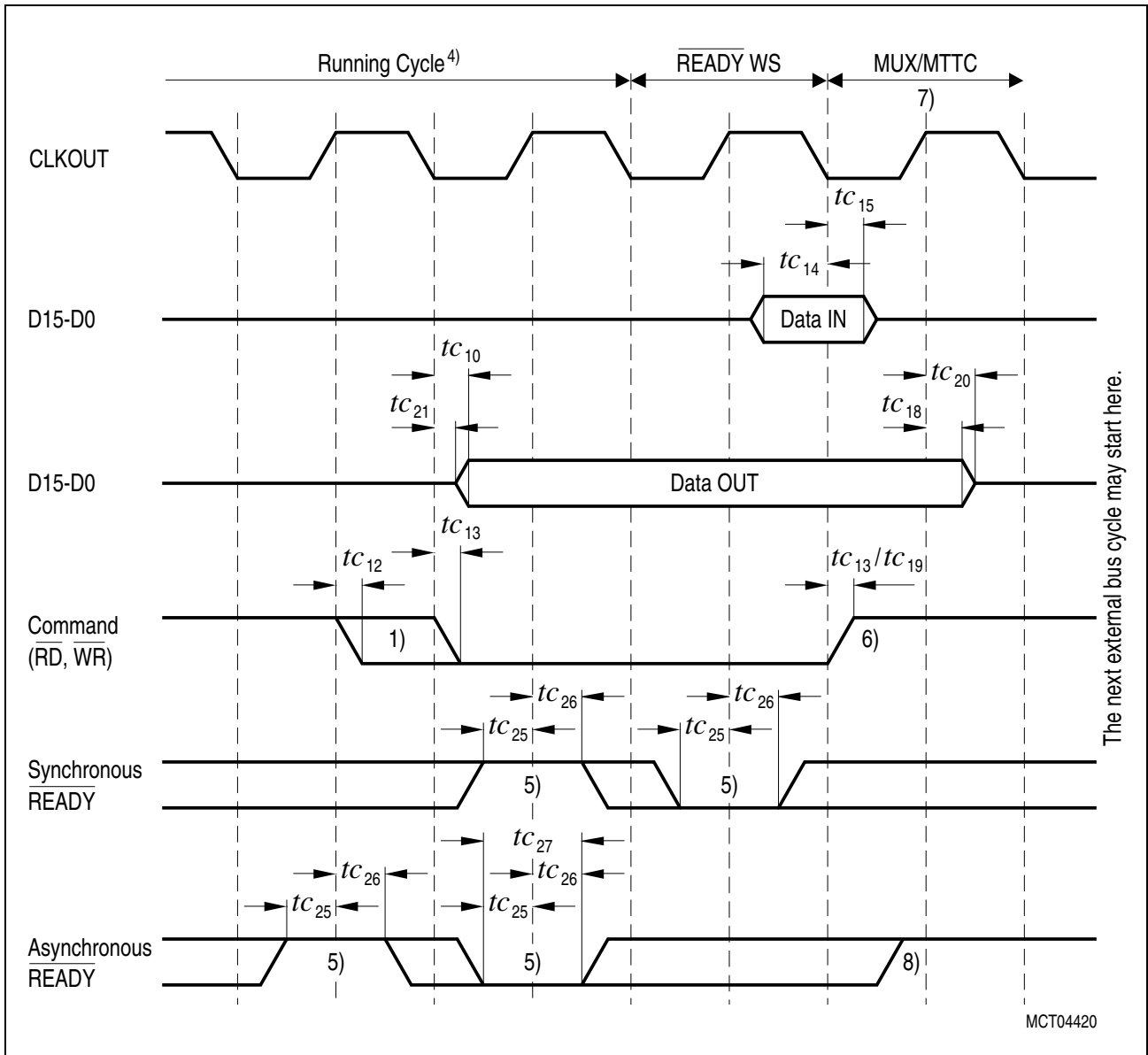


Figure 19 $\overline{\text{READY}}$ Timings

External Bus Arbitration

Table 18 Bus Arbitration Timing (Operating Conditions apply)

Parameter	Symbol	Limits		Unit
		min.	max.	
HOLD input setup time to CLKOUT falling edge	t_{c28} SR	18	–	ns
CLKOUT to $\overline{\text{BREQ}}$ delay	t_{c29} CC	-4	6	ns
CLKOUT to $\overline{\text{HLDA}}$ delay	t_{c30} CC	-4	6	ns
$\overline{\text{CSx}}$ release ¹⁾	t_{c31} CC	0	10	ns
$\overline{\text{CSx}}$ drive	t_{c32} CC	-2	6	ns
Other signals release ¹⁾	t_{c33} CC	0	10	ns
Other signals drive ¹⁾	t_{c34} CC	0	6	ns

¹⁾ Not 100% tested, guaranteed by design and characterization.

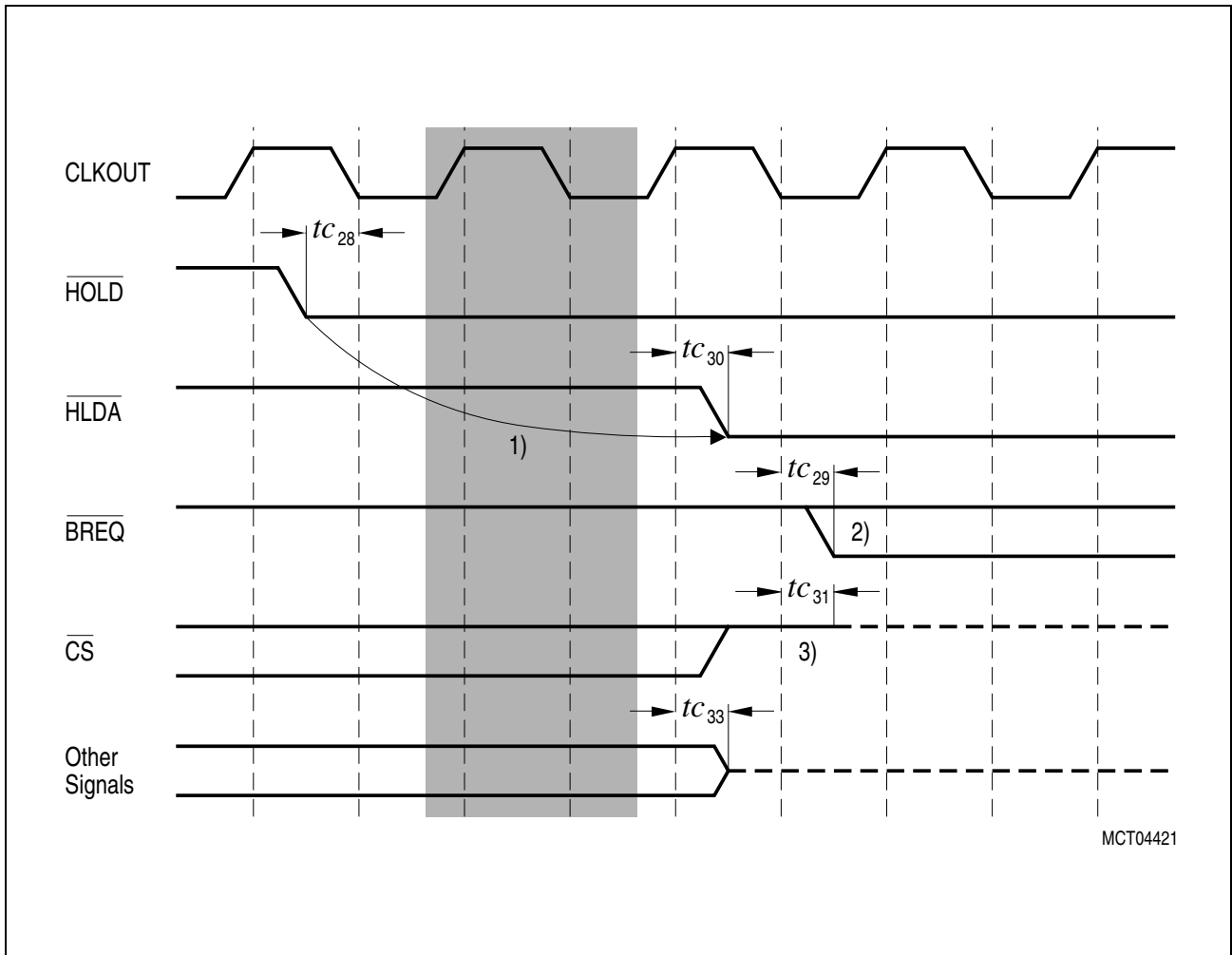


Figure 20 External Bus Arbitration, Releasing the Bus

Notes

- 1) The C167CR will complete the currently running bus cycle before granting bus access.
- 2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
- 3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{33} . Latched $\overline{\text{CS}}$ outputs are driven high for 1 TCL before the output drivers are switched off.

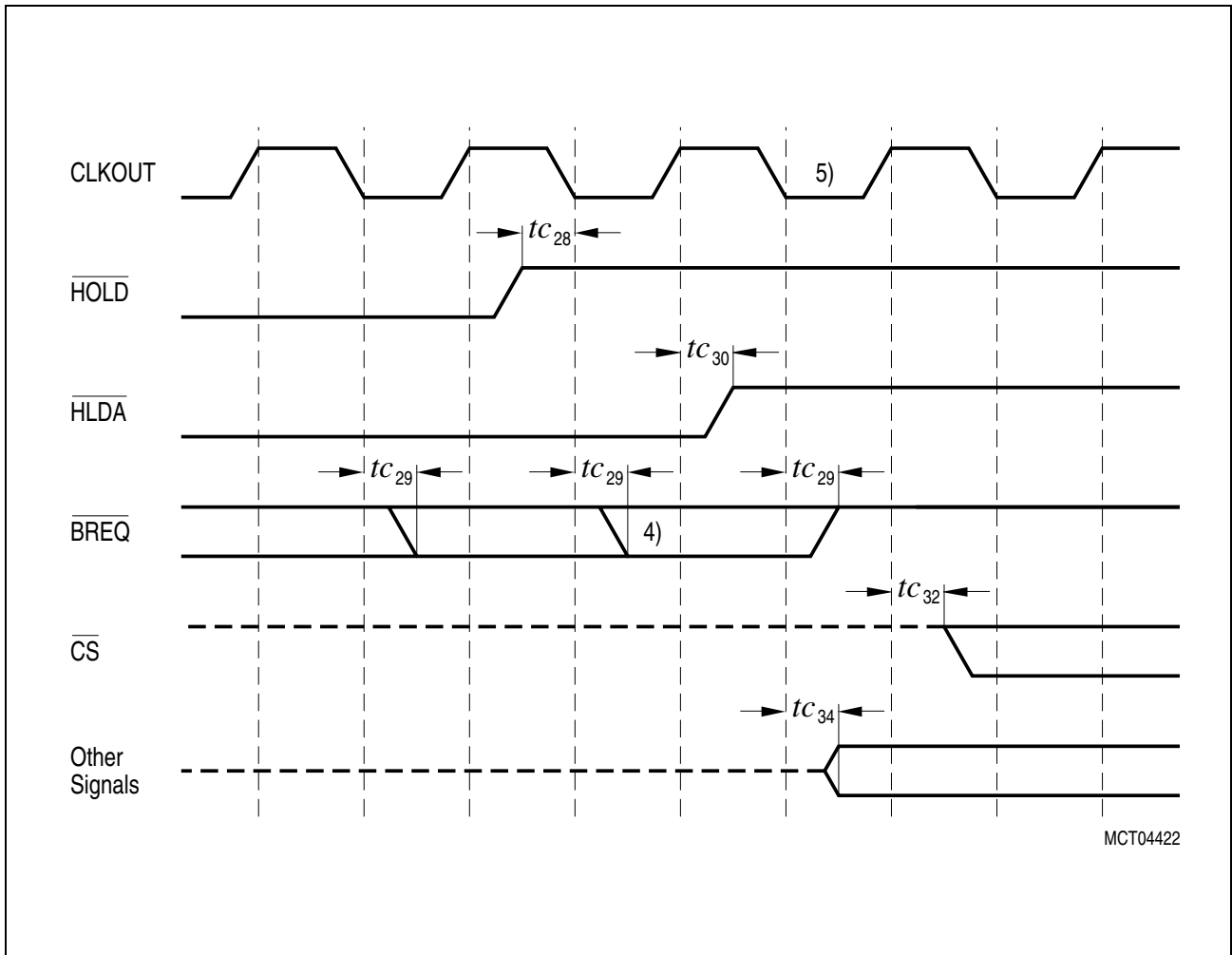


Figure 21 External Bus Arbitration, (Regaining the Bus)

Notes

- 4) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be deactivated without the C167CR requesting the bus.
- 5) The next C167CR driven bus cycle may start here.

External XRAM Access

If XPER-Share mode is enabled the on-chip XRAM of the C167CR can be accessed (during hold states) by an external master like an asynchronous SRAM.

Table 19 XRAM Access Timing (Operating Conditions apply)¹⁾

Parameter	Symbol	Limits		Unit	
		min.	max.		
Address setup time before $\overline{RD}/\overline{WR}$ falling edge	t_{40} SR	4	–	ns	
Address hold time after $\overline{RD}/\overline{WR}$ rising edge	t_{41} SR	0	–	ns	
Data turn on delay after \overline{RD} falling edge	Read t_{42} CC	1	–	ns	
Data output valid delay after address latched		t_{43} CC	–	40	ns
Data turn off delay after \overline{RD} rising edge		t_{44} CC	1	14	ns
Write data setup time before \overline{WR} rising edge	Write t_{45} SR	10	–	ns	
Write data hold time after \overline{WR} rising edge		t_{46} SR	2	–	ns
\overline{WR} pulse width		t_{47} SR	20	–	ns
\overline{WR} signal recovery time		t_{48} SR	t_{40}	–	ns

¹⁾ The minimum access cycle time is 60 ns.

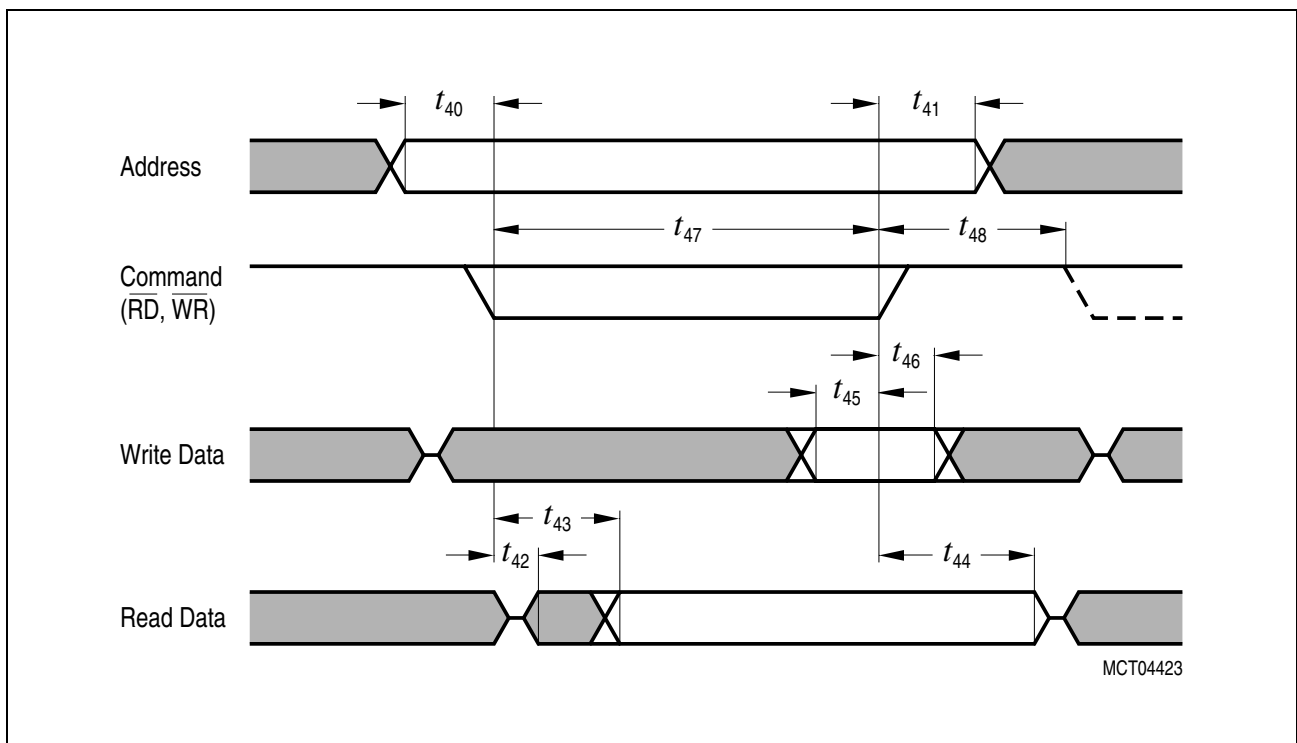
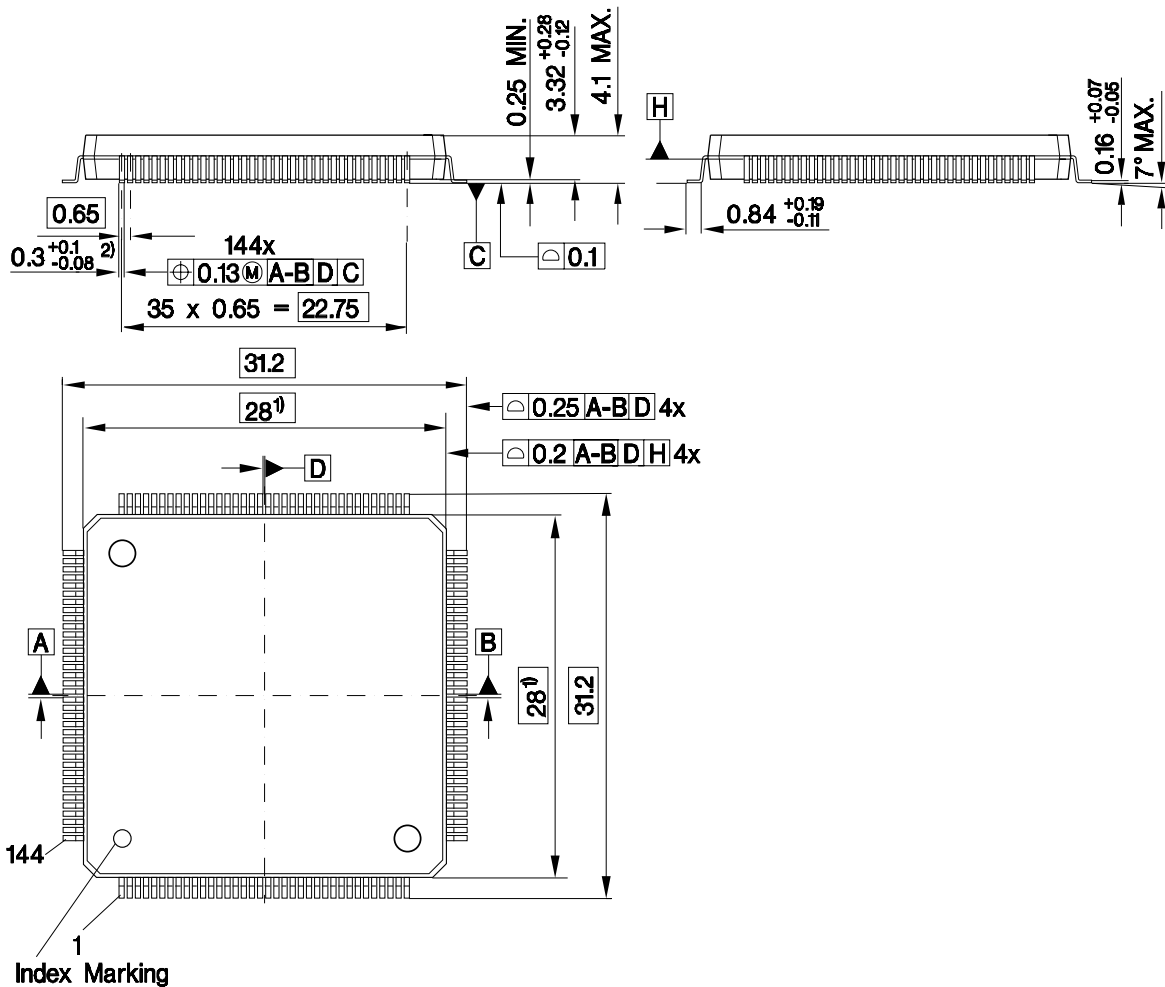


Figure 22 External Access to the XRAM

Package Outlines

P-MQFP-144-6

(Plastic Metric Quad Flat Package)



- 1) Does not include plastic or metal protrusion of 0.25 max. per side
- 2) Does not include dambar protrusion of 0.08 max. per side

GPM09391

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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