



SANYO Semiconductors

DATA SHEET

LV51134T — CMOS IC 2-Cell Lithium-Ion Secondary Battery Protection IC

Overview

The LV51134T is a protection IC for 2-cell lithium-ion secondary batteries.

Features

- Monitoring function for each cell: Detects overcharge and over-discharge conditions and controls the charging and discharging operation of each cell.
- High detection voltage accuracy: Over-charge detection accuracy $\pm 25\text{mV}$
Over-discharge detection accuracy $\pm 100\text{mV}$
- Hysteresis cancel function: The hysteresis of over-discharge detection voltage is canceled by sensing the connection of a load after overcharging has been detected.
- Discharge current monitoring function: Detects over-currents, load shorting, and excessively high voltage of a charger and regulates charging and discharging operations.
- Low current consumption: Normal operation mode typ. $6.0\mu\text{A}$
Stand by mode max. $0.2\mu\text{A}$
- 0V cell charging function: Charging is enabled even when the cell voltage is 0V by giving a potential difference between the V_{DD} pin and V⁻ pin.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LV51134T

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{DD}		-0.3 to +12	V
Input voltage Charger minus voltage	V ⁻		V _{DD} -28 to V _{DD} +0.3	V
Output voltage	Cout pin voltage	V _{cout}	V _{DD} -28 to V _{DD} +0.3	V
	Dout pin voltage	V _{dout}	V _{SS} -0.3 to V _{DD} +0.3	V
Allowable power dissipation	P _{d max}	Independent IC	170	mW
Operating ambient temperature	T _{opr}		-30 to +80	°C
Storage temperature	T _{stg}		-40 to +125	°C

Electrical Characteristics at Ta = 25°C, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation input voltage	V _{cell}	Between V _{DD} and V _{SS}	1.5		10	V
0V cell charging minimum operation voltage	V _{min}	Between V _{DD} -V _{SS} =0 and V _{DD} -V ⁻			1.5	V
Over-charge detection voltage	V _{d1}		4.225	4.250	4.275	V
Over-charge reset voltage	V _{h1}		4.000	4.050	4.100	V
Over-charge detection delay time	t _{d1}	V _{DD} -V _c =3.5V→4.5V, V _c -V _{SS} =3.5V	0.5	1.0	1.5	s
Over-charge reset delay time	t _{r1}	V _{DD} -V _c =4.5V→3.5V, V _c -V _{SS} =3.5V	20.0	40.0	60.0	ms
Over-discharge detection voltage	V _{d2}		2.40	2.50	2.60	V
Over-discharge reset hysteresis voltage	V _{h2}		10.0	20.0	44.0	mV
Over-discharge detection delay time	t _{d2}	V _{DD} -V _c =3.5V→2.2V, V _c -V _{SS} =3.5V	50	100	150	ms
Over-discharge reset delay time	t _{r2}	V _{DD} -V _c =2.2V→3.5V, V _c -V _{SS} =3.5V	0.5	1.0	1.5	ms
Over-current detection voltage	V _{d3}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	0.170	0.200	0.230	V
Over-current reset hysteresis voltage	V _{h3}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	5.0	10.0	20.0	mV
Over-current detection delay time	t _{d3}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	10.0	20.0	30.0	ms
Over-current reset delay time	t _{r3}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	0.5	1.0	1.5	ms
Short circuit detection voltage	V _{d4}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	1.0	1.3	1.6	V
Short circuit detection delay time	t _{d4}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	0.4	1.0	1.6	ms
Over-charger detection voltage	V _{d5}	Between V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V (V ⁻)-V _{SS}	-0.60	-0.45	-0.30	V
Overcharge reset hysteresis voltage	V _{h5}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	25.0	50.0	100.0	mV
Standby reset voltage	V _{stb}	Between V _{DD} -V _c =2.0V, V _c -V _{SS} =2.0V (V ⁻)-V _{SS}	V _{DD} ×0.4	V _{DD} ×0.5	V _{DD} ×0.6	V
Excessively high voltage charger detection delay time	t _{d5}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V	0.5	1.5	3.0	ms
Excessively high voltage charger reset delay time	t _{r5}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V *	0.5	1.5	3.0	ms
Reset resistance (connected to V _{DD})	R _{DD}		100	200	400	kΩ
Reset resistance (connected to V _{SS})	R _{SS}		15	30	60	kΩ
Cout Nch ON voltage	V _{OL1}	I _{OL} =50μA, V _{DD} -V _c =4.4V, V _c -V _{SS} =4.4V			0.5	V
Cout Pch ON voltage	V _{OH1}	I _{OL} =50μA, V _{DD} -V _c =3.9V, V _c -V _{SS} =3.9V	V _{DD} -0.5			V
Dout Nch ON voltage	V _{OL2}	I _{OL} =50μA, V _{DD} -V _c =2.2V, V _c -V _{SS} =2.2V			0.5	V
Dout Pch ON voltage	V _{OH2}	I _{OL} =50μA, V _{DD} -V _c =3.9V, V _c -V _{SS} =3.9V	V _{DD} -0.5			V
V _c input current	I _{vc}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V		0.0	1.0	μA
Current drain	I _{DD}	V _{DD} -V _c =3.5V, V _c -V _{SS} =3.5V		6.0	13.0	μA
Standby current	I _{stb}	V _{DD} -V _c =2.2V, V _c -V _{SS} =3.5V			0.2	μA

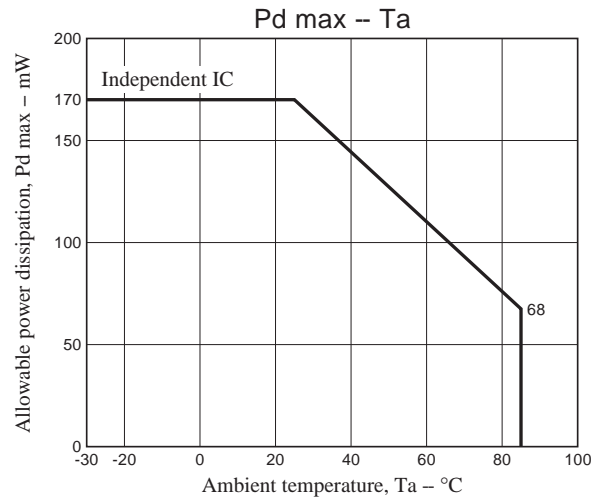
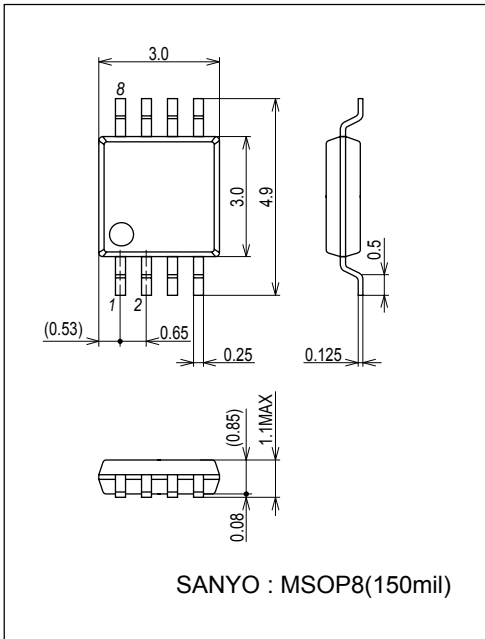
* Upon connecting to charger upon over-discharge, the delay time after recovery from over-discharge.

LV51134T

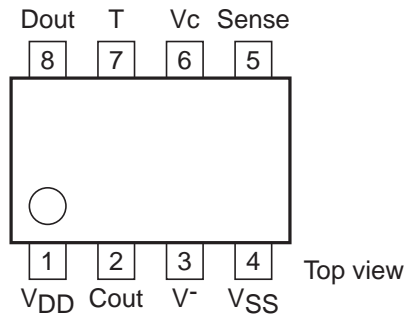
Package Dimensions

unit : mm (typ)

3245B



Pin Assignment

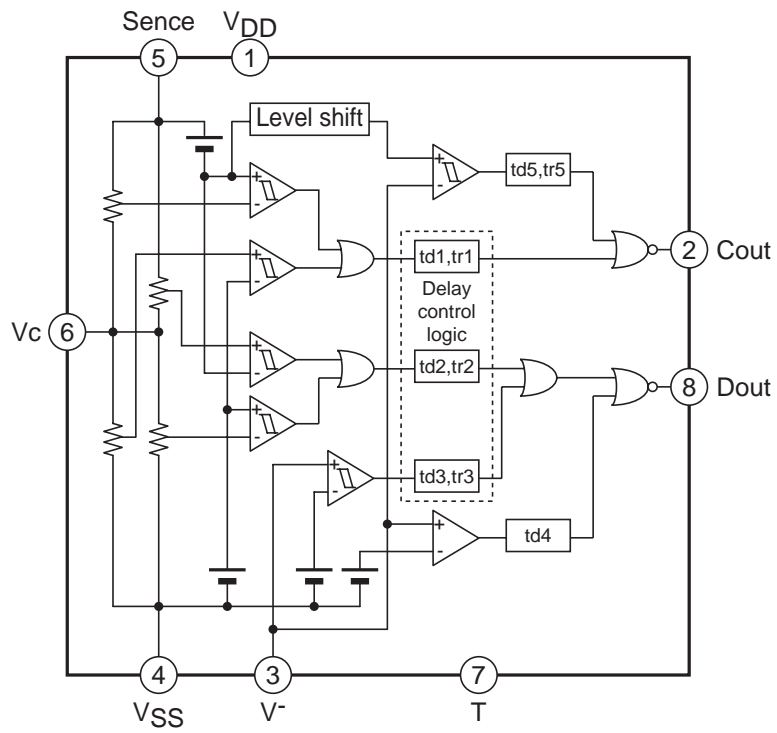


Pin Functions

Pin No.	Symbol	Description
1	V _{DD}	V _{DD} pin
2	Cout	Overcharge detection output pin
3	V ⁻	Charger minus voltage input pin
4	V _{SS}	V _{SS} pin
5	Sense	Sense pin
6	V _c	Intermediate voltage input pin
7	T	Pin to shorten detection time (open under normal condition)
8	Dout	Overdischarge detection output pin

LV51134T

Block Diagram



Functional Description

Over-charge detection

If either of the cell voltage is equal to or more than the over-charge detection voltage, stop further charging by turning “L” the Cout pin and turning off external Nch MOS FET after the over-charge detection delay time. This delay time is set by the internal counter.

The over-charge detection comparator has the hysteresis function. Note that this hysteresis can be cancelled by connecting the load after detection of over-charge detection.

Once over-charge detection is made, over-current detection is not made to prevent malfunction. Note that short-circuit can be detected.

Over-charge return

If charger is connected and both cell voltages become equal to or lower than the over-charge recovery voltage or over-charge detection voltage when load is connected, the Cout pin returns to “H” after the over-charge recovery delay time set by the internal counter.

When load is connected and either cell or both cell voltages are equal to or more than the over-charge detection voltage, the Cout pin does not return to “H.” When the load current is passed through the external Cout pin parasite diode of Nch MOS FET after the over-charge recovery delay time and each cell voltage becomes equal to or below over-charge detection voltage, the Cout returns to “H.”

However, high voltage charger is connected as mentioned below, Cout pin does not return to “H” because over-charger detection sequence starts after over-charge recovery.

Over-discharge detection

When either cell voltage is equal to or below over-discharge voltage, stop further discharge by turning “L” the Dout pin and turning off external Nch MOS FET after the over-charge detection delay time.

The IC becomes standby state after detecting over-discharge and its consumption current is kept at about 0A. After detection, the V⁻ pin will be connected to V_{DD} pin via 200kΩ.

Over-discharge return

Return from over-discharge is made by connecting charger. If the V⁻ pin voltage becomes equal to or lower than the standby return voltage by connecting charger after detecting over-discharge, it returns from the standby state to start cell voltage monitoring. If both voltages become equal to or more than the over-discharge detection voltage by charging, the Dout pin returns to “H” after the over-discharge return delay time set by the internal counter.

Over-current detection

When high current is passed through the battery, the V potential rises by the ON resistor of external MOS FET and becomes equal to or more than the over-current detection voltage, that will be deemed over-current state. Turn “L” the Dout pin after the over-current detection delay time and turn off the external Nch MOS FET to prevent high current in the circuit. The delay time is set by the internal counter. After detection, the V⁻ pin will be connected to V_{SS} via 30kΩ. It will not go into standby state after detecting over-current.

Short circuit detection

If greater discharge current is passed and the V⁻ pin voltage becomes equal to or more than the short-circuit detection voltage, it will go into short-circuit detection state after the short circuit delay time shorter than the over-current detection delay time. When short-circuit is detected, just like the time of over-current detection, turn Dout pin “L” and turn off external Nch MOS FET to prevent high current in the circuit. The V⁻ pin will be connected to V_{SS} after detection via 30kΩ. It will not go into standby state after detecting short-circuit.

Over-current/short-detection return

After detecting over-current or short circuit, the return resistor (typ.30kΩ) between V⁻ pin and V_{SS} pin becomes effective and if the resistor is opened the V⁻ pin voltage will be pulled by the V_{SS} pin voltage. Thereafter, the IC will return from the over-current/short-circuit detection state when the V⁻ pin voltage becomes equal to or below the over-current detection voltage and the Dout pin returns to “H” after over-current return delay time set by the internal counter.

Over-charger detection/return

If the potential difference between V⁻ pin and V_{SS} pin becomes equal to or below the over-charger detection voltage by connecting a charger, no charging can be made by turning “L” the Cout pin after certain delay time and turning off the external Nch MOS FET. If this difference returns to equal to or more than the over-charger detection voltage during detection delay time, the over-charger detection will be stopped. If the potential difference between V⁻ pin and V_{SS} pin becomes equal to or more than the over-charger detection voltage after over-charger detection, the Cout returns to “H” after certain time. The detection/return delay time is set internally.

If Dout pin is “L” charging will be made through the external Nch FET parasite diode of Dout pin. In that case, the potential difference between V⁻ pin and V_{SS} pin becomes -V_f which is equal to or less than the over-charger detection voltage, no over-charger detection will be made during over-discharge, over-current or short-circuit detection. Further, if over-discharged battery is connected to over-charger, no over-charger detection is made while the Dout pin is “L.”

If the battery voltage rises to the over-discharge detection voltage through the parasite diode and the Dout pin becomes “H”, and the potential difference between V⁻ pin and V_{SS} pin is equal to or below the over-charger detection voltage, the delay operation will be started after Dout pin becoming “H.”

0V cell charge

If the cell voltage is 0V but a potential difference between V_{DD} and V becomes equal to or greater than the 0V cell charging lowest operation voltage, the Cout pin will output “H” and enable charging.

Test time reduction function

By turning T pin to the V_{DD} potential, the delay times set by the counter can be cut. Normal time settings if T pin is open. Delay time not set by the counter cannot be controlled by this pin.

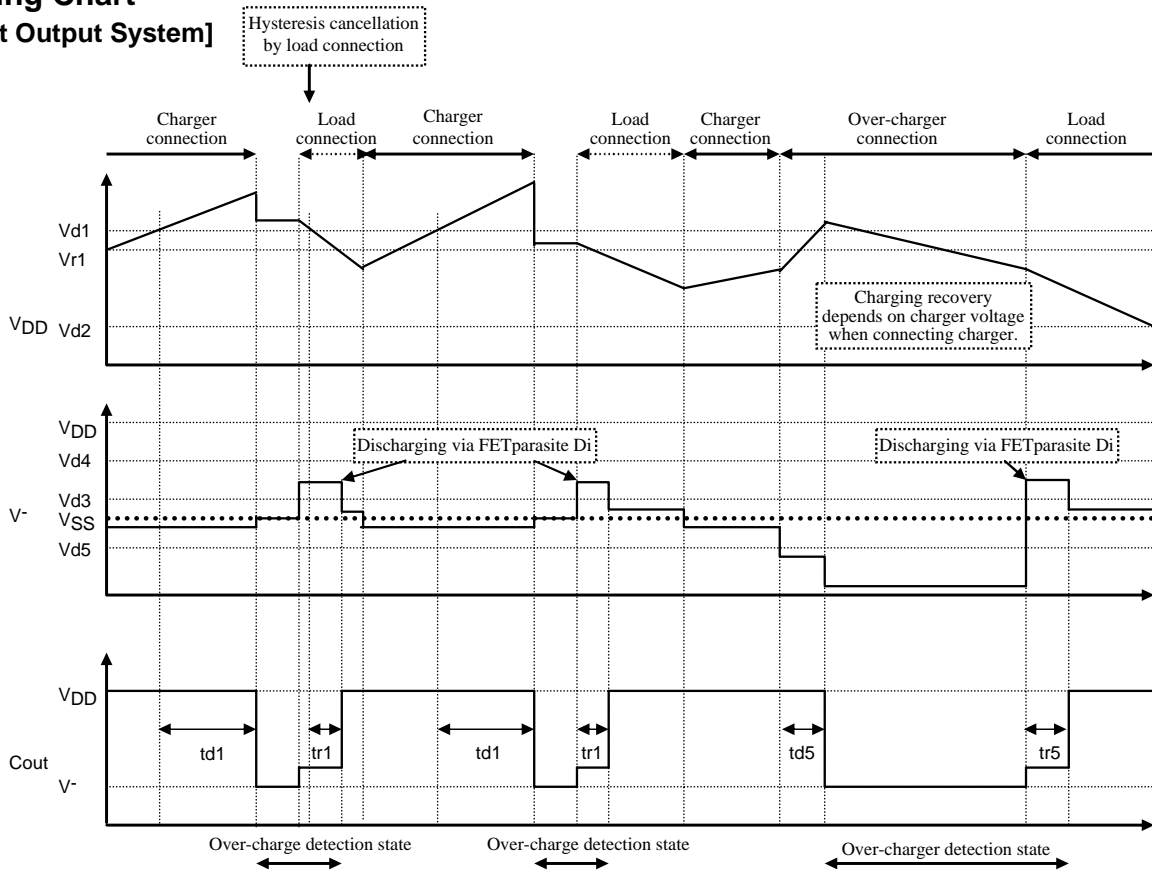
Operation in case of detection overlap

Overlap state		Operation in case of detection overlap	State after detection
When, during over-charge detection,	Over-discharge detection is made,	Over-charge detection is preferred. If over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	When over-charge detection is made first, V ⁻ is released. When over-discharge is detected after over-charge detection, the standby state is not effectuated. Note that V ⁻ is connected to V _{DD} via 200kΩ.
	Over-current detection is made,	(*1) Both detections' can be made in parallel. Over-charge detection continues even when the over-current state occurs. If the over-charge state occurs first, over-current detection is interrupted.	(*2) When over-current is detected first, V ⁻ is connected to V _{SS} via 30kΩ. When over-charge detection is made first, V ⁻ is released.
When, during over-discharge detection,	Over-charge detection is made,	Over-discharge detection is interrupted and over-charge detection is preferred. When over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	The standby state is not effectuated when over-discharge detection is made after over-charge detection. Note that V ⁻ is connected to V _{DD} via 200kΩ.
	Over-current detection is made,	(*3) Both detections can be made in parallel. Over-discharge detection continues even when the over-current state is effectuated first. Over-current detection is interrupted when the over-discharge state is effectuated first,	(*4) If over-current is detected in advance, V will be connected to V _{SS} via 30kΩ. After detecting over-discharge, V will be connected to V _{DD} via 200kΩ to get into standby state. If over-discharge is detected in advance, V will be connected to V _{DD} via 200kΩ to get into standby state.
When, during over-current detection,	Over-charge detection is made,	(*1)	(*2)
	Over-discharge detection is made,	(*3)	(*4)

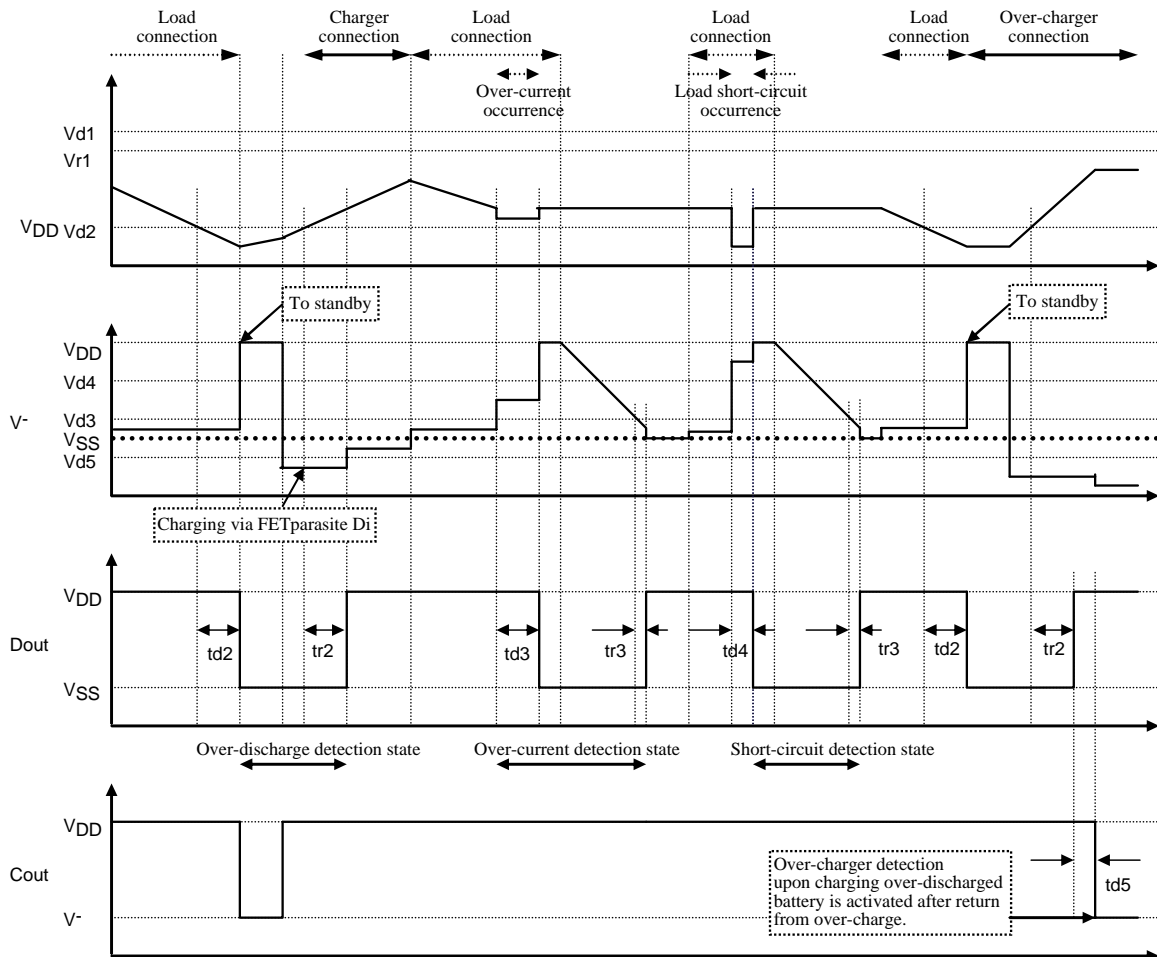
(Note) Short-circuit detection can be made independently.

Over-charger detection does not work during over-discharge, over-current or short-circuit detection and the delay time starts after return from these states.

Timing Chart
[Cout Output System]

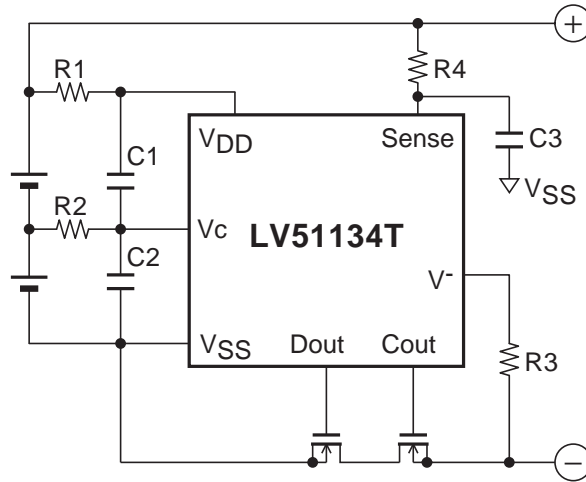


[Dout Output System]



LV51134T

Application Circuit Example



Components	Recommended value	max	unit
R1, R2	100	1k	Ω
R3	2k	4k	Ω
R4	100	10k	Ω
C1, C2, C3	0.1 μ	1 μ	F

* These numbers don't mean to guarantee the characteristic of the IC.

* In addition to the components in the upper diagram, it is necessary to insert a capacitor with enough capacity between VDD and VSS of the IC as near as possible to stabilize the power supply voltage to the IC.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of May, 2007. Specifications and information herein are subject to change without notice.