

## 3-line IPAD™, EMI filter including ESD protection

### Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation: 1.2 mm<sup>2</sup>
- Very thin package: 0.60 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

### Complies with the following standards:

- IEC 61000-4-2 Level 4 on external and V<sub>cc</sub> pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- Level 1 on internal pins:
  - 2 kV (air discharge)
  - 2 kV (contact discharge)
- MIL STD 883E - Method 3015-6 Class 3

### Applications

EMI filtering and ESD protection for:

- SIM interface (subscriber identity module)
- UIM interface (universal identity module)

### Description

The EMIF03-SIM02F3 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference.

This filter includes ESD protection circuitry which prevents damage to the protected device when subjected to ESD surges up to 15 kV.

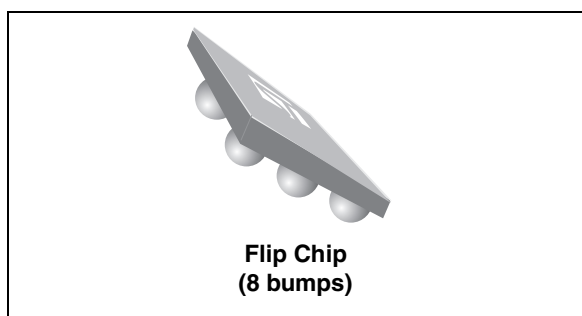


Figure 1. Pin layout (bump side)

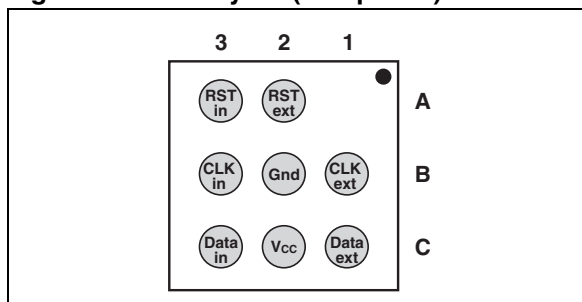
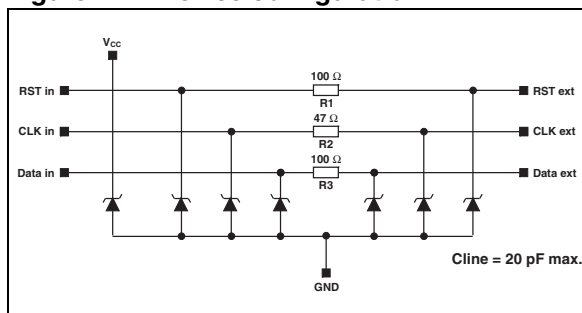


Figure 2. Device configuration



TM: IPAD is a trademark of STMicroelectronics.

# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

| Symbol                                    | Parameter and test conditions                 | Value      | Unit               |
|---|---|------------|--------------------|
| $V_{PP}$                                  | <b>Internal pins (A3, B3, C3):</b>            |            |                    |
|   | ESD discharge IEC61000-4-2, air discharge     | 2          | kV                 |
|   | ESD discharge IEC61000-4-2, contact discharge | 2          |                    |
|   | <b>External pins (A2, B1, C2, C1):</b>        |            |                    |
| ESD discharge IEC61000-4-2, air discharge | 15  |            |                    |
|   | ESD discharge IEC61000-4-2, contact discharge | 8          |                    |
| $T_j$                                     | Maximum junction temperature                  | 125        | $^{\circ}\text{C}$ |
| $T_{op}$                                  | Operating temperature range                   | -40 to +85 | $^{\circ}\text{C}$ |
| $T_{stg}$                                 | Storage temperature range                     | -55 to 150 | $^{\circ}\text{C}$ |

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

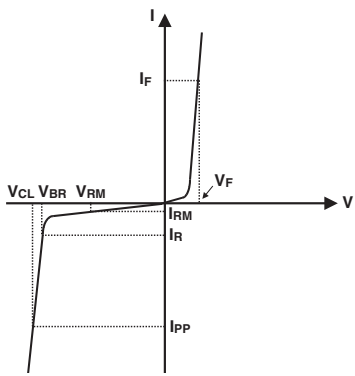
| Symbol     | Parameters  |   |     |     |               |
|------------|---|---|-----|-----|---------------|
| $V_{BR}$   | Breakdown voltage   |  |     |     |               |
| $I_{RM}$   | Leakage current @ $V_{RM}$  |   |     |     |               |
| $V_{RM}$   | Stand-off voltage   |   |     |     |               |
| $V_{CL}$   | Clamping voltage  |   |     |     |               |
| $I_{PP}$   | Peak pulse current  |   |     |     |               |
| $R_{I/O}$  | Series resistance between input and output                        |   |     |     |               |
| $C_{line}$ | Input capacitance per line  |   |     |     |               |
| Symbol     | Test conditions   | Min   | Typ | Max | Unit          |
| $V_{BR}$   | $I_R = 1\text{ mA}$   | 6   |     | 20  | V             |
| $I_{RM}$   | $V_{RM} = 3\text{ V}$   |   |     | 0.2 | $\mu\text{A}$ |
| $R_d$      |   |   | 1.5 |     | $\Omega$      |
| $R_1, R_3$ | Tolerance $\pm 20\%$  |   | 100 |     | $\Omega$      |
| $R_2$      | Tolerance $\pm 20\%$  |   | 47  |     | $\Omega$      |
| $C_{line}$ | $V_{line} = 0\text{ V}, V_{osc} = 30\text{ mV}, F = 1\text{ MHz}$ |   |     | 20  | pF            |

Figure 3. S21 (dB) attenuation measurement (A2-A3 line)

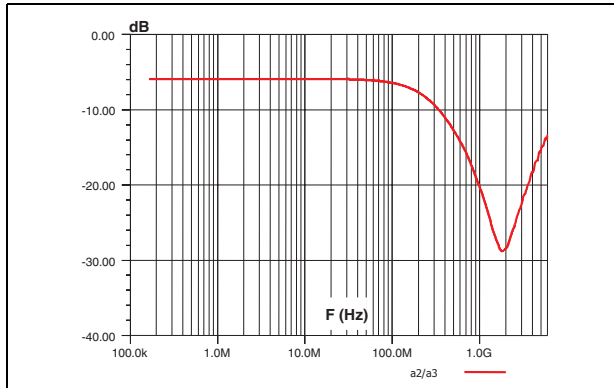


Figure 4. S21 (dB) attenuation measurement (B1-B3 line)

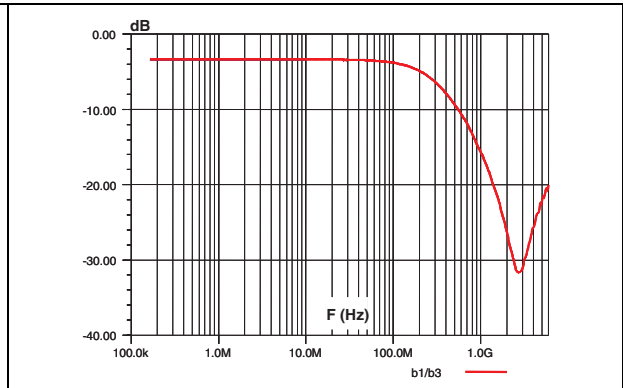


Figure 5. S21 (dB) attenuation measurement (C1-C3 line)

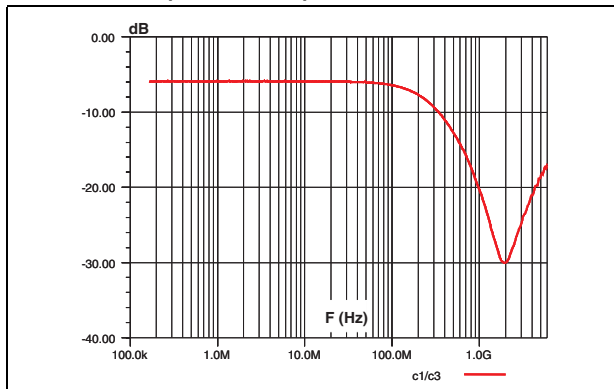


Figure 6. Analog crosstalk measurement

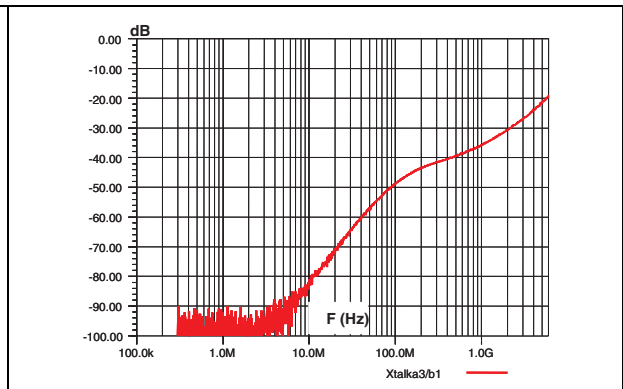


Figure 7. Digital crosstalk measurement

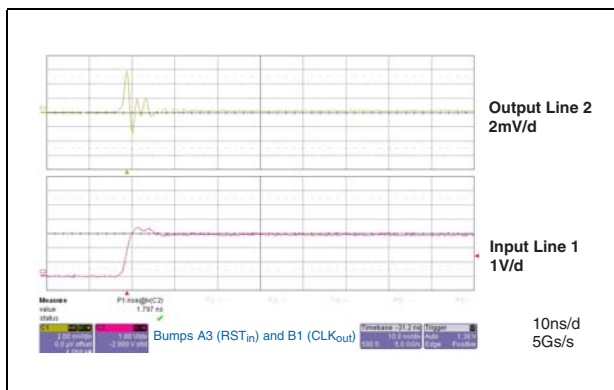


Figure 8. Line capacitance versus reverse applied voltage (typical)

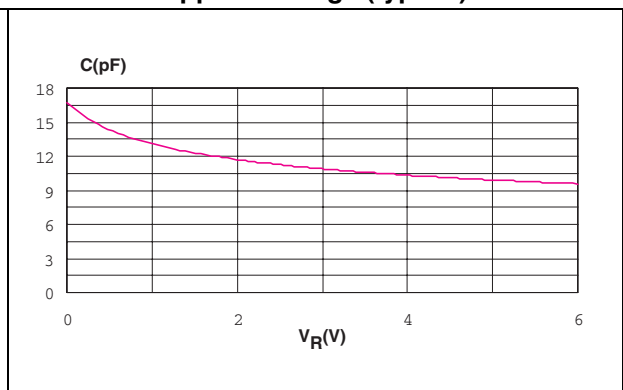


Figure 9. Voltages when IEC 61000-4-2 (+15 kV air discharge) applied to external pin

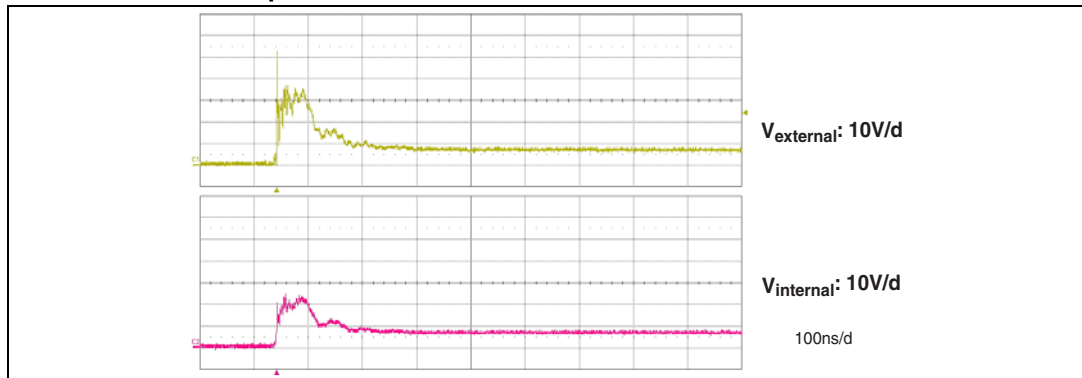
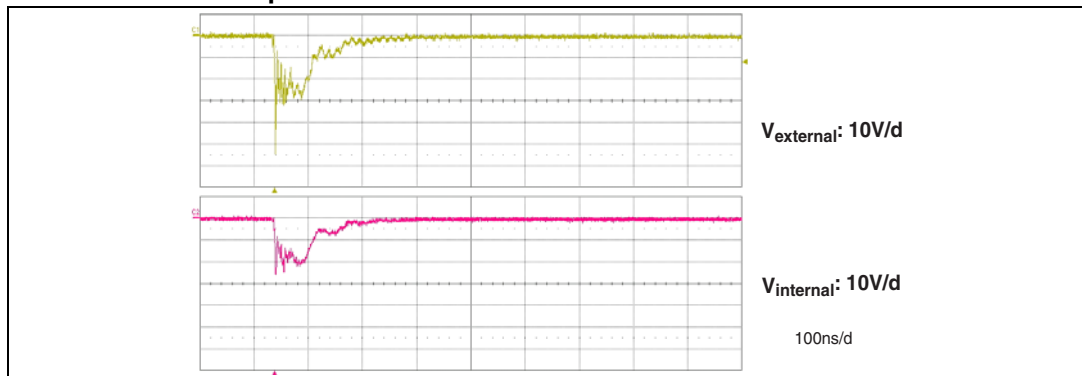


Figure 10. Voltages when IEC 61000-4-2 (- 15 kV air discharge) applied to external pin



## 2 Application information

Figure 11. Aplac model

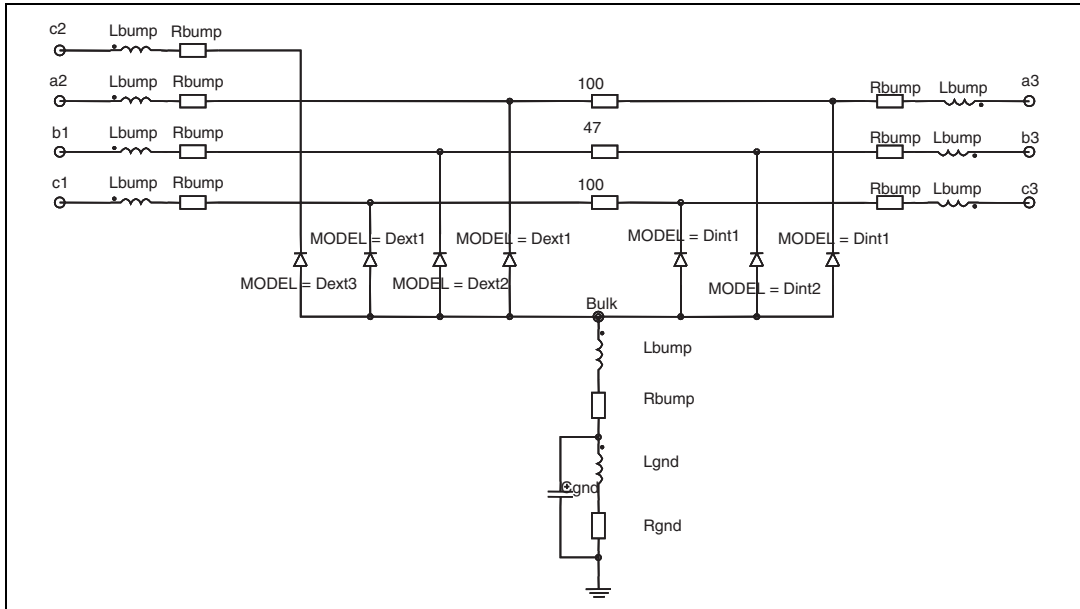
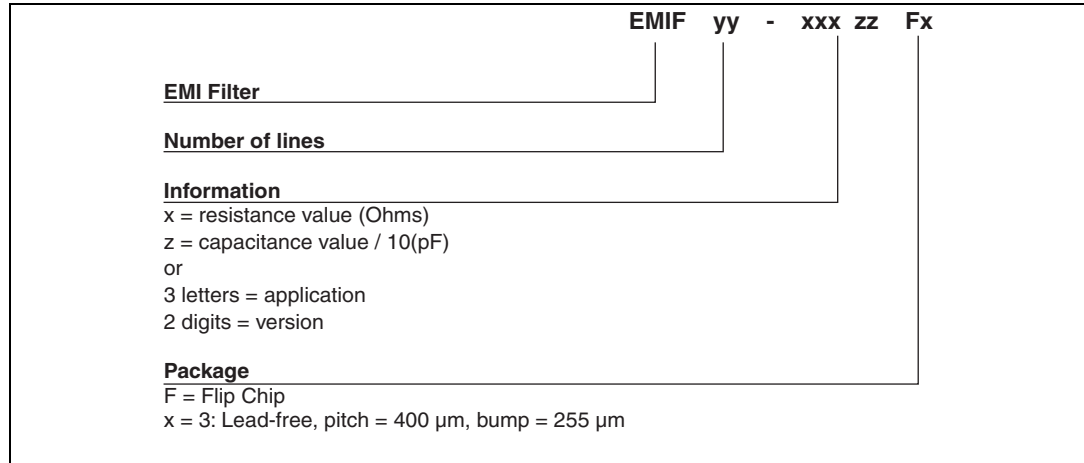


Figure 12. Aplac parameters

|                      |           |           |           |           |           |
|----------------------|-----------|-----------|-----------|-----------|-----------|
| aplacvar Ls 950pH    |           |           |           |           |           |
| aplacvar Rs 150m     |           |           |           |           |           |
| aplacvar Cext1 12pF  | Dint1     | Dext1     | Dint2     | Dext2     | Dext3     |
| aplacvar Cext2 14pF  | BV=15     | BV=15     | BV=15     | BV=15     | BV=15     |
| aplacvar Cext3 18pF  | CJO=Cint1 | CJO=Cext1 | CJO=Cint2 | CJO=Cext2 | CJO=Cext3 |
| aplacvar Cint1 4.5pF | IBV=1u    | IBV=1u    | IBV=1u    | IBV=1u    | IBV=1u    |
| aplacvar Cint2 4pF   | IKF=1000  | IKF=1000  | IKF=1000  | IKF=1000  | IKF=1000  |
| aplacvar Rbump 17m   | IS=10f    | IS=10f    | IS=10f    | IS=10f    | IS=10f    |
| aplacvar Lbump 43pH  | ISR=100p  | ISR=100p  | ISR=100p  | ISR=100p  | ISR=100p  |
| aplacvar Rgnd 500m   | N=1       | N=1       | N=1       | N=1       | N=1       |
| aplacvar Lgnd 50pH   | M=0.3333  | M=0.3333  | M=0.3333  | M=0.3333  | M=0.3333  |
| aplacvar Cgnd 0.15pF | RS=0.29   | RS=0.25   | RS=0.31   | RS=0.28   | RS=0.25   |
| aplacvar Rsub 100m   | VJ=0.6    | VJ=0.6    | VJ=0.6    | VJ=0.6    | VJ=0.6    |
|                      | TT=50n    | TT=50n    | TT=50n    | TT=50n    | TT=50n    |

### 3 Ordering information scheme

Figure 13. Ordering information scheme



### 4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at [www.st.com](http://www.st.com).

Figure 14. Package dimensions

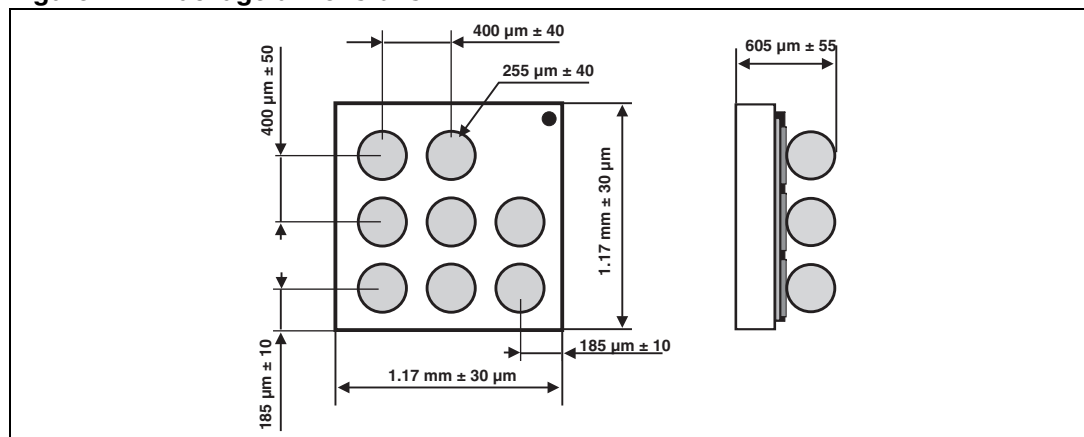


Figure 15. Footprint

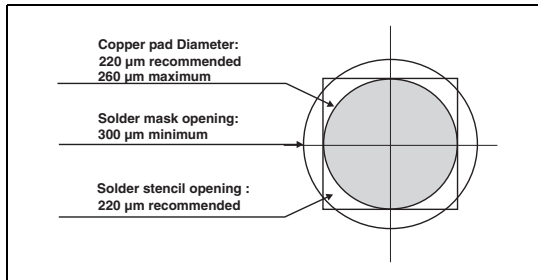


Figure 16. Marking

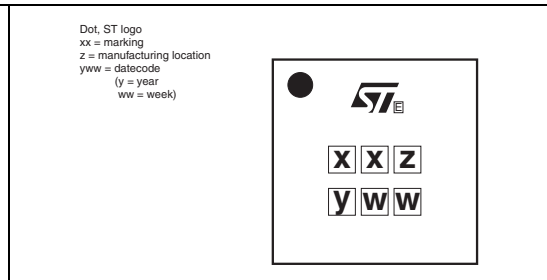
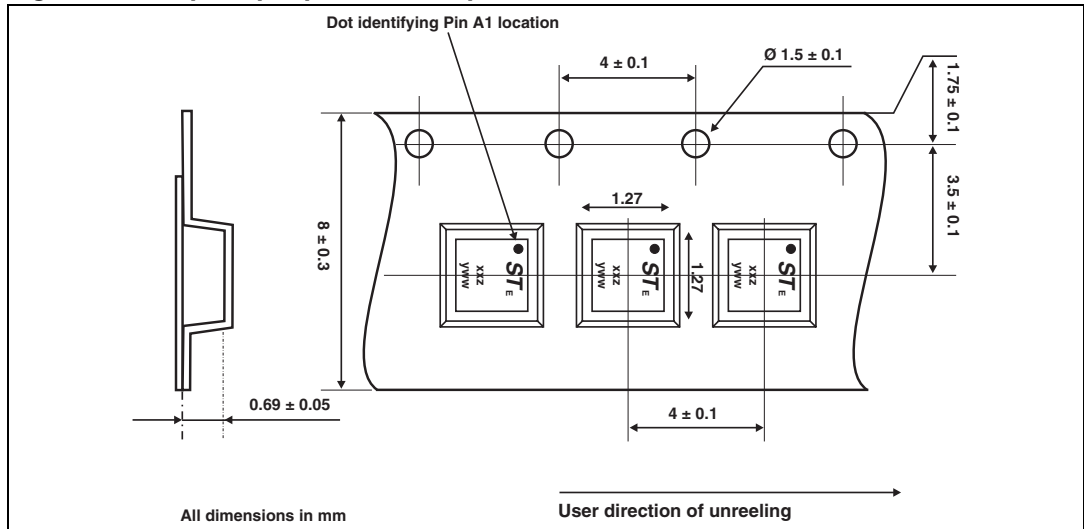


Figure 17. Flip Chip tape and reel specification



Note:

More information is available in the application notes:

AN2348: "STMicroelectronics 400 micro-metre Flip Chip: Package description and recommendation for use"

AN1751: "EMI Filters: Recommendations and measurements"

## 5 Ordering information

Table 3. Ordering information

| Order code     | Marking | Package   | Weight  | Base qty | Delivery mode    |
|----------------|---------|-----------|---------|----------|------------------|
| EMIF03-SIM02F3 | HA      | Flip Chip | 1.74 mg | 5000     | Tape and reel 7" |

## 6 Revision history

**Table 4. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 19-Jul-2005 | 1        | Initial release.   |
| 26-Feb-2007 | 2        | Changed out to ext in Configuration diagram on page 1. Added Ecopack statement. Reformatted to current layout standard. Updated Application note AN2348 reference and description. |
| 28-Apr-2008 | 3        | Updated ECOPACK statement. Updated <a href="#">Figure 13</a> , <a href="#">Figure 14</a> , and <a href="#">Figure 17</a> . Reformatted to current standards.                       |



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