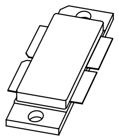


BLF369

Multi-use VHF power LDMOS transistor

Rev. 03 — 29 January 2008 **Preliminary data sheet**

1. Product profile

1.1 General description

A general purpose 500 W LDMOS RF power transistor for pulsed and continuous wave applications in the HF/VHF band up to 500 MHz.

Table 1. Typical performance

Typical RF performance at V_{DS} = 32 V and T_h = 25 °C in a common-source 225 MHz test circuit.[1]

Mode of operation	f (MHz)	P_L (W)	$P_{L(PEP)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)
CW, class AB	225	500	-	18	60	-
2-tone, class AB	f_1 = 225; f_2 = 225.1	-	500	19	47	–28
pulsed, class AB [2]	225	500	-	19	55	-

[1] T_h is the heatsink temperature.

[2] t_p = 2 ms; δ = 10 %.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

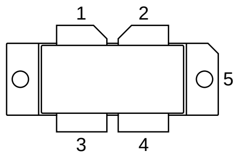
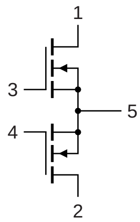
- Typical pulsed performance at 225 MHz, a drain-source voltage V_{DS} of 32 V and a quiescent drain current I_{Dq} = 2 × 1.0 A:
  - Load power P_L = 500 W
  - Power gain G_p = 19 dB
  - Drain efficiency η_D = 55 %
- Advanced flange material for optimum thermal behavior and reliability
- Excellent ruggedness
- High power gain
- Designed for broadband operation (HF/VHF band)
- Source on underside eliminates DC isolators, reducing common-mode inductance
- Easy power control
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS), using exemption No. 7 of the annex

1.3 Applications

- Pulsed applications up to 500 MHz
- Communication transmitter applications in the HF/VHF/UHF band under specific conditions
- Industrial applications up to 500 MHz under special conditions

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF369	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT800-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

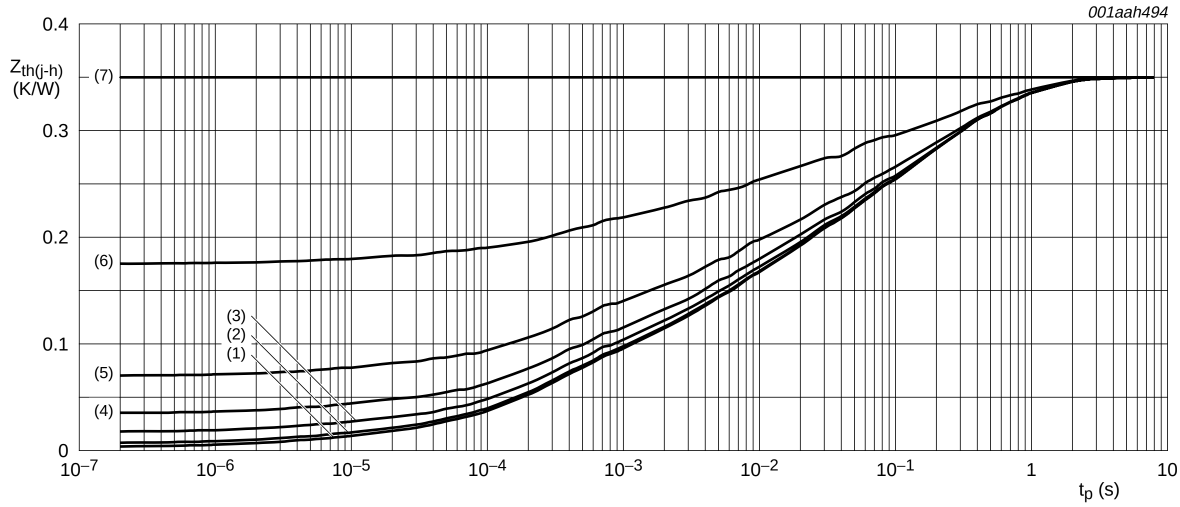
Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_j = 200 °C	[1][2]	0.26	K/W
$R_{th(j-h)}$	thermal resistance from junction to heatsink	T_j = 200 °C	[1][2][3]	0.35	K/W
$Z_{th(j-h)}$	transient thermal impedance from junction to heatsink	T_j = 200 °C			
		t_p = 100 µs; δ = 10 %	[4]	0.063	K/W
		t_p = 1 ms; δ = 10 %	[4]	0.117	K/W
		t_p = 2 ms; δ = 10 %	[4]	0.133	K/W
		t_p = 3 ms; δ = 10 %	[4]	0.142	K/W
		t_p = 1 ms; δ = 20 %	[4]	0.140	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-case)}$ and $R_{th(j-h)}$ are measured under RF conditions.

[3] $R_{th(j-h)}$ is dependent on the applied thermal compound and clamping/mounting of the device.

[4] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to heatsink as function of pulse duration

6. Characteristics

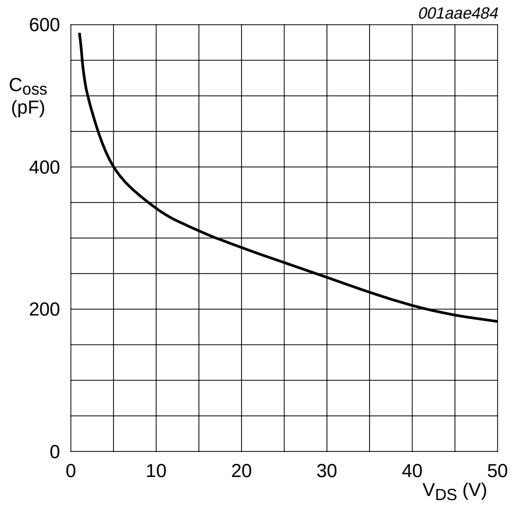
Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 6 mA	[1]	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 600 mA	[1]	4	-	5.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V		-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V		-	100	-	A
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V		-	-	60	nA
g_{fs}	forward transconductance	V_{GS} = 20 V; I_D = 13 A	[1]	-	15	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 9 V; I_D = 13 A	[1]	-	40	-	mΩ
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	[2]	-	400	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	[2]	-	230	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz		-	15	-	pF

[1] I_D is the drain current.

[2] C_{iss} and C_{oss} include reverse transfer capacitance (C_{rss}).



V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Application information

Table 7. RF performance in a common-source 225 MHz test circuit

T_h = 25 °C unless otherwise specified.

Mode of operation	f (MHz)	V_{DS} (V)	I_{Dq} (A)	P_L (W)	$P_{L(PEP)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	ΔG_p (dB)
CW, class AB	225	32	2 × 1.0	500	-	> 17	> 55	-	-
2-tone, class AB	f_1 = 225; f_2 = 225.1	32	2 × 1.0	-	500	> 18	> 43	< −24	1
pulsed, class AB [1]	225	-	-	500	-	> 18	> 50	-	-

[1] t_p = 2 ms; δ = 10 %.

7.1 CW

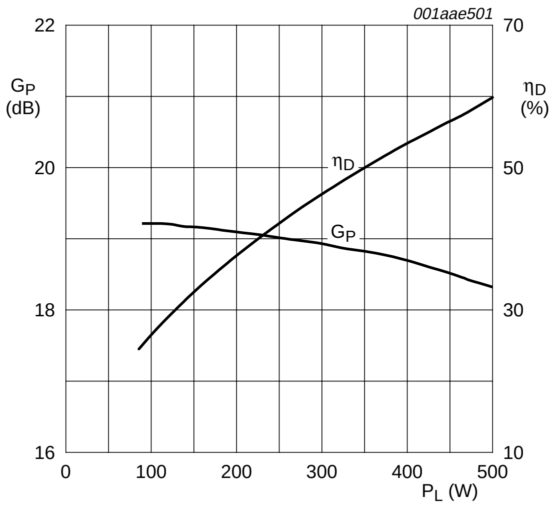
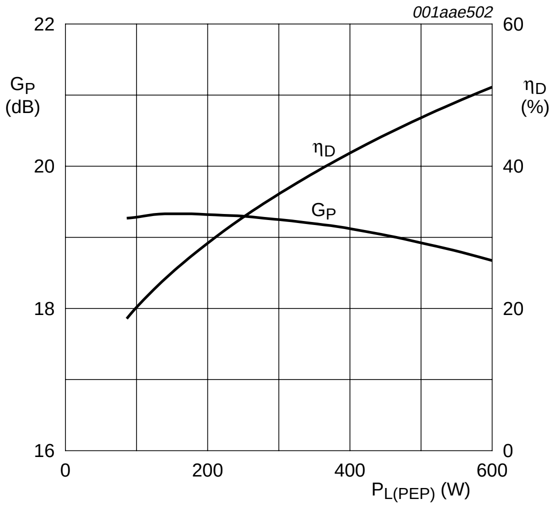


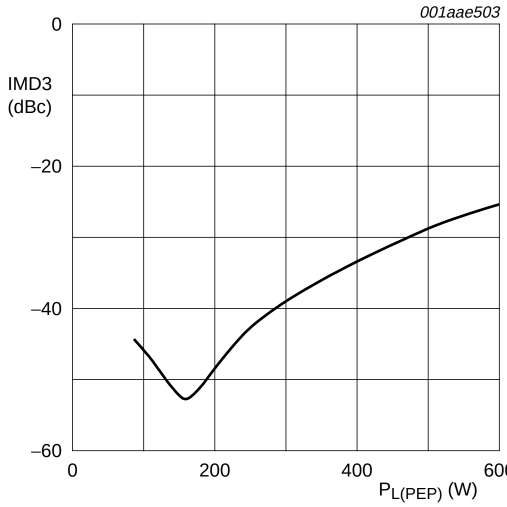
Fig 3. CW power gain and drain efficiency as a function of output power; typical values

7.2 2-Tone



V_{DS} = 32 V; f_1 = 225 MHz; f_2 = 225.1 MHz;
I_{Dq} = 2 × 1.0 A; T_h = 25 °C.

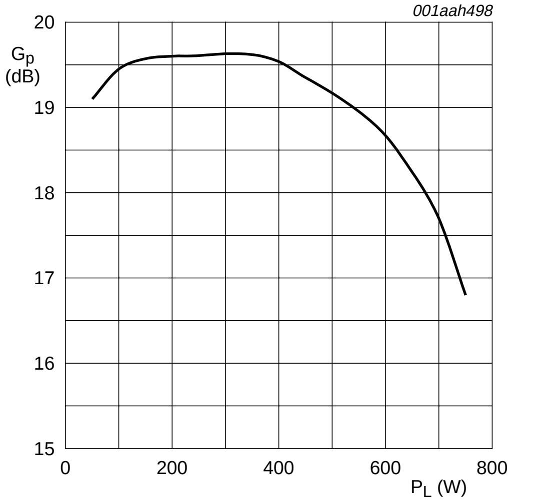
Fig 4. 2-Tone power gain and drain efficiency as a function of peak envelope power; typical values



V_{DS} = 32 V; f_1 = 225 MHz; f_2 = 225.1 MHz;
I_{Dq} = 2 × 1.0 A; T_h = 25 °C.

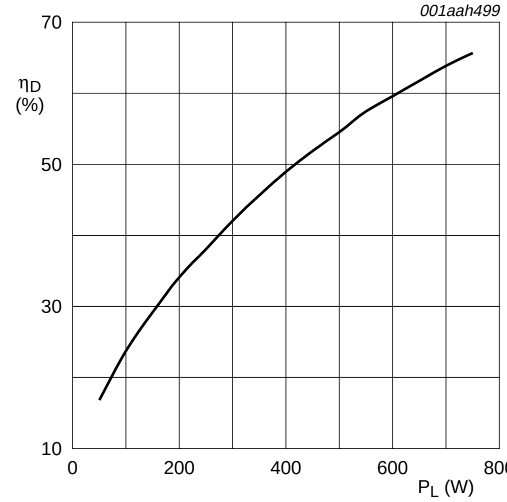
Fig 5. 2-Tone third order intermodulation distortion as a function of peak envelope power; typical values

7.3 Pulsed



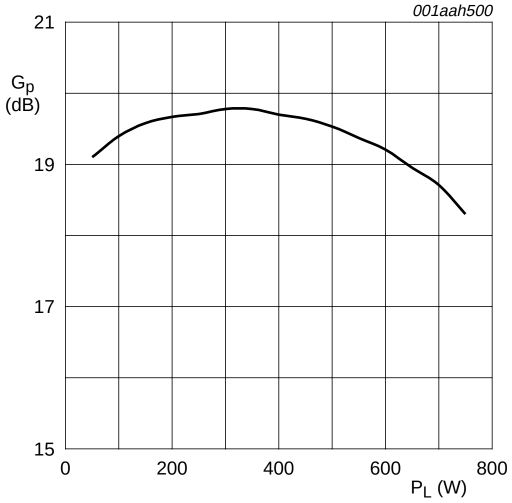
f = 225 MHz; V_{DS} = 32 V; I_{Dq} = 2 × 1 A; t_p = 2 ms;
δ = 10 %.

Fig 6. Pulsed power gain as function of load power; typical values



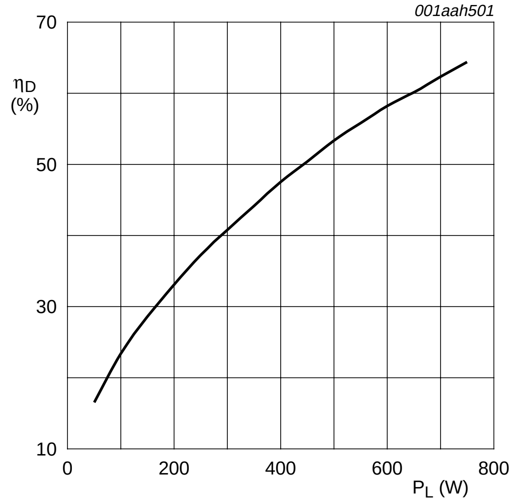
f = 225 MHz; V_{DS} = 32 V; I_{Dq} = 2 × 1 A; t_p = 2 ms;
δ = 10 %.

Fig 7. Pulsed drain efficiency as function of load power; typical values



f = 225 MHz; V_{DS} = 32 V; I_{Dq} = 2 × 1 A; t_p = 100 µs; δ = 10 %.

Fig 8. Pulsed power gain as function of load power; typical values



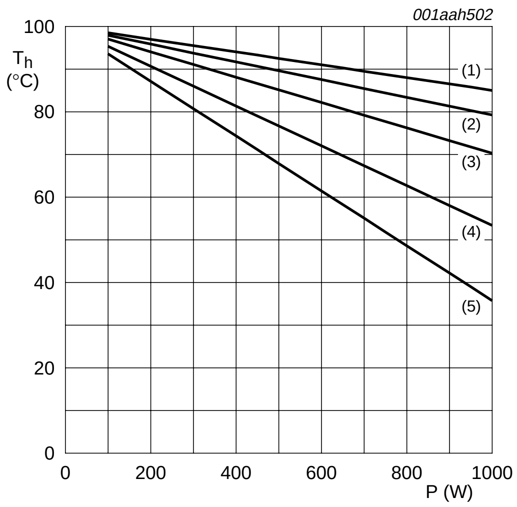
f = 225 MHz; V_{DS} = 32 V; I_{Dq} = 2 × 1 A; t_p = 100 µs; δ = 10 %.

Fig 9. Pulsed drain efficiency as function of load power; typical values

7.4 Maximum heatsink temperature

The heatsink temperature is defined 1 mm below the surface of the heatsink at the center of the flange.

The maximum allowable heatsink temperature is given in the following graphs at several pulsed conditions as well as for CW.



δ = 10 %.

(1) $t_p \leq 2$ ms

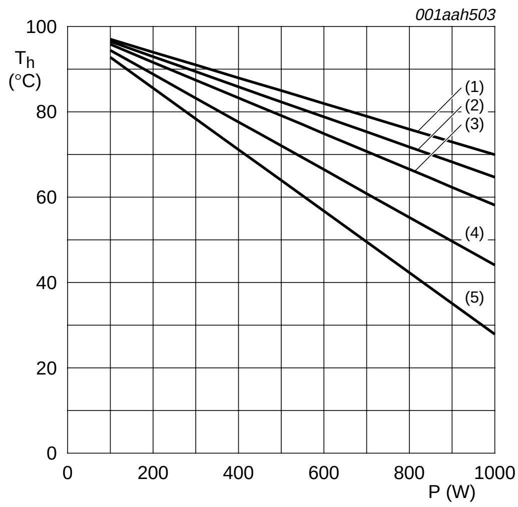
(2) $t_p = 10$ ms

(3) $t_p = 20$ ms

(4) $t_p = 50$ ms

(5) $t_p = 100$ ms

Fig 10. Heatsink temperature as function of power dissipation at a duty cycle of 10 %



δ = 20 %.

(1) $t_p \leq 2$ ms

(2) $t_p = 10$ ms

(3) $t_p = 20$ ms

(4) $t_p = 50$ ms

(5) $t_p = 100$ ms

Fig 11. Heatsink temperature as function of power dissipation at a duty cycle of 20 %

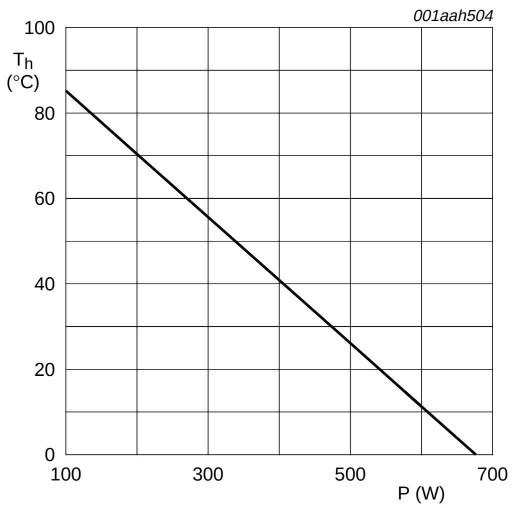
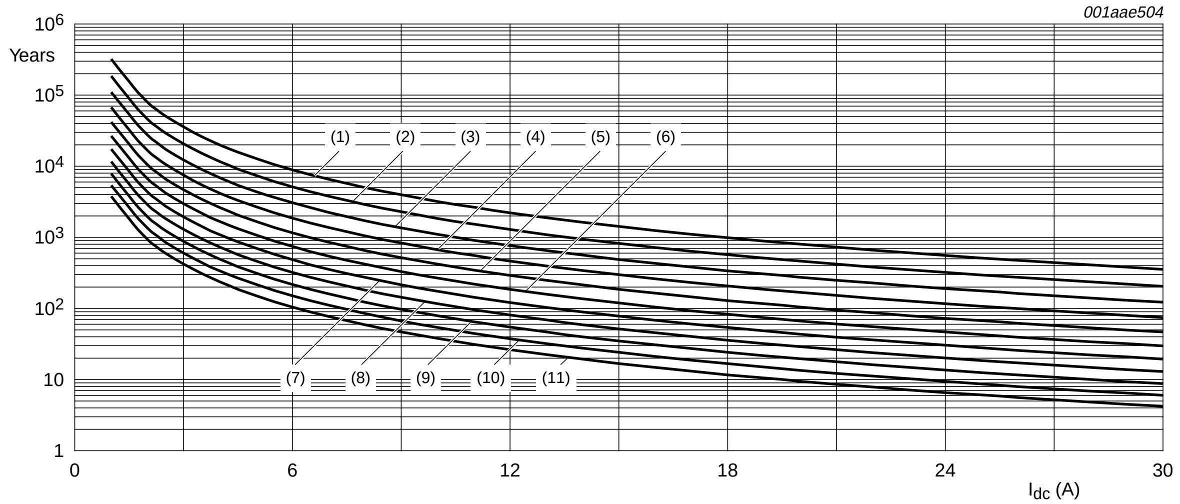


Fig 12. CW heatsink temperature as function of power dissipation

7.5 Ruggedness in class-AB operation

The BLF369 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: 2-tone signal; $V_{DS} = 32$ V; f = 225 MHz at rated load power ($P_{L(PEP)} = 500$ W).

7.6 Reliability



TTF (0.1 % failure fraction); best estimate values.

The reliability at pulsed conditions can be calculated as follows: TTF (0.1 %) × 1 / δ.

(1) T_j = 100 °C
(2) T_j = 110 °C
(3) T_j = 120 °C
(4) T_j = 130 °C
(5) T_j = 140 °C
(6) T_j = 150 °C
(7) T_j = 160 °C
(8) T_j = 170 °C
(9) T_j = 180 °C
(10) T_j = 190 °C
(11) T_j = 200 °C

Fig 13. BLF369 electromigration (I_D, total device)

8. Test information

Table 8. List of components

For test circuit, see Figure 14, Figure 15 and Figure 16.

Component	Description	Value		Remarks
B1	semi rigid coax	25 Ω; 120 mm		EZ90-25-TP
B2	semi rigid coax	25 Ω; 56 mm		EZ90-25-TP
C1	multilayer ceramic chip capacitor	91 pF	[1]	
C2, C3	multilayer ceramic chip capacitor	56 pF	[1]	
C4, C7	multilayer ceramic chip capacitor	100 pF	[1]	
C5, C8	ceramic capacitor	15 nF		
C6, C9	electrolytic capacitor	220 µF		
C10, C11, C13, C14	multilayer ceramic chip capacitor	220 pF	[1]	
C12, C15	ceramic capacitor	15 nF	[1]	

Table 8. List of components *...continued*

For test circuit, see Figure 14, Figure 15 and Figure 16.

Component	Description	Value		Remarks
C20	multilayer ceramic chip capacitor	100 pF	[1]	
C21	multilayer ceramic chip capacitor	20 pF	[1]	
C22, C25	multilayer ceramic chip capacitor	100 pF	[1]	
C23, C26	ceramic capacitor	15 nF		
C24, C27	electrolytic capacitor	10 μF		
C28, C31	multilayer ceramic chip capacitor	100 pF	[1]	
C29, C32	multilayer ceramic chip capacitor	220 pF		
C30, C33	ceramic capacitor	15 nF		
L1, L3	stripline	-	[2]	(W × L) 12 mm × 15 mm
L2, L4	air coil	-		4 windings; D = 8 mm; d = 1 mm
L5, L6	stripline	-	[2]	(W × L) 14 mm × 15 mm
R1, R2, R3, R4	resistor	0.25 W; 4 Ω		
R5, R6, R8, R9	resistor	0.25 W; 10 Ω		
R7, R10	potentiometer	10 kΩ		
R11, R12	resistor	0.25 W; 1 Ω		
T1, T2	semi rigid coax	25 Ω; 68 mm		EZ90-25-TP
T3, T4	semi rigid coax	25 Ω; 60 mm		EZ90-25-TP

[1] American technical ceramics type 100B or capacitor of same quality.

[2] Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.

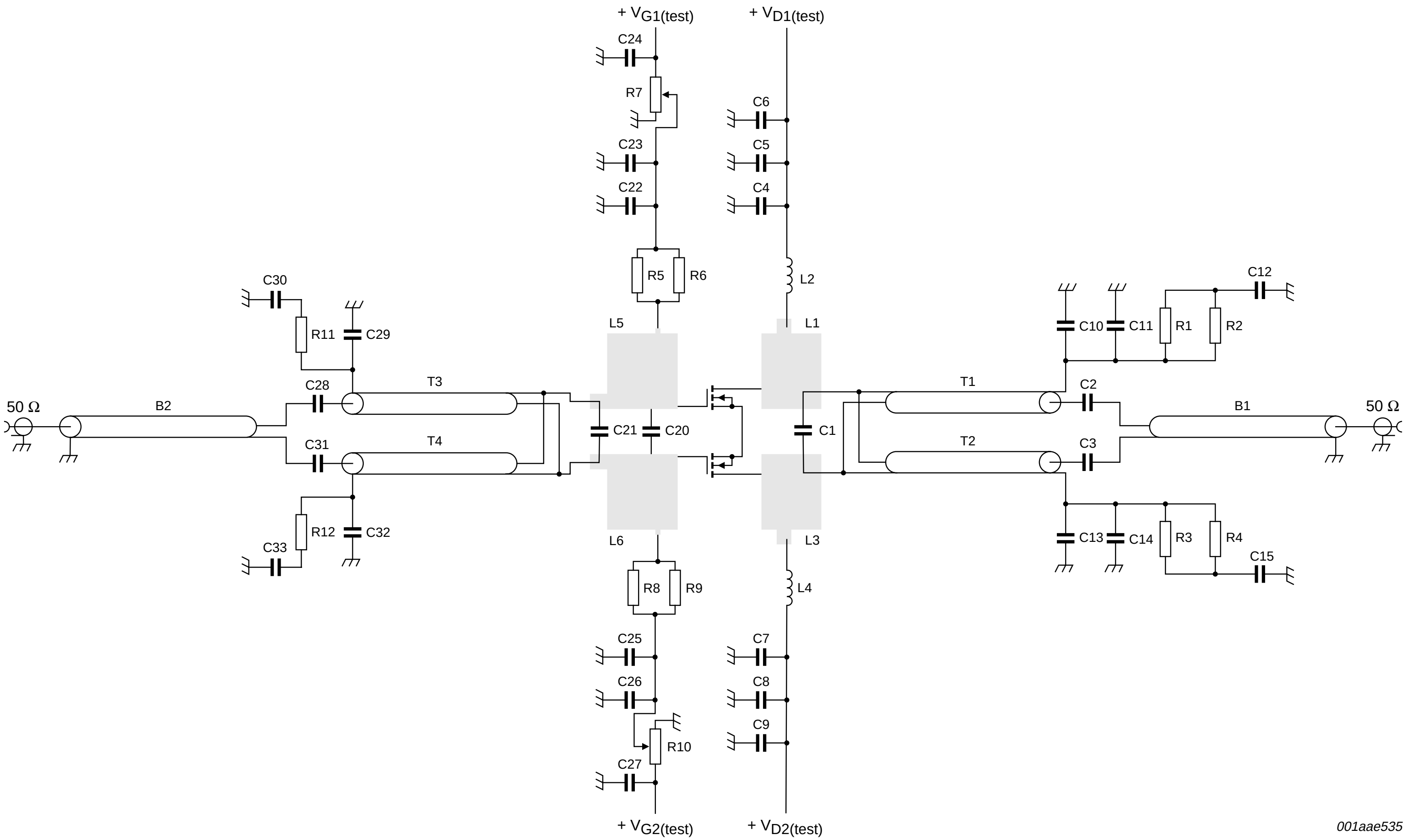


Fig 14. Class-AB common-source 225 MHz test circuit; $V_{D1(test)}$, $V_{D2(test)}$, $V_{G1(test)}$ and $V_{G2(test)}$ are drain and gate test voltages

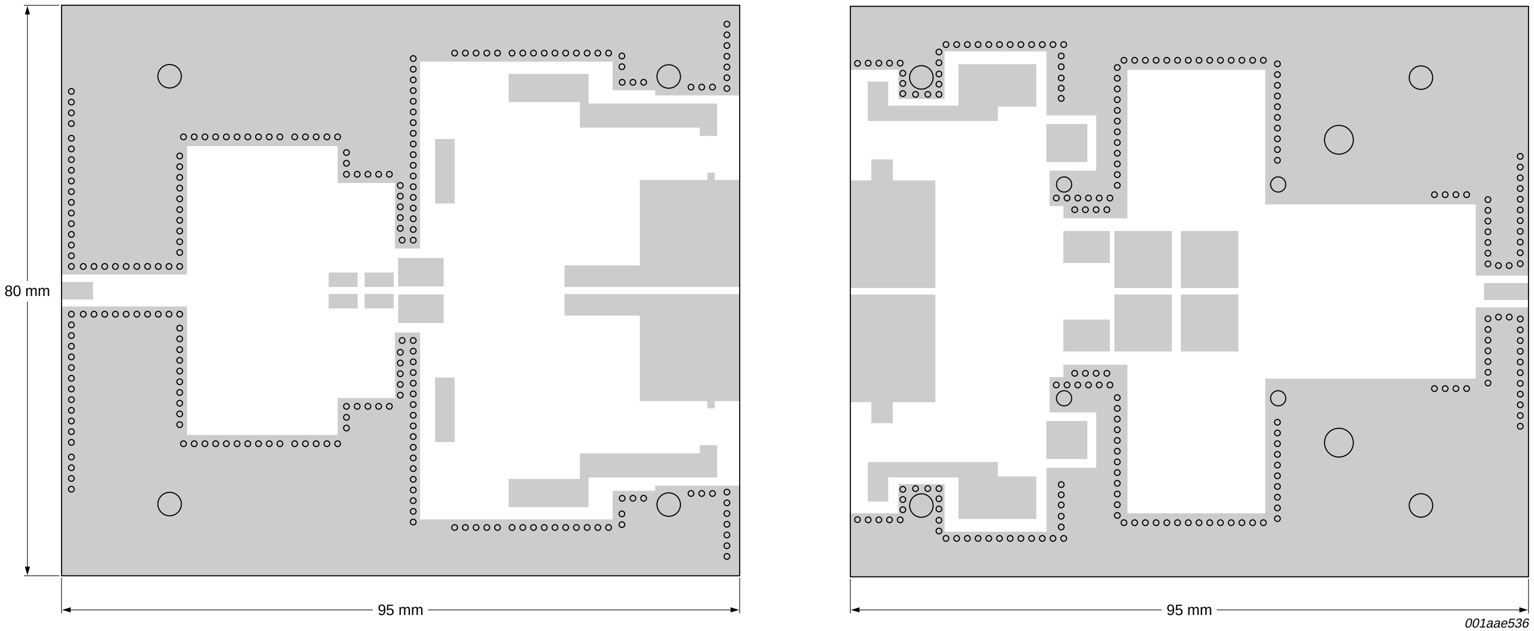
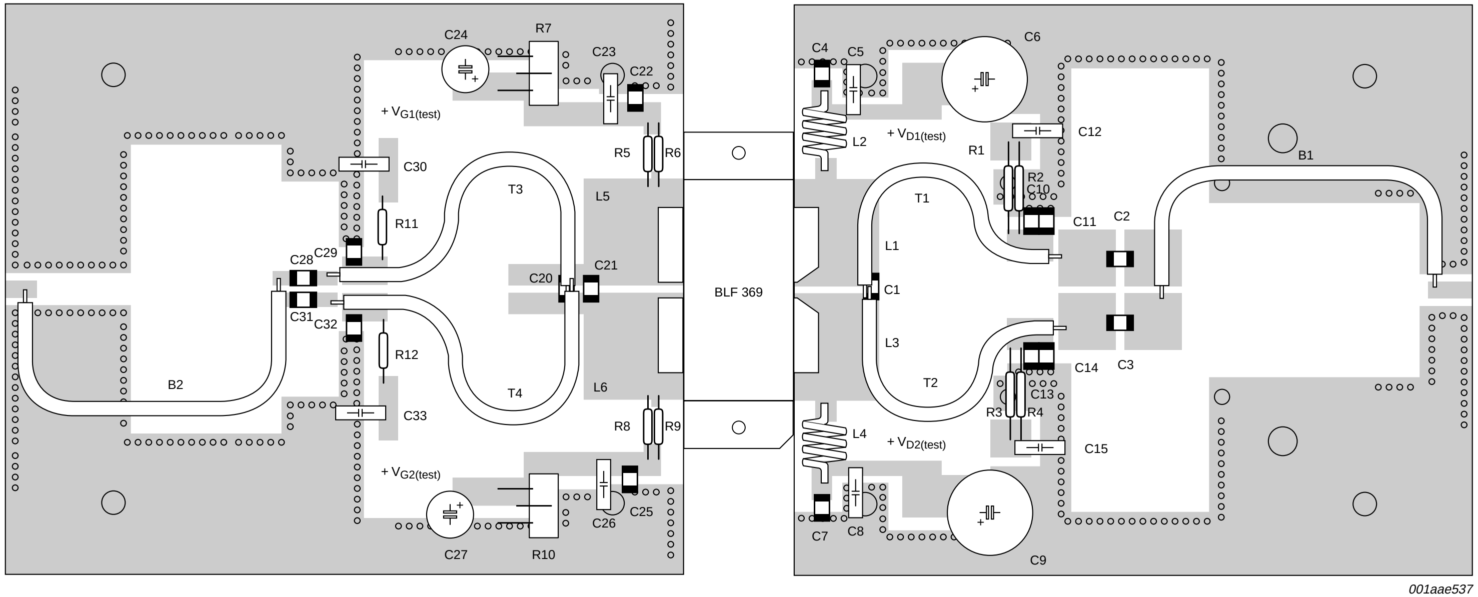


Fig 15. Printed-Circuit Board (PCB) for class-AB 225 MHz test circuit

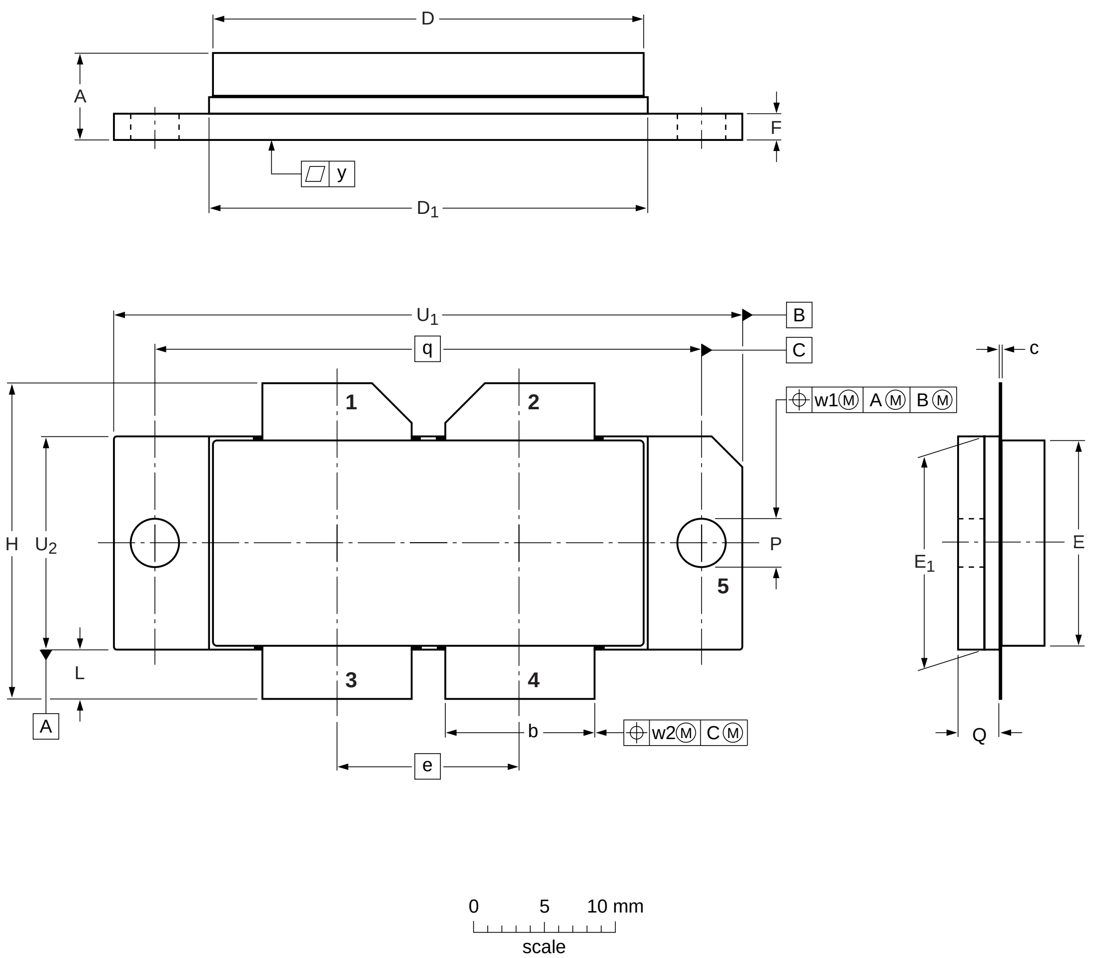


C1 mounted on top of transformers T1 and T2; C20 mounted on top of transformers T3 and T4.

Fig 16. Component layout for class-AB 225 MHz test circuit

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT800-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	L	p	Q	q	U_1	U_2	w_1	w_2	y
mm	6.3 5.9	10.55 10.45	0.15 0.10	30.5 29.9	31.1 30.9	14.6 14.4	15.3 15.1	12.7	2.26 2.00	22.8 21.8	3.7 3.3	3.56 3.49	3.1 2.8	38.5	44.5 44.2	15.4 15.0	0.25	0.25	0.05
inches	0.248 0.232	0.415 0.411	0.006 0.004	1.201 1.177	1.224 1.216	0.575 0.567	0.602 0.594	0.5	0.089 0.079	0.898 0.858	0.146 0.130	0.140 0.137	0.122 0.110	1.516	1.752 1.740	0.606 0.591	0.01	0.01	0.002

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT800-2						~~05-06-02~~ 05-06-07

Fig 17. Package outline SOT800-2

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
CW	Continuous Wave
DC	Direct Current
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PEP	Peak Envelope Power
RF	Radio Frequency
TTF	Time To Failure
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF369_3	20080129	Preliminary data sheet	-	BLF369_2
Modifications:	• Information for pulsed conditions has been added.			
BLF369_2	20061208	Objective data sheet	-	BLF369_1
BLF369_1	20060413	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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