EM77930

USB + BB Controller

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial released version	2007/08/20

1 General Description

The EM77930 from ELAN Technology is a low-cost and high performance 8-bit CMOS advance RISC architecture microcontroller device. It has an on-chip 1-Mbps RF driver Baseband (BB), Universal Serial Bus (USB), one Pulse Width Modulation (PWM) with 16-bit resolution, an 8-bit Timer Clock Counter (TCC) and a 16-bit Free Run Timer, Key Wake-up function (KWU), Power-on Reset (POR), Watchdog Timer (WDT), and power saving Sleep Mode. All these features combine to ensure applications require the least external components, hence, not only reduce system cost, but also have the advantage of low power consumption and enhanced device reliability.

The 44-pin EM77930 is available in a very cost-effective ROM version. It is also suitable for wireless base-band and USB device production.

2 Features

2.1 Core

- Operating Voltage Range: 2.2V ~ 3.6V DC
- Operating Temperature Range: 0°C ~ 70°C
- Operating Frequency Range: DC ~ 48MHz (1 clock/cycle)
- 6MHz external clock source
- 6/12/24/48 MHz Core & BB clock
- 6/48MHz internal USB clock (Low/Full speed)
- 12K x 16 bits of on-chip Program ROM
- 1216 x 8 bits of on-chip Register (SRAM) plus USB indirect addressing RAM
- Watchdog Timer (WDT)
- 16-level stacks for both CALL and interrupt subroutine
- Internal Power-on Reset (POR) function.
- All single cycle (1 clock) instruction except for conditional branches which are two or three cycles
- Direct, indirect and relative addressing modes
- Low power, high speed CMOS technology
- Power consumption:

  < 4 mA @ 3.3V, 6 MHz

  < 1 µA standby current

2.2 Oscillators/System Clocks

- Three oscillator options:
  - Crystal/Resonate oscillator of high frequency
  - PLL oscillator: 6MHz, 12 MHz, 24 MHz, and 48 MHz (External crystal should be 6 MHz)
  - Internal RC oscillator (32kHz)
- Three modes of system clocks:
  - Sleep mode
  - Green mode
  - Normal mode
- Internal RC oscillator for Power-on Reset (POR) and Watchdog Timer (WDT)

2.3 Input and Output (I/O) Pins

- Max. of 30 I/O pins
- Pull-up resistor options
- Key Wake-up function
- Open drain output options

2.4 Timers and Counters

- Programmable 8-bit real Time Clock/Counter (TCC) with prescaler and overflow interrupt
- 16-bit Free Run Counter (FRC) with overflow interrupt

2.5 Interrupt Sources and Features

- Hardware priority check
- Different interrupt vectors
- Interrupts:
  - Key Wake up
  - External pin interrupt
  - 16-bit Free Run Counter Overflow
  - TCC (time-base) overflow
  - One complete period of Pulse Width Modulation (PWM)
  - Base band (BB) function interrupts
    - CSD: carrier sense detection

- TX_AE: TX_FIFO almost full
- RX_AF: RX_FIFO almost full
- TX_ EMPTY: finish a transmitting a package
- RX_OF: RX_FIFO overflow
- LINK_DIS: zero counter capacitor discharge mechanism
- LOCK_OUT: finish receiving a package
- LOCK_IN: start receiving a package

- USB function interrupts:
  - Endpoint 0 Interrupt Event:
    - INT0RX: EP0 USB RX Event
    - INT0TX: EP0 USB TX Event
    - INT0IN: EP0 USB IN Token Event
  - Endpoint X Interrupt Event:
    - INT1: EP1 Interrupt
    - INT2: EP2 Interrupt
    - INT3: EP3 Interrupt
  - Device State Interrupt Event:
    - RSTINT: USB Bus Reset Event Detect
    - IDLEINT: USB Bus Suspend Detect
    - RUEINT: Enable USB Bus Resume Detect
    - SOFINT: Start of Frame Interrupt

2.6 Baseband

- Serial to Parallel conversion of RFW102 interface
- Input FIFO (RX_FIFO)
- Output FIFO (TX_FIFO)
- Preamble Correlation
- Packet Address Filter (Network and unique)

- CRC calculation
- Inter-RFWAVES networks Carrier-sense
- Discharge of RFW-102 reference capacitor
- Compensate for clock drifts between the transmitting EM77930 and the receiving EM77930 up to 1000ppm. Hence, the EM77930 requires low performance crystal
- Interrupt Driver

2.7 Universal Serial Bus (USB)

- USB Specification Compliance
  - Conforms to USB specification, version 1.1
  - Conforms to USB Human Interface Device (HID) Specification, version 1.1.
- 5V supplied from PC USB interface

2.8 Pulse Width Modulation (PWM)

- One Pulse Width Modulation (PWM) with 16-bit resolution

2.9 Built-in Voltage Regulator

- Internal 3.3V regulator is used to be the power source of the MCU and the regulated output pin to provide a pull-up source for the external USB resistor on the downstream D- pin.

3 Pin Assignment

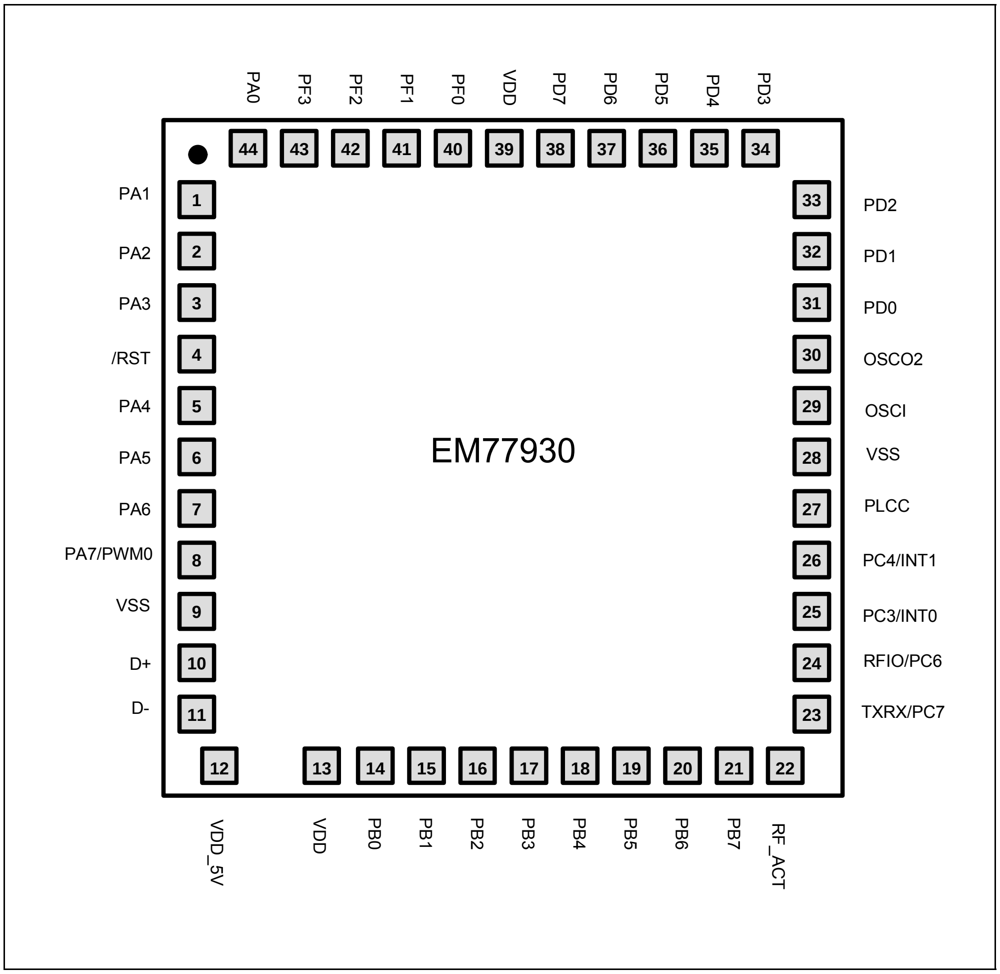


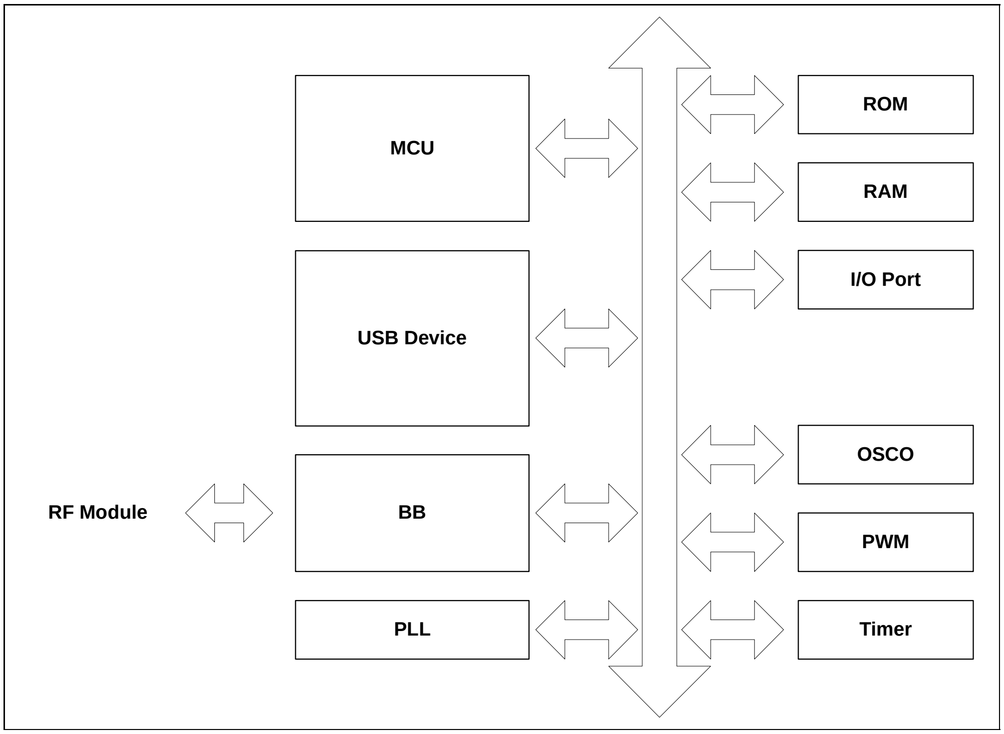
Fig. 3 Pad and Pins Configuration of EM77930

4 Pin Description

The Table below shows the corresponding relationship between the pad and pins of EM77930

Pin No.	Symbol	Type	Smitt Trigger	Pull High /50KΩ	Open Drain	Function Description
1~3	PTA1~3	I/O	–	√	–	Pins 0~3 of Port A (default)
4	/RST	–	√	–	–	Reset
5~8	PTA4~6	I/O	–	√	–	Pins 4~7 of Port A
11	PWM0/PA7	I/O	–	√	–	Pin 7 of Port A PWM0 output
9	VSS	–	–	–	–	Ground Pin
10	UPRT_D+	–	–	–	–	USB upstream differential data plus
11	UPRT_D-	–	–	–	–	USB upstream differential data minus
12	VDD_5V	–	–	–	–	5V Power supply for digital circuit and the embedded USB.
13	VDD	–	–	–	–	3.3v input. (no use regulator) 3.3v stable output. (use regulator)
14~21	KWU0~7 PB0~7	I/O	–	√	√	Pins 0~7 of Port B (default). Key Wake up 0~7
22	RF_ACT	O	–	–	–	BB/RF Active
23	TXRX	O	–	–	–	Transceiver modes control
24	RFIO	I/O	–	√	–	Transceiver to/from RF modem
25	EINT0/ PC3	I/O	–	√	–	External interrupt Pin 0 Pin 3 of Port C
26	EINT1/ PC4	I/O	–	√	–	External interrupt Pin 1 Pin 4 of Port C
27	PLLC	–	–	–	–	External capacitor for PLL circuit
28	VSS	–	–	–	–	Ground Pin
29	OSCI	I	–	–	–	Input of crystal oscillator
30	OSCO2	O	–	–	–	Selected PLL Clock Output
31~ 38	PD0~7	I/O	–	√	–	Pins 0~7 of Port D
39	VDD	–	–	–	–	3.3v input.
40~43	PF0 ~PF3	I/O	–	√	–	Pins 0 ~ 3 of Port F
44	PA0	I/O	–	√	–	Pin 0 of Port A

5 Block Diagram



6 Memory

6.1 Program Memory

The EM77930 has a 14-bit program counter (PC). The program memory space, which is partitioned into two pages can address up to 12K. The first page has 8K and the second page has 4K in length. Fig. 6-1 depicts the profile of the program memory and stack. The initial Address is 0x0000. The table of the interrupt-vectors starts from 0x10 to 0xA8 with every other eight-address space.

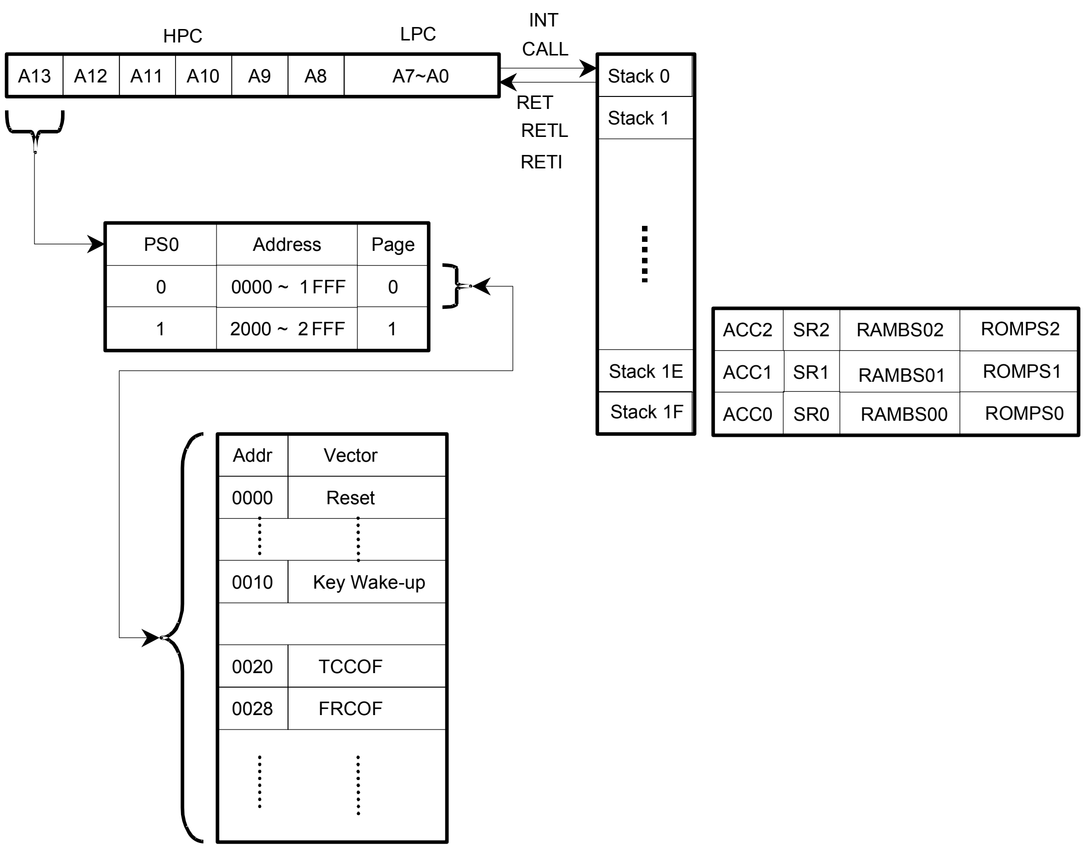


Fig. 6-1 Configuration of Program Memory (ROM) for EM77930

6.2 RAM–Register

A total of 1218 accessible bytes of data memory are available for the EM77930. By function, they are classified into general purpose registers, system control / configuration registers, specification purpose registers, USB control/status registers, baseband (BB) control/status registers, timer/counter registers, and I/O port status/control registers. All of the above registers except I/O ports and their related control registers are implemented as static RAM. The RAM configurations are shown in Fig. 6-2.

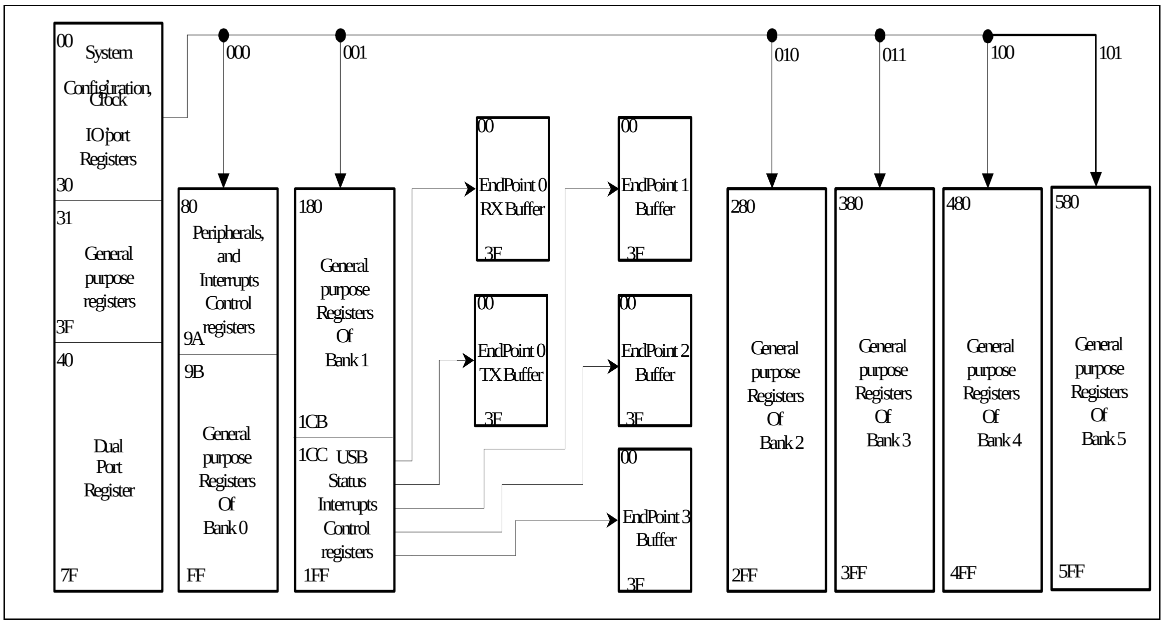


Fig. 6-2 Configuration of Data Memory (RAM) for EM77930

The table is a summary of all registers except general purpose registers.

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	IAC0	Full Name	Indirect Addressing Register contents							
		Bit Name	IAC07	IAC06	IAC05	IAC04	IAC03	IAC02	IAC01	IAC00
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x01	HPC	Full Name	Most Significant Byte of Programming Counter							
		Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	Jump to the corresponding interrupt vector or continue to execute next instruction							
0x02	LPC	Full Name	Least Significant Byte of Programming Counter							
		Bit Name	PCF	PCE	PCD	PCC	PCB	PCA	PC9	PC8
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	Jump to the corresponding interrupt vector or continue to execute next instruction							
0x03	SR	Full Name	Status Register							
		Bit Name	-	-	RST	T	P	Z	DC	C
		Read/Write (R/W)	-	-	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	-	0	1	1	U	U	U
		/RESET and WDT	-	-	P	T	T	P	P	P
		Wake-up from Int	-	-	P	T	T	P	P	P
0x04	RAMBS0	Full Name	RAM Bank Select 0							
		Bit Name	-	-	-	-	-	RBS02	RBS01	RBS00
		Read/Write (R/W)	-	-	-	-	-	R/W	R/W	R/W
		Power-on	-	-	-	-	-	0	0	0
		/RESET and WDT	-	-	-	-	-	0	0	0
		Wake-up from Int	-	-	-	-	-	P	P	P
0x05	ROMPS	Full Name	ROM Page Select							
		Bit Name	-	-	-	-	-	-	-	RPS0
		Read/Write (R/W)	-	-	-	-	-	-	-	R/W
		Power-on	-	-	-	-	-	-	-	0
		/RESET and WDT	-	-	-	-	-	-	-	0
		Wake-up from Int	-	-	-	-	-	-	-	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	IAP0	Full Name	Indirect Addressing Pointer 0							
		Bit Name	IAP07	IAP06	IAP05	IAP04	IAP03	IAP02	IAP01	IAP00
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x07	RAMBS1	Full Name	RAM Bank Select 1							
		Bit Name	-	-	-	-	-	RBS12	RBS11	RBS10
		Read/Write (R/W)	-	-	-	-	-	R/W	R/W	R/W
		Power-on	-	-	-	-	-	0	0	0
		/RESET and WDT	-	-	-	-	-	0	0	0
		Wake-up from Int	-	-	-	-	-	P	P	P
0x08	IAP1	Full Name	Indirect Addressing Pointer 1							
		Bit Name	IAP17	IAP16	IAP15	IAP14	IAP13	IAP12	IAP11	IAP10
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x09	IAC1	Full Name	Indirect Addressing Contents 1							
		Bit Name	IAC17	IAC16	IAC15	IAC14	IAC13	IAC12	IAC11	IAC10
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x0A	IAPDR	Full Name	Indirect Address Pointer Direction Control Register							
		Bit Name	-	-	-	-	IAP1_D	IAP0_D	IAP1_D_E	IAP0_D_E
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P
0x0B	LTBL	Full Name	Least Significant Byte of Table Lookup							
		Bit Name	TBL7	TBL6	TBL5	TBL4	TBL3	TBL2	TBL1	TBL0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	IAP0	Full Name	Indirect Addressing Pointer 0							
		Bit Name	IAP07	IAP06	IAP05	IAP04	IAP03	IAP02	IAP01	IAP00
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x07	RAMBS1	Full Name	RAM Bank Select 1							
		Bit Name	-	-	-	-	-	RBS12	RBS11	RBS10
		Read/Write (R/W)	-	-	-	-	-	R/W	R/W	R/W
		Power-on	-	-	-	-	-	0	0	0
		/RESET and WDT	-	-	-	-	-	0	0	0
		Wake-up from Int	-	-	-	-	-	P	P	P
0x08	IAP1	Full Name	Indirect Addressing Pointer 1							
		Bit Name	IAP17	IAP16	IAP15	IAP14	IAP13	IAP12	IAP11	IAP10
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x09	IAC1	Full Name	Indirect Addressing Contents 1							
		Bit Name	IAC17	IAC16	IAC15	IAC14	IAC13	IAC12	IAC11	IAC10
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x0A	IAPDR	Full Name	Indirect Address Pointer Direction Control Register							
		Bit Name	-	-	-	-	IAP1_D	IAP0_D	IAP1_D_E	IAP0_D_E
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P
0x0B	LTBL	Full Name	Least Significant Byte of Table Lookup							
		Bit Name	TBL7	TBL6	TBL5	TBL4	TBL3	TBL2	TBL1	TBL0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	HTBL	Full Name	Most Significant Byte of Table Lookup							
		Bit Name	TBLF	TBLE	TBLD	TBLC	TBLB	TBLA	TBL9	TBL8
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x0D	STKPTR	Full Name	Stack Pointer							
		Bit Name	STKPT7	STKPT6	STKPT5	STKPT4	STKPT3	STKPT2	STKPT1	STKPT0
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Int	P	P	P	P	P	P	P	P
0x0E	RPTC	Full Name	Repeat Pointer							
		Bit Name	RPTC7	RPTC6	RPTC5	RPTC4	RPTC3	RPTC2	RPTC1	RPTC0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x0F	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x10	TCC	Full Name	Time Clock/Counter							
		Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	0	0	0	0	0	0	0	0
0x11	INTF	Full Name	Interrupt Flag							
		Bit Name	-	-	-	PWM0IF	EINT1F	EINT0F	TCCOF	FRCOF
		Read/Write (R/W)	-	-	-	R/W	R/W	R/W	R/W	R/W
		Power-on	-	-	-	0	0	0	0	0
		/RESET and WDT	-	-	-	0	0	0	0	0
		Wake-up from Int	-	-	-	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x12	KWUAIF	Full Name	Port A Key Wake-up Interrupt Flag							
		Bit Name	-	-	-	-	KWU3IF	KWU2IF	KWU1IF	KWU0IF
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	0	0	0	0
0x13	KWUBIF	Full Name	Port B Key Wake-up Interrupt Flag							
		Bit Name	KWU7IF	KWU6IF	KWU5IF	KWU4IF	KWU3IF	KWU2IF	KWU1IF	KWU0IF
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	0	0	0	0	0	0	0	0
0x14	PA	Full Name	General Purpose I/O port, Port A							
		Bit Name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Int	P	P	P	P	P	P	P	P
0x15	PB	Full Name	General Purpose I/O port, Port B							
		Bit Name	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Int	P	P	P	P	P	P	P	P
0x16	PC	Full Name	General Purpose I/O port, Port C							
		Bit Name	-	-	-	PTC4	PTC3	-	-	-
		Read/Write (R/W)	-	-	-	R/W	R/W	-	-	-
		Power-on	-	-	-	U	U	-	-	-
		/RESET and WDT	-	-	-	U	U	-	-	-
		Wake-up from Int	-	-	-	P	P	-	-	-
0x17	PD	Full Name	General Purpose I/O port, Port D							
		Bit Name	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x19	PF	Full Name	General Purpose I/O port, Port F							
		Bit Name	-	-	-	-	PTF3	PTF2	PTF1	PTF0
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	U	U	U	U
		/RESET and WDT	-	-	-	-	U	U	U	U
		Wake-up from Int	-	-	-	-	P	P	P	P
0x1A	LFRC	Full Name	Least Significant Byte of the 16-bit Free Run Counter							
		Bit Name	FRC7	FRC6	FRC5	FRC4	FRC3	FRC2	FRC1	FRC0
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	0	0	0	0	0	0	0	0
0x1B	HFRC	Full Name	Most Significant Byte of 16-bit Free Run Counter							
		Bit Name	FRCF	FRCE	FRCD	FRCC	FRCB	FRCA	FRC9	FRC8
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	0	0	0	0	0	0	0	0
0x1C	LFRCB	Full Name	Least Significant Byte Buffer of the 16-bit Free Run Counter							
		Bit Name	FRCB7	FRCB6	FRCB5	FRCB4	FRCB3	FRCB2	FRCB1	FRCB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	0	0	0	0	0	0	0	0
0x1D	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x1F	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x20	NC	Full Name	LSB Converting Value of ADC							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on		-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x21	DT0L	Full Name	Duty of PWM-Low Byte							
		Bit Name	DT07	DT06	DT05	DT04	DT03	DT02	DT01	DT00
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x22	DT0H	Full Name	Duty of PWM-High Byte							
		Bit Name	DT0F	DT0E	DT0D	DT0C	DT0B	DT0A	DT09	DT08
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x23	PRD0L	Full Name	Period of PWM - Low Byte							
		Bit Name	PRD07	PRD06	PRD05	PRD04	PRD03	PRD02	PRD01	PRD00
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24	PRD0H	Full Name	Period of PWM- High Byte							
		Bit Name	PRD0F	PRD0E	PRD0D	PRD0C	PRD0B	PRD0A	PRD09	PRD08
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x25	DL0L	Full Name	Duty Latch of PWM-Low Byte							
		Bit Name	DL07	DL06	DL05	DL04	DL03	DL02	DL01	DL00
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x26	DL0H	Full Name	Duty Latch of PWM-High Byte							
		Bit Name	DL0F	DL0E	DL0D	DL0C	DL0B	DL0A	DL019	DL08
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x27	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x28	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x29	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x2B	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x2C	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x2D	RFAAR	Full Name	BB Address Register							
		Bit Name	-	-	-	AAR4	AAR3	AAAR2	AAR1	AAR0
		Read/Write (R/W)	-	-	-	R/W	R/W	R/W	R/W	R/W
		Power-on	-	-	-	0	0	0	0	0
		/RESET and WDT	-	-	-	0	0	0	0	0
		Wake-up from Int	-	-	-	P	P	P	P	P
0x2E	RFDB	Full Name	BB Data Buffer							
		Bit Name	RFDB7	RFDB6	RFDB5	RFDB4	RFDB3	RFDB2	RFDB1	RFDB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x2F	RFACR	Full Name	BB Data Read/Write Control Register							
		Bit Name	-	-	-	-	-	RRST	RFRD	RFWR
		Read/Write (R/W)	-	-	-	-	-	R/W	R/W	R/W
		Power-on	-	-	-	-	-	0	1	1
		/RESET and WDT	-	-	-	-	-	0	1	1
		Wake-up from Int	-	-	-	-	-	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x30	RFINTF	Full Name	BB Interrupt Flag Register							
		Bit Name	CSDF	TX_AEF	RX_AFF	TX_EMPTYF	RX_OFF	LINK_DISF	LOCK_OUTF	LOCK_INF
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x40 ~ 0x7F	DPR	Full Name	Dual Port Registers (64 in total)							
		Bit Name	DPR7	DPR6	DPR5	DPR4	DPR3	DPR2	DPR1	DPR0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	X	X	X	X	X	X	X	X
		/RESET and WDT	X	X	X	X	X	X	X	X
		Wake-up from Int	P	P	P	P	P	P	P	P
0x80	PRIE	Full Name	Peripheral Function Enable							
		Bit Name	-	USBE	WME	-	-	PWME	TCCE	FRCE
		Read/Write (R/W)	-	R/W	R/W	-	-	R/W	R/W	R/W
		Power-on	-	0	0	-	-	0	0	0
		/RESET and WDT	-	0	0	-	-	0	0	0
		Wake-up from Int	-	P	P	-	-	P	P	P
0x81	INTE	Full Name	Interrupt Enable Control Register							
		Bit Name	GIE	-	-	PWM0IE	EINT1E	EINT0E	TCCOE	FRCOE
		Read/Write (R/W)	R/W	-	-	R/W	R/W	R/W	R/W	R/W
		Power-on	0	-	-	0	0	0	0	0
		/RESET and WDT	0	-	-	0	0	0	0	0
		Wake-up from Int	P	-	-	P	P	P	P	P
0x82	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x83	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x84	EINTED	Full Name	External Interrupt Edge Control							
		Bit Name	SYNB2	SYNB1	SYNB0	-	-	-	EINT1ED	EINT0ED
		Read/Write (R/W)	R/W	R/W	R/W	-	-	-	R/W	R/W
		Power-on	0	0	0	-	-	-	0	0
		/RESET and WDT	0	0	0	-	-	-	0	0
		Wake-up from Int	P	P	P	-	-	-	P	P
0x85	SPIC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x86	IOCA	Full Name	I/O Control of Port A							
		Bit Name	IOCA7	IOCA6	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Int	P	P	P	P	P	P	P	P
0x87	IOCB	Full Name	I/O Control of Port B							
		Bit Name	IOCB7	IOCB5	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Int	P	P	P	P	P	P	P	P
0x88	IOCC	Full Name	I/O Control of Port C							
		Bit Name	-	-	-	IOCC4	IOCC3	-	-	-
		Read/Write (R/W)	-	-	-	R/W	R/W	-	-	-
		Power-on	-	-	-	1	1	-	-	-
		/RESET and WDT	-	-	-	1	1	-	-	-
		Wake-up from Int	-	-	-	P	P	-	-	-
0x89	IOCD	Full Name	I/O Control of Port D							
		Bit Name	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x8A	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x8B	IOCF	Full Name	I/O Control of Port F							
		Bit Name	-	-	-	-	IOCF3	IOCF2	IOCF1	IOCF0
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	1	1	1	1
		/RESET and WDT	-	-	-	-	1	1	1	1
		Wake-up from Int	-	-	-	-	P	P	P	P
0x8C	PUCA	Full Name	Pull-up control of Port A							
		Bit Name	PUCA7	PUCA6	PUCA5	PUCA4	PUCA3	PUCA2	PUCA1	PUCA0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x8D	PUCB	Full Name	Pull-up control of Port B							
		Bit Name	PUCB7	PUCB6	PUCB5	PUCB4	PUCB3	PUCB2	PUCB1	PUCB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x8E	PUCC	Full Name	Pull-up control of Port C							
		Bit Name	-	-	-	PUCC4	PUCC3			
		Read/Write (R/W)	-	-	-	R/W	R/W			
		Power-on	-	-	-	0	0			
		/RESET and WDT	-	-	-	0	0			
		Wake-up from Int	-	-	-	P	P			
0x8F	PUCD	Full Name	Pull-up control of Port D							
		Bit Name	PUCD7	PUCD6	PUCD5	PUCD4	PUCD3	PUCD2	PUCD1	PUCD0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x90	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x91	PUCF	Full Name	Pull-up Control of Port F							
		Bit Name	-	-	-	-	PUCF3	PUCF2	PUCF1	PUCF0
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P
0x92	ODCB	Full Name	Open Drain Control of Port B							
		Bit Name	OPCB7	OPCB6	OPCB5	OPCB4	OPCB3	OPCB2	OPCB1	OPCB0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	0	0	0
0x93	TCCC	Full Name	Time Clock/Counter Control							
		Bit Name	-	-	-	-	TCCS0	PS2	PS1	PS0
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P
0x94	FRCC	Full Name	Free Run Counter Control/OSCO2 Output Control							
		Bit Name	-	OSC02E	OSCO2 SL1	OSCO2 SL0	PPSCL2	PPSCL1	PPSCL0	FRCCS
		Read/Write (R/W)	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x95	WDTC	Full Name	Watchdog Timer Control							
		Bit Name	GREEN	-	-	WDTCE	-	RAT2	RAT1	RAT0
		Read/Write (R/W)	R/W	-	-	R/W	-	R/W	R/W	R/W
		Power-on	0	-	-	0	-	0	0	0
		/RESET and WDT	0	-	-	0	-	0	0	0
		Wake-up from Int	0	-	-	P	-	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x96	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x97	NC	Full Name	No Connection							
		Bit Name	-	-	-	-	-	-		
		Read/Write (R/W)	-	-	-	-	-	-		
		Power-on	-	-	-	-	-	-		
		/RESET and WDT	-	-	-	-	-	-		
		Wake-up from Int	-	-	-	-	-	-		
0x98	PWMCR	Full Name	PWM Control Register							
		Bit Name	-	-	-	-	-	S_PWM0	-	-
		Read/Write (R/W)	-	-	-	-	-	R/W	-	-
		Power-on	-	-	-	-	-	0	-	-
		/RESET and WDT	-	-	-	-	-	0	-	-
		Wake-up from Int	-	-	-	-	-	P	-	-
0x99	RFINTE	Full Name	BB Interrupt Enable Control Register							
		Bit Name	CSDE	TX_AEE	RX_AFE	TX_EMPTYE	RX_OFE	LINK_ DISE	LOCK_OUTE	LOCK_ INE
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1CC			Reserved							
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
			-	-	-	-	-	-	-	-
0x1CD	GCNTR	Full Name	USB General Control Register							
		Bit Name	-	-	-	-	RESUME	SUSPEND	PLUG	URST
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1CE	EP1CNTR	Full Name	End Point 1 Control Register							
		Bit Name	-	-	EP1EN	-	-	EP1DIR	EP1TP1	EP1TP0
		Read/Write (R/W)	-	-	R/W			R/W	R/W	R/W
		Power-on	-	-	0	-	-	1	0	0
		/RESET and WDT	-	-	0	-	-	1	0	0
		Wake-up from Int	-	-	P	-	-	P	P	P
0x1CF	EP2CNTR	Full Name	End Point 2 Control Register							
		Bit Name	-	-	EP2EN	-	-	EP2DIR	EP2TP1	EP2TP0
		Read/Write (R/W)	-	-	R/W	-	-	R/W	R/W	R/W
		Power-on	-	-	0	-	-	1	0	0
		/RESET and WDT	-	-	0	-	-	1	0	0
		Wake-up from Int	-	-	P	-	-	P	P	P
0x1D0	EP3CNTR	Full Name	End Point 3 Control Register							
		Bit Name	-	-	EP3EN	-	-	EP3DIR	EP3TP1	EP3TP0
		Read/Write (R/W)	-	-	R/W	-	-	R/W	R/W	R/W
		Power-on	-	-	0	-	-	1	0	0
		/RESET and WDT	-	-	0	-	-	1	0	0
		Wake-up from Int	-	-	P	-	-	P	P	P
0x1D1	EPINTR	Full Name	Endpoint Interrupt Event Status Register							
		Bit Name	-	-	INT3	INT2	INT1	INT0IN	INT0TX	INT0RX
		Read/Write (R/W)	-	-	R/W	R/W	R/W	R/W	R/W	R
		Power-on	-	-	0	0	0	1	0	0
		/RESET and WDT	-	-	0	0	0	1	0	0
		Wake-up from Int	-	-	P	P	P	P	P	P
0x1D2	EPINTE	Full Name	Endpoint Interrupt Event Enable Control Register							
		Bit Name	-	-	INT3E	INT2E	INT1E	INT0INE	INT0TXE	INT0RXE
		Read/Write (R/W)	-	-	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	-	0	0	0	0	0	0
		/RESET and WDT	-	-	0	0	0	0	0	0
		Wake-up from Int	-	-	P	P	P	P	P	P
0x1D3	STAINTR	Full Name	State Interrupt Event Flag Register							
		Bit Name	-	-	-	-	FRWPINT	RUEINT	IDLEINT	RSTINT
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D4	STAINTE	Full Name	State Interrupt Event Enable Control Register							
		Bit Name	-	-	-	-	FRWPINTE	RUEINTE	IDLEINTE	RSTINTE
		Read/Write (R/W)	-	-	-	-	R/W	R/W	R/W	R/W
		Power-on	-	-	-	-	0	0	0	0
		/RESET and WDT	-	-	-	-	0	0	0	0
		Wake-up from Int	-	-	-	-	P	P	P	P
0x1D5	FAR	Full Name	Function Address							
		Bit Name	-	FADDR6	FADDR5	FADDR4	FADDR3	FADDR2	FADDR1	FADDR0
		Read/Write (R/W)	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x1D6	EP0RXTR	Full Name	Endpoint 0 RX Token							
		Bit Name	-	-	-	-	-	USETUPOW	USETUP	UOUT
		Read/Write (R/W)	-	-	-	-	-	R/W	R/W	R/W
		Power-on	-	-	-	-	-	0	0	0
		/RESET and WDT	-	-	-	-	-	0	0	0
		Wake-up from Int	-	-	-	-	-	P	P	P
0x1D7	EP0RXCSR	Full Name	Endpoint 0 RX Command/Status							
		Bit Name	CDTOG0RX	ERRSTS0RX	STALLSTS0RX	ACKSTS0RX	DTOGERR0RX	DTOG0RX	SESTALL0RX	RXEN0RX
		Read/Write (R/W)	W	R	R	R	R	R	R/W	R/W
		Power-on	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1D8	EP0TXCSR	Full Name	Endpoint 0 TX Command/Status							
		Bit Name	CDTOG0TX	ERRSTS0TX	STALLSTS0TX	ACKSTS0TX	-	DTOG0TX	SESTALL0TX	TXEN0TX
		Read/Write (R/W)	W	R	R	R	-	R	R/W	R/W
		Power-on	0	0	0	0	-	1	1	0
		/RESET and WDT	0	0	0	0	-	1	1	0
		Wake-up from Int	P	P	P	P	-	P	P	P
0x1D9	EP1CSR	Full Name	Endpoint 1 Command/Status							
		Bit Name	CDTOG1	ERRSTS1	STALLSTS1	ACKSTS1	DTOGERR1	DTOG1	SESTALL1	RXTXEN1
		Read/Write (R/W)	W	R	R	R	R	R	R/W	R/W
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1DA	EP2CSR	Full Name	Endpoint 2 Command/Status							
		Bit Name	CDTOG2	ERRSTS2	STALLSTS2	ACKSTS2	DTOGERR2	DTOG2	SESTALL2	RXTXEN2
		Read/Write (R/W)	W	R	R	R	R	R	R/W	R/W
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1DB	EP3CSR	Full Name	Endpoint 3 Command/Status							
		Bit Name	CDTOG3	ERRSTS3	STALLSTS3	ACKSTS3	DTOGERR3	DTOG3	SESTALL3	RXTXEN3
		Read/Write (R/W)	W	R	R	R	R	R	R/W	R/W
		Power-on	0	0	0	0	0	0	1	0
		/RESET and WDT	0	0	0	0	0	0	1	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1DC	EP0RXCTR	Full Name	Endpoint 0 RX Count							
		Bit Name	-	EP0RXCT6	EP0RXCT5	EP0RXCT4	EP0RXCT3	EP0RXCT2	EP0RXCT1	EP0RXCT0
		Read/Write (R/W)	-	R	R	R	R	R	R	R
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x1DD	EP0TXCTR	Full Name	Endpoint 0 TX Count							
		Bit Name	-	EP0TXCT6	EP0TXCT5	EP0TXCT4	EP0TXCT3	EP0TXCT2	EP0TXCT1	EP0TXCT0
		Read/Write (R/W)	-	R	R	R	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x1DE	EP1CTR	Full Name	Endpoint 1 Count							
		Bit Name	-	EP1CT6	EP1CT5	EP1CT4	EP1CT3	EP1CT2	EP1CT1	EP1CT0
		Read/Write (R/W)	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x1DF	EP2CTR	Full Name	Endpoint 2 Count							
		Bit Name	-	EP2CT6	EP2CT5	EP2CT4	EP2CT3	EPCT2	EP2CT1	EP2CT0
		Read/Write (R/W)	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E0	EP3CTR	Full Name	Endpoint 3 Count							
		Bit Name	-	EP3CT6	EP3CT5	EP3CT4	EP3CT3	EP3CT2	EP3CT1	EP3CT0
		Read/Write (R/W)	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	-	0	0	0	0	0	0	0
		/RESET and WDT	-	0	0	0	0	0	0	0
		Wake-up from Int	-	P	P	P	P	P	P	P
0x1E1	EP0RXDAR	Full Name	Endpoint 0 RX Data							
		Bit Name	EP0RX7	EP0RX6	EP0RX5	EP0RX4	EP0RX3	EP0RX2	EP0RX1	EP0RX0
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1E2	EP0TXDAR	Full Name	Endpoint 0 TX Data							
		Bit Name	EP0TX7	EP0TX6	EP0TX5	EP0TX4	EP0TX3	EP0TX2	EP0TX1	EP0TX0
		Read/Write (R/W)	W	W	W	W	W	W	W	W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1E3	EP1DAR	Full Name	Endpoint 1 Data							
		Bit Name	EP1D7	EP1D6	EP1D5	EP1D4	EP1D3	EP1D2	EP1D1	EP1D0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1E4	EP2DAR	Full Name	Endpoint 2 Data							
		Bit Name	EP2D7	EP2D6	EP2D5	EP2D4	EP2D3	EP2D2	EP2D1	EP2D0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1E5	EP3DAR	Full Name	Endpoint 3 Data							
		Bit Name	EP3D7	EP3D6	EP3D5	EP3D4	EP3D3	EP3D2	EP3D1	EP3D0
		Read/Write (R/W)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1E6	HGSR	Full Name	Reserved							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x1E7	HINTR	Full Name	Hub Interrupt Event Flag Register							
		Bit Name	-	SOFINT	-	-	-	-	-	-
		Read/Write (R/W)	-	R/W	-	-	-	-	-	-
		Power-on	-	0	-	-	-	-	-	-
		/RESET and WDT	-	0	-	-	-	-	-	-
		Wake-up from Int	-	P	-	-	-	-	-	-
0x1E8	HINTE	Full Name	Hub Interrupt Event Enable Control Register							
		Bit Name	-	SOFINTE	-	-	-	-	-	-
		Read/Write (R/W)	-	R/W	-	-	-	-	-	-
		Power-on	-	0	-	-	-	-	-	-
		/RESET and WDT	-	0	-	-	-	-	-	-
		Wake-up from Int	-	P	-	-	-	-	-	-
0x1E9 ~ 0x1FD		Full Name	Reserved							
		Bit Name	-	-	-	-	-	-	-	-
		Read/Write (R/W)	-	-	-	-	-	-	-	-
		Power-on	-	-	-	-	-	-	-	-
		/RESET and WDT	-	-	-	-	-	-	-	-
		Wake-up from Int	-	-	-	-	-	-	-	-
0x1FE	FNLR	Full Name	Least Significant Byte of the Frame Number							
		Bit Name	FN7	FN6	FN5	FN4	FN3	FN2	FN1	FN0
		Read/Write (R/W)	R	R	R	R	R	R	R	R
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Int	P	P	P	P	P	P	P	P
0x1FF	FNHR	Full Name	Most Significant Byte of the Frame Number							
		Bit Name	-	-	-	-	-	FNA	FN9	FN8
		Read/Write (R/W)	-	-	-	-	-	R	R	R
		Power-on	-	-	-	-	-	0	0	0
		/RESET and WDT	-	-	-	-	-	0	0	0
		Wake-up from Int	-	-	-	-	-	P	P	P

7 Function Description

7.1 Special Purpose Registers

The special purpose registers are function-oriented registers used by the CPU to access memory, record execution results, and carry out the desired operation. The functions of the registers related to the core are described in the following subsections

7.1.1 Accumulator – ACC

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

7.1.2 Indirect Addressing Contents – IAC0 (0x00) and IAC1 (0x09)

The contents of R0 and R9 are implemented as indirect addressing pointers if any instruction uses R6 and R8 as registers.

7.1.3 Program Counter HPC (0x01) and LPC (0x02)

- The Program Counter (PC) is composed of registers HPC and LPC.
- The PC and the hardware stacks are 14 bits wide.
- The structure is depicted in Fig. 6-1.
- Generates 12K × 16 on-chip ROM addresses to the corresponding program memory (ROM).
- All the bits of PC are set to "0"s as a reset condition occurs.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of the stack.
- "MOV R2, A" allows the loading of an address from the "A" register to the lower 8 bits of the PC, and the high byte (A8~A14) of the PC remain unchanged.
- "ADD R2, A" & "TBL" allows a corresponding address / offset to be added to the current PC.

7.1.4 Status Register –SR (0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	RST	T	P	Z	DC	C

Bit 0 (C): Carry flag. This bit indicates that a carry out of ALU occurred during the last arithmetic operation. This bit is also affected during bit test, branch instruction and during bit shifts.

Bit 1 (DC): Auxiliary carry flag. This bit is set during ADD and ADC operations to indicate that a carry occurred between Bit 3 and Bit 4.

Bit 2 (Z): Zero flag. Set to "1" if the result of the last arithmetic, data or logic operation is zero.

Bit 3 (P): Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" command and the "WDTC" command, or during power up and reset to 0 by WDT timeout.

Bit 5 (RST): Set if the CPU wakes up by keying on the wake-up pins. Reset if the chip wakes up through other ways.

Bits 6 and 7 are reserved.

7.1.5 RAM Bank Selector – RAMBS0 (0x04) and RAMBS1 (0x07)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	RAMBSX2	RAMBSX1	RAMBSX0

As depicted in Fig. 6-2, there are six available banks in the MCU. Each of them has 128 registers and can be accessed by defining the bits, RAMBSX0 ~ RAMBSX2, as shown below.

RAMBSX (0x04/0x07)	Bank
000	0
001	1
010	2
011	3
100	4
101	5

7.1.6 ROM Page Selector – ROMPS (0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	RPS0

As depicted in Fig. 6-1, there are two available pages in MCU. The first page has 8K*16 ROM size and the second page has 4K×16 ROM size. Both of them can be accessed by defining the bits, RPS0, as shown below.

RPS0	Page (Address)
0	0 (0x0000~0x1FFF)
1	1 (0x2000~0x2FFF)

7.1.7 Indirect Addressing Pointers – IAP0 (0x06), and IAP1 (0x08)

Both R6 and R8 are not physically implemented registers. They are useful as indirect addressing pointers. Any instruction using R6/R4 and R8/R7 as registers actually access data pointed by R0 and R9 individually.

7.1.8 Indirect Address Pointer Direction Control Register – IAPDR (0x0A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	IAP1_D	IAP0_D	IAP1_D_E	IAP0_D_E

Bit 0/1 (IAP0_D_E/IAP1_D_E) Indirect addressing Pointer 0/1 direction function enable bit.

0: Disable

1: Enable

Bit 2/3 (IAP0_D/IAP1_D) Indirect addressing pointer0/1 direction control bit.

0: Minus direction

1: Plus direction

7.1.9 Table Look-up Pointers – LTBL (0x0B), and HTBL (0x0C)

The maximum length of a table is 64K, and can be accessed through registers LTBL and HTBL. HTBL is the high byte of the pointer, whereas LTBL is the low byte.

7.1.10 Stack Pointer – STKPTR (0x0D)

Register RD indicates how many stacks the current free run program uses. It is a read only register.

7.1.11 Repeat Counter – RPTC (0x0E)

The RE register is used to set how many times the “RPT” instruction is going to read the table.

7.1.12 Real Time Clock Counter – RTCC (0x10)

TCC counter.

7.1.13 Interrupt Flag Register – INTF (0x11)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	PWM0IF	EINT1F	EINT0F	TCCOF	FRCOF

Bit 0 (FRCOF): FRC Overflow interrupt. Set as the contents of the FRC counter change from 0xFFFF to 0x0000, reset by software.

Bit 1 (TCCOF): TCC Overflow interrupt. Set as the contents of the TCC counter change from 0xFF to 0x00, reset by software.

Bits 2 ~ 3 (EINT0F & EINTIF): External input pin interrupt flag. Interrupt occurs at the defined edge of the external input pin, reset by software.

Bit 4 (PWM0IF): PWM interrupt flag. Interrupt occurs when TMRX is equal to PRDX, reset by software.

Bits 5 ~ 7 reserved

Each bit can function independently regardless whether its related interrupt mask bit is enabled or not.

Each bit can function independently no matter its related interrupt mask bit is enabled or not.

7.1.14 Key Wake-up Flag Register – KWUAIF (0x12) and KWUBIF (0x13)

KWUAIF: Port A Key Wake-up Interrupt Flag

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	KWUBIF	KWUAIF	KWU9IF	KWU8IF

KWUBIF: Port B Key Wake-up Interrupt Flag

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KWU7IF	KWU6IF	KWU5IF	KWU4IF	KWU3IF	KWU2IF	KWU1IF	KWU0IF

7.1.15 I/O Port Registers – PTA ~ PTF (0x14 ~ 0x19)

PTX can be operated as any other general purpose registers by related instructions. That is, PTX is an 8-bit, bi-directional, general purpose port. Its corresponding IO control bit determines the data direction of a PTX pin.

7.1.16 16-bit Free Run Counter (FRC) – LFRC (0x1A) HFRC (0x1B) and LFRCB (0x1C)

R1A is a 16-bit FRC low byte; R1B is high byte; R1C is a low byte buffer.

7.1.17 PWM Duty – DT0L (0x21)/DT0H (0x22)

R22:R21 16-bit PWM0 output duty cycle.

7.1.18 PWM Period – PRD0L (0x23)/PRD0H (0x24)

R24:R23 16-bit PWM output period cycle.

7.1.19 PWM Duty Latch – DL0L (0x25)/DL0H (0x26)

R26:R25 16-bit PWM output duty cycle buffer.

7.1.20 BB Address Register – RFAAR (0x2D)

Register R2D indicates BB indirect RAM address.

7.1.21 BB Data Buffer Register – RFDB (0x2E)

Register R2E indicates BB indirect RAM data.

7.1.22 BB Data Read/Write Control Register – RFACR (0x2F)

Register R2F indicates WM RAM access control.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	RRST	RFRD	RFWR

Bit 0 (RFWR): Write BB register

Bit 1 (RFRD): Read BB register

Bit 2 (RRST): BB S/W reset

Bit 3~Bit 7: reserved

7.1.23 BB Interrupt Flag Register – RFINTF (0x30)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSDF	TX_AEF	RX_AFF	TX_ EMPTYF	RX_OFF	LINK_ DISF	LOCK_OUTF	LOCK_ INF

Bit 0 (LOCK_INF): This bit reflects the LOCK IN flag interrupt.

Bit 1 (LOCK_OUTF): This bit reflects the LOCK OUT flag interrupt.

Bit 2 (LINK_DISF): This interrupt is invoked by the zero counter capacitor discharge mechanism.

Bit 3 (RX_OFF): This bit reflects the RX FIFO full flag interrupt.

Bit 4 (TX_EMPTYF): This bit reflects the TX EMPTY flag interrupt.

Bit 5 (RX_AFF): This bit reflects the RX FIFO almost full flag interrupt.

Bit 6 (TX_AEF): This bit reflects the TX FIFO almost empty flag interrupt.

Bit 7 (CSDF): This flag indicates that a carrier-sense interrupt has occurred.

7.2 Dual Port Register (0x40 ~ 0x7F)

R 40 ~ R7F are dual port register.

7.3 System Status, Control and Configuration Registers

These registers are function-oriented registers used by the CPU to record, enable or disable the peripheral modules, interrupts, and the operation clock modes.

7.3.1 Peripherals Enable Control – PRIE (0x80)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	USBE	BBE	-	-	PWM0E	TCCE	FRCE

Bit 0 (FRCE): Free Run Counter 0 (FRC0) Enable bit

Bit 1 (TCCE): Timer Clock/Counter (TCC) Enable bit

Bit 2 (PWM0E): PWM0 function enable bit

Bit 5 (BBE): Base band (BB) Enable bit

Bit 6 (USBE): Universal Serial Bus (USB) Enable bit

Bits 3, 4, 7: Reserved

0: disable function

1: enable function

7.3.2 Interrupts Enable Control – INTE (0x81)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	-	-	PWM0IE	EINT1E	EINT0E	TCCOE	FRCOE

Bit 0 (FRC0OE): Free Run Counter (FRC) Overflow interrupt enable bit.

Bit 1 (TCCOE): TCC (TCC) Overflow interrupt enable bit**.**

Bit 2 (EINT0E): External pin (EINT0) interrupt enable bit.

Bit 3 (EINT1E): External pin (EINT1) interrupt enable bit.

Bit 4 (PWM0IE): PWM0 period complete enable bit.

Bits 5, 6: Reserved

0: disable function interrupt

1: enable function interrupt

Bit 7 (GIE): Global interrupt control bit. Global interrupt is enabled by the ENI and RETI instructions and is disabled by the DISI instruction.

0: Global interrupt disable

1: Global interrupt enable

7.3.3 Key Wake-up Enable Control – KWUAIE (0x82) and KWUBIE (0x83)

KWUAIE: Port A Key Wake-up Interrupt Enable Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	KWUBE	KWUAE	KWU9E	KWU8E

Bit 0 ~Bit 3 (KWU8E ~ KWUBE): Enable or disable the PTA0 ~ PTA3 Key Wake-up function.

0: disable key wake-up function

1: enable key wake-up function

KWUBIE: Port B Key Wake-up Interrupt Enable Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KWU7E	KWU6E	KWU5E	KWU4E	KWU3E	KWU2E	KWU1E	KWU0E

Bit 0 ~Bit 7 (KWU0 ~ KWU7): Enable or disable the PTB0 ~ PTB7 Key Wake-up function.

0: disable key wake-up function

1: enable key wake-up function

7.3.4 External Interrupts Edge Control – EINTED (0x84)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						EINT1ED	EINT0ED

Bit 0 (EINT0ED): Define which edge as an interrupt source for EINT0.

Bit 1 (EINT1ED): Define which edge as an interrupt source for EINT1.

0: Falling Edge

1: Rising Edge

Bit 2 ~ **Bit 7:** reserved

7.3.5 I/O Control Registers – IOCA~IOCF (0x86~0x8B)

OCX is used to determine the data direction of its corresponding I/O port bit.

0: configure a selected I/O pin as output

1: configure a selected I/O pin as input

The only four least significant bits of Port F and the only five least significant bits of Port C are available

7.3.6 Pull-up Resistance Control Registers for Ports – PUCA~PUCF (0x8C ~ 0x91)

Each bit of PUCX is used to control the pull-up resistors attached to its corresponding pin respectively. The theoretical value of the resistor is 50 KΩ. However, due to process variation, ±35% variation in resistance must be taken into consideration.

PUCX:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PUCX7	PUCX6	PUCX5	PUCX4	PUCX3	PUCX2	PUCX1	PUCX0

0: Pull-up Resistors disconnected

1: Pull-up Resistors attached

7.3.7 Open Drain Control Registers of Port B – ODCB (0x92)

ODCB: Open drain control of Port B.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPCB7	OPCB6	OPCB5	OPCB4	OPCB3	OPCB2	OPCB1	OPCB0

0: Open drain disable

1: Open drain enable

7.3.8 Timer Clock Counter Controller – TCCC (0x93)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	TCCS0	PSR2	PSR1	PSR0

Bits 0 ~ 2 (PSR0 ~ PSR2): Prescaler for TCC.

PSR2	PSR1	PSR0	Clock Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (TCCS0): Clock Source Select

TCCS0	Clock Source
0	Selected PLL Clock Source
1	Selected IRC Clock Source

Bits 4 ~ 7: Reserved

7.3.9 Free Run Counter Controller – FRCC (0x94)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	OSCO2E	OSCO2SL1	OSCO2SL0	PPSCL2	PPSCL1	PPSCL0	FRCCS

Bit 0 (FRCCS): Clock Source Select.

FRCCS	Clock Source
0	Selected PLL Clock Source
1	Selected IRC Clock Source

Bit 1 ~ 3 (PSR0 ~ PSR2): Prescaler for the OSCO2 clock output.

PPSCL2	PPSCL1	PPSCL0	Clock Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 4 and Bit 5 (OSCO2SL0 and OSCO1SL1): System Clock Frequency Select Control Bits

OSCO2SL0	OSCO2SL1	Output Frequency (MHz)
0	0	6
0	1	12
1	0	24
1	1	48

Bit 6 (OSCO2E): Enable the OSCO2 output.

0: OSCO2 disabled, output low;

1: OSCO2 enabled.

Bit 7 is reserved.

7.3.10 Watchdog Timer Controller – WDTC (0x95)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GREEN	-	-	WDTCE	-	RAT2	RAT1	RAT0

Bit 0 ~ 2 (RAT0 ~ RAT2): Prescaler of WDT.

RAT2	RAT1	RAT0	Clock Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 4 (WDTCE): Enable the WDT Counter

0: WDT disabled

1: WDT enabled

Bits 7 (GREEN): for power saving purposes, the system clock can be changed to external RC mode.

0: Normal Mode

1: Green Mode

Bit 3, 5 and 6 are reserved.

7.3.11 PWM Control Register – PWMCR (0x98)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	S_PWM0	-	-

Bit 2 (S_PWM0): Selected PWM0 output enable.

0: disable PWM output

1: enable PWM output

Bits 0, 1 and 3 ~ 7 are reserved.

7.3.12 BB Interrupt Control Register – RFINTE (0x99)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSDE	TX_AEE	RX_AFE	TX_ EMPTYE	RX_OFE	LINK_ DISE	LOCK_OUTE	LOCK_ INE

Bit 0 (LOCK_INE): LOCK IN interrupt enable bit.

Bit 1 (LOCK_OUTE): LOCK OUT interrupt enable bit.

Bit 2 (LINK_DISE): LINK_DIS interrupt enable bit.

Bit 3 (RX_OFE): The RX FIFO full interrupt enable bit.

Bit 4 (TX_EMPTYE): The TX EMPTY interrupt enable bit.

Bit 5 (RX_AFE): The RX FIFO almost full interrupt enable bit.

Bit 6 (TX_AEE): The TX FIFO almost empty interrupt enable bit.

Bit 7 (CSDE): The carrier-sense interrupt enable bit.

0: disable function interrupt

1: enable function interrupt

7.4 USB Status, Control and Configuration Registers

These registers are function-oriented registers used by the USB to record, enable or disable the peripheral modules, interrupts, and the operation clock modes. See Section 9.5.

7.5 Code Option Code Option (ROM-0x2FFF)

Register SCLK is located on the very last bit of EM77930's 12K program ROM. These values will be fetched first to be the system initial values during power-on.

SCLKC: System Clock Control Register

SCLKC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2FFF	-	-	-	USBCLK	RFCLK1	RFCLK0	SCLK1	SCLK0

SCLKC	15	14	13	12	11	10	9	8
0x2FFF	-	-	-	-	-	-	-	-

Bit 0 ~ Bit 1 (SCLK0 ~ SCLK1): System Clock Frequency Select Control Bits

SCLK1	SCLK0	System Clock (MHz)
0	0	6
0	1	12
1	0	24
1	1	48

Bits 2~3 (RFCLK0~RFCLK1): Wireless Modem Clock Frequency Select Control Bits

RFCLK1	RFCLK0	System Clock (MHz)
0	0	6
0	1	12
1	0	24
1	1	48

Bit 4 (USBCLK): USB 48MHz PLL Clock Source Control Bit

0: Disable 48 MHz oscillation from PLL.

1: Enable 48 MHz oscillation from PLL for USB during power-on.

Bits 5 ~ 15: Reserved

SCLK [1:0]	RFCLK [1:0]	USB_ CLK	WDT_ CON.GREEN	SYS CLK	RF CLK	USB CLK
00	00	0	0	6 (Bypass)	6 (Bypass)	6 (Bypass)
00/01/10/11	01/10/11	0	0	6/12/24/48	12/24/48	48
01/10/11	00/01/10/11	0	0	12/24/48	6/12/24/48	48
00/01/10/11	00/01/10/11	1	0	6/12/24/48	6/12/24/48	48
00/01/10/11	00/01/10/11	0/1	1	IRC	-	-

8 Base Band (BB)

8.1 BB: Standard Interface to the RFW102 Series

8.1.1 Features

- Parallel interface to RFW102 modem.
- Serial to Parallel conversion of RFW102 interface.
- Input FIFO (RX_FIFO).
- Output FIFO (TX_FIFO).
- Preamble Correlation.
- Packet Address Filter (Network and unique).

- CRC calculation
- Working Frequencies: 6-24MHz
- Power Saving modes: Idle mode, Power-down mode
- Inter-RFWAVES networks Carrier-sense
- Discharge of the RFW-102 reference capacitor
- Compensate for clock drifts between the transmitting EM77930 and the receiving EM77930 up to 1000ppm. Hence, the EM77930 requires low performance crystal.
- Interrupt Driver – connected to the EM77930's internal interrupt and informs the EM77930 about BB events.

8.1.2 Description

RFWAVES has developed a very low cost wireless modem (RFW102) for short range, cost-sensitive applications. The modem is a physical layer element (PHY) – allowing the transmission and reception of bits from one end to the other.

In an RFWAVES application, the MCU is in charge of the MAC layer protocol. In order to reduce the real-time demands of the MCU handling the MAC protocol, the BB was developed. The BB enables the MCU an easy interface to RFW102 through a parallel interface, similar to memory access. It converts the fast serial input to 8-bit words, which are much easier for an 8-bit MCU to work with and requires a lower rate oscillator. It buffers the input through a TBD bytes FIFO, enabling the MCU to access the BB more efficiently. Instead of reading one byte per interrupt, the MCU can read up to 16 bytes in each interrupt. This reduces the MCU overhead in reading incoming words, insofar as stack stuffing and pipeline emptying are concerned, in cases where each incoming byte causes an interrupt. When using the FIFO, the MCU pays the same overhead for all the FIFO bytes as it paid for only one byte without a FIFO.

Having a low-cost BB with a built-in state machine that can support basic wireless communication elements would present the following advantages:

- Shorter development time, hence shorter time to market.
- Save CPU power and other resources for other applications.
- Offer an easy, standard integrated solution.

8.1.3 I/O and Package Description

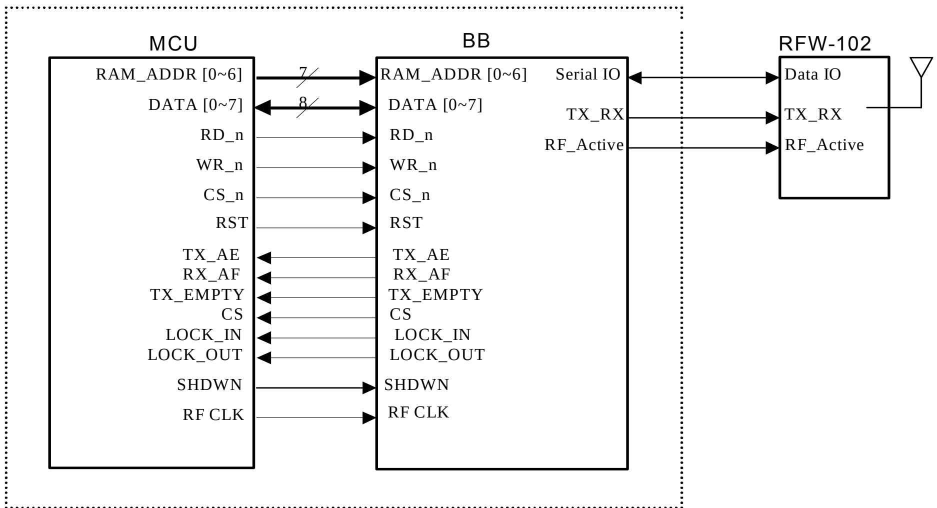


Fig. 8-1 Parallel Interface between the MCU and RFW-102 through BB

Name	Type	Description
DATA [0-7]	I/O	This bus comprises of eight TRI-STATE input/output lines. The bus provides bidirectional communication between the system and the MCU. Data, control words, and status information are transferred via the DATA [0-7] data bus.
RD_n	I	When RD_n is low while the system is enabled, BB outputs one of its internal register values to DATA[0-7] according to RAM_ADDR[0-6].
WR_n	I	When WR_n is low while the system is enabled, BB enables writing to its internal registers. The register is determined by RAM_ADDR [0-6] and the value DATA[0-7].
RAM_ADDR[0-6]	I	These four input signals determine the register to which the MCU writes to or reads from.
CS_n	I	Chip select input pin. When CS_n is low, the chip is selected; when high, the chip is disabled. This pin overrides all pins excluding RST. This enables communication between BB and the MCU. This pin functions as wake-up pin for power-down and idle modes.
TX_AE TX_EMPTY RX_AF CS LOCK_IN LOCK_OUT	O	Interrupt driver pins. This pin goes high whenever any of the interrupt sources has an active high condition and is enabled via the IER. The purpose of this pin is to notify the MCU through its external interrupt pin that an event (such as empty TX_FIFO) has occurred. Goes low when IER register is read.

Name	Type	Description
RST	I	Chip's reset pin. When this pin is set high, all registers and FIFOs are cleared to their initial values. All transceiver traffic is disabled and aborted. Reset is asynchronous to system clock. After power-up, a pulse in RST input should be applied (by POR).
SHDWN	I	Shut Down BB
RF_ACTIVE	O	This output pin controls the RFW102 working/shutdown mode. Its values are determined by SCR4(1).
SERIAL_IO	I/O	Serial input or output according to TX_RX mode. It functions as serial interface for the RFW-102 (RFWAVES modem). When SERIAL_IO is input, it is a Schmitt-trigger input.
RX_TX	O	This pin controls the RFW-102 operation mode. It should be connected to RFW-102 RX_TX input pin. When RX_TX is low, RFW-102 is in receiving mode. When RX_TX is high, RFW-102 is in transmitting mode. In most cases RX_TX output pin is determined by SCR2(0) register. SCR3(7) and the capacitor discharge mechanism has effects on this pin.
RF_CLK	I	Clock for RF operation

8.1.4 BB Architecture

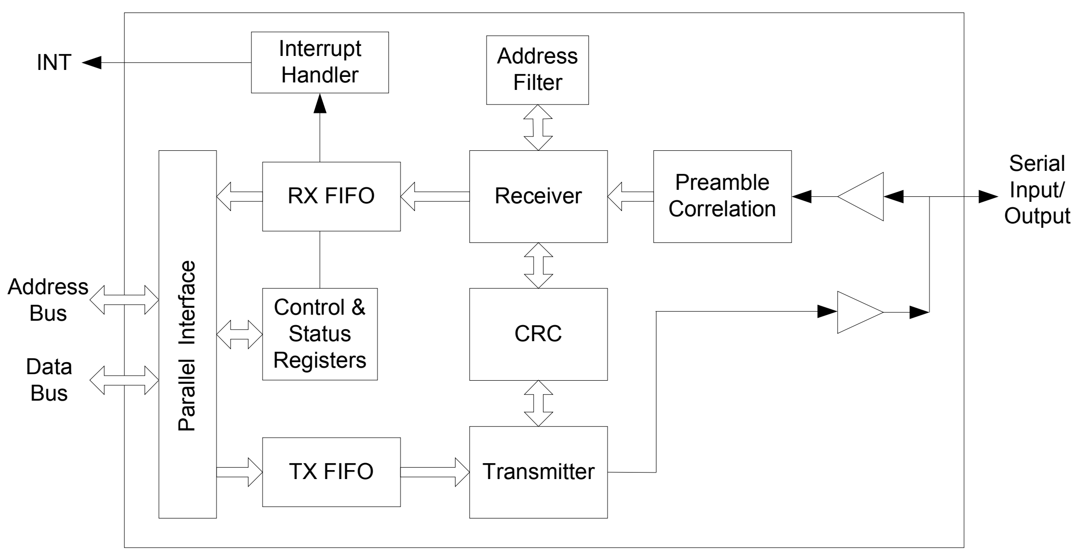


Fig. 8-2 BB Block Diagram

8.2 BB Description

8.2.1 Reset

A reset is achieved by holding the RST pin high for at least TBD oscillator cycles.

To ensure good power-up, a reset should be given to BB after power-up.

8.2.2 Power Saving Modes

The BB is designed to work in similar working modes as a typical MCU.

These modes enable the system to save power when the BB is not in use.

8.2.2.1 Power-Down Mode

The MCU can halt all activity in the BB by stopping its clock. This enables the MCU to reduce the power consumption of the BB to a minimum.

All registers and FIFOs retain their values when BB is in power-down mode.

BB enters power-down mode by setting the bit TBD to "1". This bit is set by MCU and cleared by BB.

BB goes back to working mode by setting CS_n input pin to "0" for TBD msec.

The wake-up time of the BB from power-down mode to fully operating mode is TBD msec.

Since BB retains all the register values in power-down mode, special care should be given to the register values before it enters power-down. For example, the MCU should check that the BB is not in the middle of transmitting or receiving a packet.

The RFACTIVE should be set low to shutdown the RFW-102, before entering power-down mode.

8.2.2.2 Idle Mode

In idle mode, the BB internally blocks the clock input. The external clock is not stopped, but it is not routed to the internal logic. By doing this, the MCU achieves substantial power savings and yet the wake-up time is still relatively short. The power consumption is not minimal since the external clock is still active.

All registers and FIFOs retain their values when BB is in idle mode.

BB enters idle mode by setting bit TBD to "1". This bit is set by MCU and cleared by BB.

BB goes back to working mode by setting CS_n input pin to "0" for TBD µsec.

Since BB retains all the register values in idle mode, special care should be given to the register values before BB enters idle mode. For example, the MCU should check that the BB is not in the middle of transmitting or receiving a packet. In addition, the RFACTIVE should be set low to shutdown the RFW-102.

8.2.3 Preamble Correlation

The transmitting BB sends the Preamble in order to synchronize the receiver to its transmission. BB transmits a fixed size Preamble of 16 bits. The received Preamble has a variable length of 16⇔9 bits, determined by SCR2 [5:7]. The receiver correlates the 16⇔9 bits from its PRE-L and PRE-H registers to the 16⇔9 bits in its input shift-register. If a correlation is found, then the BB receiver state machine is enabled.

The purpose of the Preamble is to filter the module packets from white noise or other transmissions on the channel. NODE_ID and NET_ID filter are used to filter packets from other module networks.

The Preamble is transmitted MSB to LSB (PRE-H first and then PRE-L).

The value of the Preamble is determined according to PRE-L and PRE-H registers.

The BB has the same Preamble when it is in transmitting mode (TX_RX=1) as when it is in receiving mode (TX_RX=0).

The value of the PRE-L and PRE-H registers should be identical in the BB in all nodes in the network.

8.2.4 Refresh Bit

When receiving a valid packet, the RFWaves modem (PHY layer) has to receive a “1” symbol each time a certain period has elapsed in order to maintain its sensitivity. T he time between adjacent “1” symbols is determined by the value of the reference capacitor. This constraint is transparent to the application layer since the BB adds a “1” symbol (refresh bit) if too many “0” symbols are transmitted consecutively. On the receiver side, these additional “1” symbols (refresh bits) are removed by the BB.

This feature is transparent to the application layer. The application layer has only to initialize the maximum allowed number of consecutive x“00” bytes.

The BB has the flexibility to add a refresh bit every 1 to 7 bytes. This is configured by RB(0:2) bits in PPR register. The value of RB (0:2) bits in PPR register determines the overhead the refresh bit has on the throughput of the link.

The refresh bit does not add substantial overhead on the bit stream, since it is only added when the number of consecutive x”00” bytes exceeds a certain value.

The data that is sent is application-dependent, so the application can be adjusted in order that there will be a negligible probability of this event happening.

Typical RFWaves capacitor: C=1nF

Normal discharge current = 200nA

Each 10mV on the capacitor represent 1dB in receiving power.

$$\frac{I}{C \cdot V} = \frac{200nA}{1nF \cdot 10mV} = \frac{1dB}{50\mu \sec}$$

The capacitor is charged with each received “1” symbol.

The receiver is allowed to lose 1dB before a new “1” is to be received.

Thus, after each 50 consecutive “0” bits in 1Mbps (50µsec) a “1” symbol should be sent.

In this case, setting RB [0:2] in PPR register to be 5 (“101”) would be sufficient (5 bytes = 40bits).

When RB (0:2) bits are set to “000” a refresh bit is added to every transmitted byte, regardless of its content. This introduces a constant overhead of 12.5%.

8.2.5 Bit Structure

The BB uses an oscillator ranging from 6⇔24 MHz. In order to determine the output and input bit rate, the BB must be configured to the number of clocks consisting each bit. This gives the applicator the control over the bit rate with certain restrictions. Each bit must have at least six clock cycles.

The maximum bit rate is: 1Mbps

The minimum bit rate is: 10Kbps (TBD)

However it is recommended to work only at 1Mbps since reducing the bit rate does not change the energy of a transmitted bit. This means that reducing the bit-rate does not improve the bit error rate or the range between the transmitter and the receiver.

Bit Length Register (BLR) determines the number of clock cycles per bit (bit period).

BLR value is given a fixed offset of 6, since the minimum number of clock cycles in one bit is 6.

Bit Rate = Oscillator / (BLR+6)

The BB outputs (for the RFW-102) the bit structure shown below.

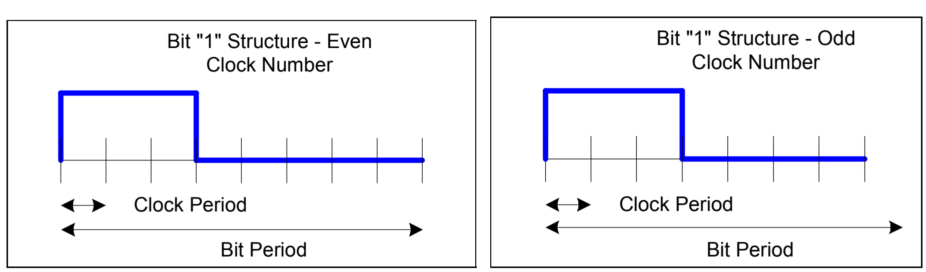


Fig. 8-3 Bit Structure of the BB output to the RFW-102

In the odd number of clocks example BLR=1.

In the even number of clocks example BLR=2.

The number of clocks when the line is "1" is determined as follows:

$$Number\ \ of\ \ "1"s = FLOOR\left[\left(\frac{BLR+6}{2}\right)-1\right]$$

In case of "0" bit, BB output "0" value for BLR+6 clock pulses.

* FLOOR – Rounds towards zero.

8.2.6 CRC

The BB adds additional CRC information to each packet in the transmitter module, in order to enable the protocol to detect errors. The CRC is a redundant code, which is calculated and added to each packet on the transmitter side. The CRC is also calculated on the receiver side. The CRC calculation results of the receiver and the CRC field in the received packet are compared in the receiver using the CRC module in the chip. If the CRC results are equal, then the receiver knows with reasonable probability that the packet was received correctly. If the CRC results are not equal then the receiver knows with probability 1 that the packet was received incorrectly.

The CRC mode is configured in the PPR (3:4) register.

Both the receiving node and the transmitting node in the network have to be in the same CRC mode.

The BB can apply CRC in three different ways:

16-Bit CRC – using polynomial $1+X^2+X^{15}+X^{16}$

8-Bit CRC – using polynomial $1+X+X^2+X^8$

No CRC.

This gives each application the flexibility to choose the adequate amount of overhead it adds to each packet and the corresponding level of protection the CRC code has.

If CRC is enabled, then the BB calculates the CRC of each incoming packet. It does not put the received CRC value in the RX_FIFO. It just puts the result of its calculation in the RX_FIFO as the last byte of the packet:

0x55 – CRC received correctly.

0xAA – CRC was received incorrectly.

The status bit SSR (0) stores the result of the last received packet.

8.2.7 RX FIFO

All received bytes are transferred to the RX_FIFO. The RX_FIFO stores the input data until the MCU reads the data from it.

CRC and Preamble bytes are not transferred to the RX_FIFO.

The RX_FIFO is accessed just like all other read-only registers in the BB. The MCU cannot write to RX_FIFO - it can only read from it.

RX_FIFO_SIZE is 16 bytes.

The purpose of having an input FIFO in BB is to reduce the real-time burden from the MCU. The FIFO is used as a buffer, which theoretically enables the MCU to read the incoming data every RX_FIFO_SIZE * 8 bit/byte * 1μsec = 128μsec, and not every 1μsec in the case of serial input, or every 8μsec in the case where there is a serial to parallel converter.

The actual buffer size for practical use is a bit smaller, since the MCU response time is taken into account.

The MCU has three ways to learn about the RX_FIFO status:

The RX FIFO Status Register (RFSR) contains the number of bytes in the RX_FIFO.

BB INT pin. If configured appropriately, the INT pin will be “1” each time RX_FIFO is almost full. This invokes a MCU interrupt if the INT pin is connected to the MCU external interrupt pin.

RX_FIFO Overflow Status Bit – bit RX_OF in SSR indicates when an overflow event has occurred. If a received byte is written to a full RX_FIFO, the last byte in the RX_FIFO is override and the RX_OF flag is raised.

The **RX_AF** interrupt should invoke the MCU to read from the RX_FIFO. Using the almost full event gives the MCU 32μsec (4 bytes * 8μsec) to respond before it loses data, assuming a bit rate of 1Mbps. It uses most of the RX_FIFO size even if the response latency of the MCU is very short.

Should the MCU not respond properly to the almost full event, and an input byte is written to the RX_FIFO when it was full, then this byte would overrun the last byte in the RX_FIFO, meaning the byte that immediately preceded it.

LOCK_OUT interrupt should also trigger the MCU to read from the RX_FIFO. In case a packet has ended and the RX_AF interrupt was not invoked, the MCU should be triggered by the LOCK_OUT interrupt.

8.2.8 TX FIFO

Transmitting data is done by writing it to the TX_FIFO.

The interface to the TX_FIFO is similar to all the other write-only registers in BB.

The purpose of the TX_FIFO is to reduce the real-time transmission process from the MCU. The TX_FIFO enables the MCU, theoretically, to write to the TX_FIFO every 128μsec and not every 8μsec, as is the case with a regular 8-bit shift register.

The TX_FIFO Status Register (TFSR) indicates the number of bytes in the TX_FIFO.

The TX_FIFO can also invoke an MCU interrupt if TX_FIFO almost empty event occurs.

Almost empty flag will rise when there are only four empty bytes in the TX_FIFO.

It gives the MCU 32μsec response time to reload the TX_FIFO in case the transmitted packet is bigger than the TX_FIFO.

In case the MCU writes to a full TX_FIFO, then this byte overruns the last byte in the TX_FIFO, meaning the byte that was written just before it. Writing to a full TX_FIFO sets the TX_OF flag in SSR.

8.2.9 Interrupt Driver

The INT output pin is the summation of all interrupts source in the BB. Whenever an interrupt event has occurred and this interrupt is enabled (IER), the INT will go from low to high. The INT will remain high until the IIR register is read. The IIR register contains all the interrupt events that have occurred since the last read. It shows the event only for enabled interrupts. If an interrupt is disabled, even if the event that invoked this interrupt has occurred, the interrupt flag will be low. The IER register is used to enable/disable each of the interrupt. SCR4 (0) enables/disables all the interrupts.

There are eight events in the BB that can cause the INT pin to go from low to high:

1. LOCK_IN – This interrupt indicates that the BB has started receiving a new packet. The Preamble has been identified. If the NET_ID and/or the NODE_ID are enabled, then they have been identified correctly. This event signals the beginning of an incoming packet.
2. LOCK OUT – BB has just finished receiving a packet. This means that if the BB is in fixed packet size mode, then it has finished receiving PSR bytes not including CRC bytes. If BB is not in fixed packet size mode, then it has just finished receiving a packet of size as indicated in the packet header. Although RX_STOP and setting TX_RX=1 (SCR2) terminate the receiving of the packet, they do not cause a LOCK_OUT event, since the MCU is already aware of it (the MCU initiated it). The LOCK_OUT interrupt tells the MCU when to get data out of the RX_FIFO.
3. LINK_DIS – This interrupt indicates that a "Zero counter" capacitor discharge event has occurred. If a consecutive number of zero bits (according to SCR3 (4:6)) have been received, this interrupt is set, even if zero count capacitor discharge is disabled (SCR3 (3) – EN_ZERO_DIS = '0'). The actual capacitor discharge and its interrupt are two separate registers (IER (2) for the interrupt and SCR3 (3) for the discharge).
4. RX_OF – This interrupt indicates that a byte from an incoming packet was discarded, since the RX_FIFO was already full. The receiver module tried to write a byte to a full RX_FIFO. The MCU should know that the corresponding packet is corrupted, since it is lacking at least one byte.

5. TX_EMPTY – The BB has finished transmitting a packet. Meaning, the transmit shift register is empty and BB is now in RX mode (not TX mode).
6. RX_FIFO_AF – RX_FIFO is almost full. If the MCU does not want the RX_FIFO to overflow, then it should empty it.
7. TX_FIFO_AE – TX_FIFO is almost empty. If the MCU did not finish putting the transmitted packet in the TX_FIFO, then it should continue doing so now.
8. CS – CS status line has gone from "1" to "0" invokes the CS interrupt. This signals the MCU that an unidentified (NET_ID or NODE_ID or Preamble were not identified) packet has ended. If the MCU has a packet to transmit, and CS="1" then the MCU waits for this event.

All these events can be masked. If an event is masked, then even if that event occurs, it does not set the INT pin to "1". The masking is done by register IER.

The reason for masking is that in different applications or in different situation in the same application these events have different priorities. The MCU determines which of these events will invoke an MCU interrupt.

Moreover all these events can be masked together by IE in IER register.

If INT pin is set to "1", the MCU learns which event has occurred by reading IIR register.

INT goes "0" when the MCU reads from IIR register.

8.2.10 Packet Size

There are two types of packet structure determined by PPR [5] (FIXED).

Fixed Sized Packet – all packets have the same, fixed size. The packet size is determined in the PSR register. The packet size can be 2 ⇔ 255 bytes.

Variable Sized Packet - the header of the incoming packet determines the packet size. One of the header bytes contains the packet size. Bits SIZE_LOC[0:1] in LCR register determines the location (offset) of the packet size inside each incoming packet header. The BB reads the packet size byte in the packet header according to LCR register. In both cases the packet size does not include the CRC addition or the Preamble.

8.2.11 NET_ID and NODE_ID Filters

NET_ID and NODE_ID are two filters in the receiver. They filter incoming packets according to their network address and node address.

The address field in each incoming packet is compared to NET_ID byte and NODE_ID byte. If one of the above comparisons fails, then the packet is discarded and the MCU will not be aware of it.

NET_ID and NODE_ID are both one byte. Their values are stored in NIR and BIR registers accordingly. The byte to which they are compared is set by LCR register.

Each of them can be enabled or disabled independently (PPR register).

NET_ID is targeted to be a filter on the network address. It is supposed to be common for all nodes in the network.

NODE_ID is targeted to be a filter on the specific node address. It is supposed to be unique to each node in the network.

The purpose of these filters is to save MCU power and to reduce its load. In a multi-node network, a node can filter all packets that are not sent to it, while in multi-network environment, a node can filter packets from other RFWaves networks.

In certain network a multicast ability inside the network is required. Even if NODE_ID filter is applied, Addresses '111111XX' in NODE_ID filter are preserved for multicast transmissions. NODE_ID filter will not discard those four addresses in any case.

8.2.12 Carrier-Sense

Carrier-sense protocols are protocols in which a node (station) listens to the common channel before it starts transmitting. The node tries to identify other transmissions in order to avoid collision that might block its own transmission. In a wider perspective, a network that applies carrier-sense protocol utilizes the channel bandwidth more efficiently. A more efficient network enables lower power consumption to each node, shorter delay and higher probability of reaching the destination of each packet.

The BB uses one complimentary technique in order to achieve very wide-ranging carrier-sense abilities. It has an internal implementation of RFWaves Network Carrier-Sense algorithm. This enables it to avoid collision with other RFWaves stations on its network or from other networks in the area.

While the Carrier-Sense status bit in SSR (CS) tells the MCU when not to transmit, the two interrupt CS and LINK_DIS gives the MCU a flag when to transmit. LINK_DIS will be invoked whenever any transmission has ended, while CS interrupt will be invoked only when an RFWaves transmission has ended. Some applications can use some of the above mechanisms though not all of them – according to its needs.

8.2.12.1 RFWaves Carrier-Sense Algorithm

Assuming our bit rate is 1Mbps. According to the described bit structure (Section 8.2.5 Bit Structure), the time difference between two rising on DATA_IO must be an integer number of 1µsec. If we take into account the frequency deviation between the two BB oscillators, the time difference between two rising edges is 1µsec±□. The □ depends on the frequency deviation between the two BB oscillators. The BB uses this quality in its carrier-sense algorithm. If an N (N = (CSR (0:3)*2)+2) number of "1" bits, where each is preceded by at least one "0" bit, are received with time difference of an integer number of 1µsec between two consecutive "1" bits, then the CS flag in SSR equals '1'. Basically, the BB counts "0" to "1" transits on DATA_IO input, where the time difference between two transits should be an integer number (≥2) to 1µsec. The number of consecutive "1" bits that conforms to this rule is counted in the following example (Figure 8-2) in ONE_CNT counter. ONE_CNT is incremented only if a "1" bit that comes after a "0" bit is received, where the time gap between the "1" bit and the

preceding "1" bit is as mentioned above. If the time difference between two consecutive "1" bits is out of the allowed deviation, the ONE_CNT is reset. ONE_CNT is also reset if the number of consecutive "0" exceeds (CSR (4:7)*2)+2, where CSR is the last "1" bit received is counted in ZERO_CNT. ZERO_CNT is reset each time "1" bit is received.
Both M and N values are determined in CSR register (CSR (7:4) and CSR (3:0) accordingly).

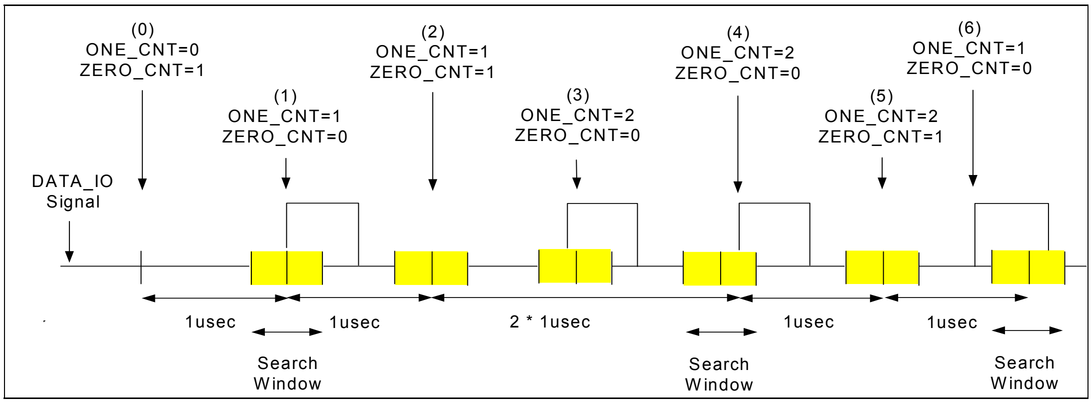


Fig. 8-4 Carrier-Sense Example

In the example shown in Figure 8-2, at time (1) a new "1" bit is received after a "0" bit was received. Thus, ONE_CNT equals 1 and ZERO_CNT is reset to 0. At time (2), a zero bit is received, so the ZERO_CNT is incremented. At time (3), a "1" is received after a "0" bit that was received before it. Thus ONE_CNT is incremented and ZERO_CNT is reset. At time (4) a "1" bit is received after a "1" bit, thus, there is no change in any counter. At time (6) a "1" bit is received out of the allowed window, so ONE_CNT is reset to 1.

The CSR register is used to configure the carrier-sense algorithm sensitivity. The CSR register determines the number of "1" bits that are required in order to decide that a carrier exists. The CSR also determines the number of successive "0" bits that reset the carrier-sense state machine.

In SSR register, bit CS notifies whether a carrier was identified. Carrier-sense can also be used as an interrupt. When CS in SSR goes from '1' to '0' i.e. the transmission has stopped, a CS interrupt is invoked (if enabled in IER). The purpose of this interrupt is to inform the MCU that the channel is free again.

If the BB identifies a packet, the carrier-sense algorithm halts. When the BB is in RX mode and the LOCK flag in SSR is "0", the CS mechanism is working. When the LOCK flag in SSR is "1", the CS mechanism is not working, since the CS flag does not add any information because a Preamble was identified already. After a Preamble was identified the CS in SSR equals '1'.

8.2.13 Receiver Reference Capacitor Discharge

The BB implements two independent mechanisms for receiver capacitor discharge:

At the end of each received packet.

Zero counter.

Mechanism 1 is enabled/disabled by bit EN_CAP_DISCH in SCR3.

Mechanism 2 is enabled/disabled by bit EN_ZERO_DISCH in SCR3.

The number of “0” bits that will cause a discharge in Mechanism 2 are determined by bits ZERO_DISCH_CNT [0:2].

For both mechanisms, the discharge time is determined by CAP_DIS_PERIOD in SCR3.

Discharge is done by setting RX_TX pin to ‘1’ for a certain time and then setting it back to ‘0’.

(*) More detailed explanations of the reference capacitor discharge algorithms and motivations can be found in the “RFW - Capacitor Discharge.pdf” document.

8.2.14 Changing the BB Configuration

It is not recommended to change the BB configuration while it is in the middle of receiving or transmitting a packet.

Thus, before writing to any of the BB control registers (such as BLR, PRE-L, PRE-H, PPR etc):

Change the TX_RX mode to RX.

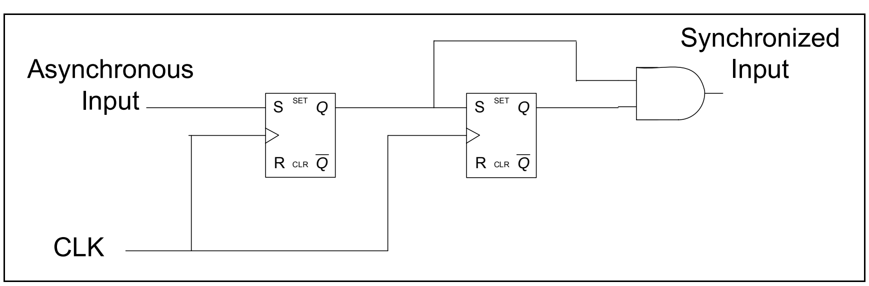
Disable the Preamble search (SEARCH_EN in SCR2)

Stop all RX receiving – RX_STOP.

It is then safe to change the BB configuration.

8.2.15 Input Synchronizer

Handling asynchronous inputs to the BB.



8.3 Register Description

The registers in the BB are divided into three groups:

Read-only registers which are mainly status registers.

Write-only registers which are mainly control registers.

Read and write registers.

In case of an RST pulse, all registers are set to their default value.

8.3.1 Bit Length Register (BLR)

This register is both a read and a write register.

It determines the length of the bit in terms of clock cycles.

The bit length will be (BLR+6) clocks, since the minimum length of a bit is 6 clocks.

Default Value: 00 (0+6=6).

8.3.2 Preamble Low Register (PRE-L)

This register is a write-only register.

This register contains the 8 least significant bits of the Preamble.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRE-L	PR-7	PR-6	PR-5	PR-4	PR-3	PR-2	PR-1	PR-0

Default Value: 0xEB.

8.3.3 Preamble High Register (PRE-H)

This register is a write-only register.

This register contains the 8 most significant bits of the Preamble.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRE-H	PR-15	PR-14	PR-13	PR-12	PR-11	PR-10	PR-9	PR-8

Default Value: 0xFF.

8.3.4 Packet Parameter Register (PPR)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPR	NET ID_EN	NODE ID_EN	FIXED	CRC1	CRC0	RB-2	RB-1	RB-0

This is a read and a write register. It contains the control bits of the transmitted and received packet structure.

Default Value: 0x3A.

Bits 0-2 (RB-0~RB-2): Refresh Bits

These bits determine the maximum number of successive "zero" bytes allowed before an added "one" bit is stuffed to the packet by the transmitter state machine. The reason for this feature is to keep the RFW-102 reference capacitor charged.

Refresh Bit	Bit 2	Bit 1	Bit 0
Refresh bit is added to every byte.	0	0	0
Refresh bit is added if 1 byte equals x"00".	0	0	1
Refresh bit is added if 2 successive bytes equal x"00".	0	1	0
Refresh bit is added if 3 successive bytes equal x"00".	0	1	1
Refresh bit is added if 4 successive bytes equal x"00".	1	0	0
Refresh bit is added if 5 successive bytes equal x"00".	1	0	1
Refresh bit is added if 6 successive bytes equal x"00".	1	1	0
Refresh bit is added if 7 successive bytes equal x"00".	1	1	1

The value of the refresh bit is determined by the value of the reference capacitor.

Bits 3, 4: CRC [0:1]

These bits control the CRC operation for both transmit and receive mode:

CRC	Bit 4	Bit 3
No CRC	0	0
CRC8	0	1
CRC8	1	0
CRC16	1	1

Bit 5: Fixed

This controls the packet mode. When high system packets are fixed size and the length is specified in the Packet Size Register (PSR).

When Fixed is low, the packet size is variable. The size is specified in the header of the incoming or outgoing packets. The location of the packet size field is specified in the LCR register.

Bit 6: NODE_ID_EN

This is NODE_ID control bit.

0: Disables Node ID search

1: Enables Node ID search according to LCR, BIR

Bit 7: NET_ID_EN

This is NET_ID control bit.

0: Disables Net ID search

1: Enables Net ID search according to LCR, NIR

8.3.5 System Control Register 1 (SCR1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

This byte is reserved.

Default Value: 0x00.

8.3.6 System Control Register 2 (SCR2)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCR2	PRE MASK 2	PRE MASK 1	PRE MASK 0	STOP RX	TX FIFO RESET	RX FIFO RESET	SEAR CH EN	TX_R X

This register is a read and a write register.

This register controls the system operation modes.

Bit 0: TX_RX

Controls the transceiver mode: receive mode or transmit mode

When TX_RX is low – BB is in receive mode (default mode). The output pin RX_TX is set to ‘0’. BB searches for a Preamble. If Preamble is found, it handles the process of receiving a packet.

If SCR3 (7) is set, then the BB goes to RX mode and the output pin RX_TX is in TX mode.

The capacitor discharge can change the output pin RX_TX to TX mode even if we are in RX mode in the BB. In this case the output pin RX_TX will be in TX for a short duration and then return to RX mode.

When TX_RX is high – BB is in transmit mode. The output pin RX_TX is set to ‘1’. The BB handles the process of transmitting a packet according to the data in the TX_FIFO. When it finishes transmitting the packet, it automatically goes back to receive mode.

Bit 1: SEARCH_EN

Preamble search enable bit.

When 1: Enables the search for Preamble in receive mode.

When 0: Disables the search for Preamble in receive mode, (used when user configures the system while in default receive mode).

This bit’s default value is ‘0’. It must be set to ‘1’ in order to start receiving a packet.

Bit 2: RX_FIFO_RESET

This bit resets the RX_FIFO address pointers when set to Logic 1. This bit is set by the MCU and is cleared automatically by the BB.

Bit 3: TX_FIFO_RESET

This bit resets the TX_FIFO address pointers when set to Logic 1. This bit is set by the MCU and is cleared automatically by the BB.

Bit 4: STOP_RX

This bit stops receiving the current command, resets the RX_FIFO counters and start new searches for a preamble. This bit is set by the MCU and is cleared automatically by the BB.

Bits 5-7: PRE_MASK [0:2]

These bits determine the mask on PRE-H in preamble correlation. Meaning, it determines the size of the Preamble in the receiver.

The PRE-L is always used in the Preamble correlation.

BB cuts off bit from PRE-H register, starting from the MSB.

PRE MASK 0	PRE MASK 1	PRE MASK 2	Preamble Size
0	0	0	16
0	0	1	15
0	1	0	14
0	1	1	13
1	0	0	12
1	0	1	11
1	1	0	10
1	1	1	9

Default Value: 0x60

8.3.7 System Control Register 3 (SCR3)

This register is a read and a write register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCR3	LOW MODE	ZERO DISCH CNT 2	ZERO DISCH CNT 1	ZERO DISCH CNT 0	EN ZERO DISCH	CAP DIS PERIOD	EN CAP DISCH.	-

Bit 1: EN_CAP_DISCH

Enables/disables capacitor discharge mechanism after each received packet:

0: Disables discharge

1: Enables discharge

This bit overrides Bit 3

Bit 2: CAP_DIS_PERIOD

Determines the capacitor discharge duration:

0: The pulse width is 36 clocks, (3 µsec at 12 MHz clock).

1: The pulse width is 72 clocks, (3 µsec at 24 MHz clock).

Bit 3: EN_ZERO_DISCH

Enables/disables zero counter mechanism for capacitor discharge:

0: Disables discharge

1: Enables discharge

Bits 4-6: ZERO_DISCH_CNT [0:2]

Determine the number of zero bits that will trigger a capacitor discharge by the zero counter mechanism.

ZERO DISCH CNT 0	ZERO DISCH CNT 1	ZERO DISCH CNT 2	Number of Zeros
0	0	0	5
0	0	1	10
0	1	0	15
0	1	1	20
1	0	0	25
1	0	1	30
1	1	0	35
1	1	1	40

Bit 7: LOW_MODE

Enables or disables low power mode for RFW-102:

0: Disables low mode (normal mode)

1: Enables low mode. BB is in RX mode, while RFW-102 is in TX mode.

The user has to put the BB into RX mode and to disable RX and PREAMBLE search, before enabling LOW_MODE. This transfers the RFW-102 to TX mode using RX_TX pin, while the BB is still in RX mode.

RFW-102 power consumption is lower in TX mode than in RX mode. BB can not remain in TX mode, if it is not transmitting. The low mode is the combination of both of the above.

Default Value: 0x01

8.3.8 System Control Register 4 (SCR4)

This register is a read and a write register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCR4	N/A	N/A	N/A	N/A	FIFO FLAGS	WIN CONT	RF_ACTIVE	IE

Bit 0: IE

This flag enables all interrupts when set to '1'.

When '0', all interrupts are disabled.

Bit 1: RF_ACTIVE

This bit controls the RF_ACTIVE pin. When this bit is high, the RF Modem is active.

Bit 2: WIN CONT

This bit determines the size of the WINDOW in the Preamble search module.

IF (BLR+6)>14 and WIN_CONT=1, then the preamble window size is 5.

Bit 3: FIFO FLAGS

Determines the RX_FIFO AF flag and TX_FIFO AE flag:

IF FIFO FLAGS = 0 then AF = 12 and AE = 4.

IF FIFO FLAGS = 1 then AF = 8 and AE = 8.

Default Value: 0x00.

8.3.9 Transmit FIFO Status Register (TFSR)

This register is a read-only register. It contains the number of bytes in the TX_FIFO.

Default Value: 0x00 (TX_FIFO empty).

8.3.10 Receive FIFO Status Register (RFSR)

This register is a read-only register. It contains the number of bytes in the RX_FIFO.

Default Value: 0x00 (TR_FIFO empty).

8.3.11 Location Control Register (LCR)

This is a read and a write register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCR	-	SIZE LOC 2	SIZE LOC 1	SIZE LOC 0	NET LOC1	NET LOC 0	NODE LOC 1	NODE LOC 0

Bits 0, 1: NODE_LOC [0:1]

These bits determine the location of the NODE_ID parameter in the header (the location is specified in bytes excluding preamble). The location should be fixed for all of the different kinds of packets transferred by the system. NODE_ID must never be set to be smaller than NET_ID, if both filters are enabled.

Location	NODE LOC 1	NODE LOC 0
2	0	0
3	0	1
4	1	0
5	1	1

Bits 2, 3: NET_LOC [0:1]

These bits determine the location of the NET_ID parameter in the header (the location is specified in bytes excluding preamble). The location should be fixed for all of the different kinds of packets transferred by the system.

Location	NET LOC 1	NET LOC 0
1	0	0
2	0	1
3	1	0
4	1	1

Bits 4-5: SIZE_LOC [0:2]

These bits determine the location of the Packet Size parameter in the header (the location is specified in bytes excluding preamble). The location should be fixed for all of the different kinds of packets transferred by the system.

Location	Size LOC 2	Size LOC 1	Size LOC 0
2	0	0	0
3	0	0	1
4	0	1	0
5	0	1	1
6	1	0	0
7	1	0	1
8	1	1	0
9	1	1	1

Default Value: 0x00

8.3.12 Node Identity Register (BIR)

This is a read and a write register.

When the Receiver State Machine builds the incoming packet, it compares the value in the BIR register to the received data at the location specified in LCR.

If the received NODE_ID and the expected NODE_ID are not equal, the packet is discarded.

Four multicast NODE_ID addresses are implemented "111111XX". All packets whose 6 MSBs are "1" are not discarded.

Default Value: 0x00

8.3.13 Net Identity Register (NIR)

This is a read and a write register.

When the Receiver State Machine builds the incoming packet, it compares the value in the NIR to the received data at the location specified in LCR.

If received NET_ID and the expected NET_ID are not equal, the packet is discarded.

Default Value: 0x00

8.3.14 System Status Register (SSR)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	-	TX_UF	BIT_ERROR	LOCK	CS	TX EMPTY	LOCKED	CRCERROR

This register is a read-only register. It provides status information to the MCU concerning the communication line and the data transfer. Bits 1, 2, 3 can trigger the interrupt if enabled in the IER. Bits 0, 5 and 6 are set by H/W and cleared automatically after the MCU reads the register. **Bits 1~4** are set and cleared by H/W

Bit 0: CRC_ERROR

This flag indicates a CRC Error in the packet. The CRC Block sets this flag at the end of each received packet according to the CRC calculation result. BB compares the calculated CRC and the received CRC. When these values differ, the flag goes high.

The flag is cleared only after the MCU reads the SSR register. If the MCU does not read the SSR register, this flag remains "1".

Bit 1: LOCKED

This flag indicates that a packet is being received.

Bit 1 is set to logic 1 whenever the system identifies a new incoming packet (triggers LOCK IN interrupt). The bit will reset to Logic 0 when the packet ends (triggers LOCK OUT interrupt) or when one of the IDs fails (NET or BYTE). This indicator is important whenever we want to switch to transmit mode because it can tell us that the line is busy and that in most cases the transmission will not succeed. The Lock triggers interrupt for every change in the bit status.

Bit 2: TX_EMPTY

This bit is the Transmitter Empty flag. When this bit is high, the system is available for loading the next packet for transmission and BB is in receive mode. When the flag is low, BB is in the middle of a packet transmission.

When transmitting few successive packets, the MCU should wait to the end of a packet before it reloads the TX_FIFO with the next packet.

Bit 3: CS

Carrier Sense detection bit

When this bit is high, the system has identified a structure of packet transmission in the air according to CSR.

When low, no carrier has been detected. This bit is only valid in receive mode. The conditions for setting or clearing this flag are determined in the CS register.

When LOCKED is high, then CS is meaningless.

Bit 4: LOCK

This signals whether a Preamble was identified or is still searching.

When the flag is “0”, the receiver is searching for Preamble.

When the flag is “1” a Preamble was identified. If a packet was discarded for any reason, the LOCK flag goes to 1.

Bit 5: BIT_ERROR

This flag indicates that there was some error in the received package. The packet was not received according to the expected timing specifications.

The packet can still pass CRC verification.

Bit 6: TX_UF

This flag is set **whenever** the MCU reads a byte from an empty TX_FIFO.

This flag indicates abnormal end of packet transmission. The MCU transmitter's state machine has expected to find a valid byte in the TX_FIFO according to the packet size, but it found an empty TX_FIFO. When this event occurs, the TX_EMPTY interrupt is invoked and TX_UF (underflow) flag is set to '1'.

This flag is set by hardware and cleared by the MCU. It is cleared whenever the MCU reads the SSR register.

Default Value: 0x04.

8.3.15 Packet Size Register (PSR)

This is a read and a write register.

It contains the Packet Size in byte units. When working in fixed size packets (see Control Bit-1), the size will be fixed for all types of packets.

The size in PSR excludes 2 bytes of Preamble and 2, 1 or 0 bytes of CRC.

Default Value: 0x00.

8.3.16 Carrier Sense Register (CSR)

This is both a read and a write register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSR	ZERO CNT.3	ZERO CNT.2	ZERO CNT.1	ZERO CNT.0	ONE CNT.3	ONE CNT.2	ONE CNT.1	ONE CNT.0

Bits 0-3: ONE_CNT [0:3]

The number of successive "1" bits that set the carrier sense high.

Bits 4-7: ZERO_CNT [0:3]

The number of successive "0" bits that reset the carrier sense (CS='0').

Default Value: 0x44

8.4 Interrupt Registers

8.4.1 Interrupt Enable Register (IER)

This register is a write and a read register.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	CS	TX_AE	RX AF	TX EMPTY	RX_OF	LINK_DIS	LOCK OUT	LOCK IN

Default Value: 0x00.

For all flags in this register, **0**: Disable

1: Enable

Bit 0: LOCK_IN

This flag enables/disables the LOCK IN interrupt.

PREABLE + NODE_ID + NET_ID identified correctly triggers LOCK IN interrupt.

Bit 1: LOCK_OUT

This flag enables/disables the LOCK OUT interrupt.

End of received packet triggers LOCK_OUT interrupt.

Bit 2: LINK_DIS

This flag enables/disables the LINK_DIS interrupt.

The zero counter capacitor discharge triggers the LINK_DIS interrupt.

Bit 3: RX_OF

This flag enables/disables the RX_OF interrupt.

End of received packet triggers RX_OF interrupt.

Bit 4: TX_EMPTY

This flag enables/disables the TX_EMPTY (Transmitter Empty) interrupt.

TX_EMPTY interrupt tell the MCU that the transmitter has just finished transmitting a packet. BB goes to RX mode after finishing the transmission of a packet.

Bit 5: RX_AF

This flag enables/disables the RX_AF interrupt.

The RX_AF interrupt is triggered when RX_FIFO AF flag goes from ‘0’ to ‘1’.

Bit 6: TX_AE

This flag enables/disables the TX_AE interrupt.

The TX_AE interrupt is triggered when TX_FIFO AE flag goes from ‘0’ to ‘1’.

Bit 7: CS

This flag enables/disables the CS interrupt.

CS flag in SSR negative edge triggers CS interrupt.

8.4.2 Interrupt Identification Register (IIR)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIR	CS	TXAE	RX AF	TXEMPTY	RX_OF	LINK_DIS	LOCKOUT	LOCKIN

This is a read only register.

When the MCU accesses the IIR, all interrupts freeze. While the MCU access is occurring, the system records the changes in the interrupts but waits until the MCU access is complete before updating the register. A flag is active only when the matching interrupt enable bit is set, and does not depend on the IE bit value. The flags are set by H/W and cleared after the MCU reads the register.

Bit 0: This bit reflects the LOCK IN flag interrupt when enabled by IER.

This bit reflects the LOCK IN flag interrupt when enabled by IER.

LOCK_IN interrupt is invoke whenever a PREAMBLE+NET_ID+NODE_ID where recognized.

If NET_ID is disabled, then a received PREAMBLE+ NODE_ID invokes the interrupt.

If NODE_ID is disabled, then a received PREAMBLE+ NET_ID invokes the interrupt.

If NET_ID and NODE_ID are disabled, then a received PREAMBLE invokes the interrupt.

Bit 1: This bit reflects the LOCK OUT flag interrupt when enabled by IER.

This bit reflects the LOCK OUT flag interrupt when enabled by IER.

LOCK_OUT interrupt is invoked whenever RFW-D100 has finished receiving a packet. The end of the packet is determined according to the packet size.

Bit 2: This bit reflects the LINK_DIS flag interrupt when enabled by IER.

This interrupt is invoked by the zero counter capacitor discharge mechanism.

Bit 3: This bit reflects the RX_OF flag interrupt when enabled by IER.

Bit 4: This bit reflects the TX EMPTY flag interrupt when enabled by IER.

Bit 5: This bit reflects the RX FIFO AF flag interrupt when enabled by IER.

Bit 6: This bit reflects the TX FIFO AE flag interrupt when enabled by IER.

Bit 7: CS – when CS flag goes from “1” to “0” an interrupt is invoked.

8.5 List of BB Register Mapping

Register Address	Write	Read	Default Values	
0 (00000)	TX_FIFO	RX_FIFO	---	---
1 (00001)	PRE_L		0xFF	
2 (00010)	PRE_H		0xFF	
3 (00011)	FRC_L		0xFF	
4 (00100)	FRC_H		0xFF	
5 (00101)	SCR1		0x00	
6 (00110)	SCR2		0x60	
7 (00111)	SCR3		0x01	
8 (01000)	SCR4		0x00	
9 (01001)	LCR		0x00	
10 (01010)	BIR		0x00	
11 (01011)	NIR		0x00	
12 (01100)	PSR		0x00	
13 (01101)	PPR		0x3A	
14 (01110)	BLR		0x00	
15 (01111)	CSR		0x44	
16 (10000)	IER		0x00	
17 (10001)	---	IIR	---	
18 (10010)	---	SSR	---	0x04
19 (10011)	---	TFR	---	0x00
20 (10100)	---	RFR	---	0x00

8.6 MCU BB Control Registers

8.6.1 Control Registers List

RFAAR (0x2D): Register R2D indicates BB indirect RAM address.

RFDB (0x2E): Register R2E indicates BB indirect RAM data.

RFACR (0x2F): Register R2F indicates BB RAM access control.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	RRST	RFRD	RFWR

RFINTF (0x30): BB interrupt flags

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSDF	TX_AEF	RX_AFF	TX_ EMPTYF	RX_OFF	LINK_ DISF	LOCK_OUTF	LOCK_ INF

RFINTE (0x99): BB interrupt enable

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSDE	TX_AEE	RX_AFE	TX_ EMPTYE	RX_OFE	LINK_ DISE	LOCK_OUTE	LOCK_ INE

PRIE (0x80): Peripherals enable control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	USBE	BBE	-	-	PWM0E	TCCE	FRCE

8.6.2 BB Control Example

```
ORG     0X0060                          // TX_EMPTY INT address
     BC      RFINTF, TX_EMPTYF          // RF data send out, clear
                                           INT flag.
     RETI

ORG     0X0100
START:
     BS      RFACR, RRST                // BB reset.
     NOP
     BC      RFACR, RRST
     BS      PRIE, BBE                  // BB power enable.
     MOV     A, #0x10
     MOV     RFINTE, A                  // BB INT.TX_EMPTY enable.
     ENI                                // enable all INT.

RF_TX_INITIAL:
     WRITE   #SCR2, #8                  // Reset TX_FIFO, RX mode.
     WRITE   #BLR, #10                  // Set bit rate.
     WRITE   #PPR, #33                  // Set package size to be
                                           fixed.
                                        // Refresh bit mode 1. CRC
                                           disabled
     WRITE   #PSR, #6                   // Set package size to 6.
     WRITE   #PRE_H, #0xDC              // Set preamble High byte
                                           value.
     WRITE   #PRE_L, #0xA7              // Set preamble Low byte
                                           value.

RF_SEND_DATA:
     WRITE   #TX_FIFO, #0x01            // Write first byte of
                                           package to TX_FIFO.
     WRITE   #TX_FIFO, #0x02
     WRITE   #TX_FIFO, #0x03
     WRITE   #TX_FIFO, #0x04
     WRITE   #TX_FIFO, #0x05
     WRITE   #TX_FIFO, #0x06            // Write last byte of package
                                           to TX_FIFO.
     READ    #TFR, 0x60                 // Read TFR register data
     WRITE   #IER, #16                  // enable TX_EMPTY INT
     WRITE   #SCR4, #0x03               // enable all INT.
     WRITE   #SCR2, #1                  // move from RX to TX mode.
```

```
LOOP:
     JMP       LOOP

WRITE_DATA_TO_RF:                  // BB register write SUB
     BC        RFACR, RFWR
     NOP
     NOP
     BS        RFACR, RFWR
     RET

READ_DATA_FROM_RF:                 // BB register read SUB
     NOP
     NOP
     NOP
     NOP
     BC        RFACR, RFRD
     NOP
     NOP
     NOP
     NOP
     NOP                           // Note the access time
     MOV       A, RFDB
     NOP
     NOP
     NOP
     BS        RFACR, RFRD
     RET

; ================================================
WRITE MACRO     #CON1, #CON2      // BB register write MACRO
     MOV       A, #CON2
     MOV       RFDB, A
     MOV       A, #CON1
     MOV       RFAAR, A
     CALL      WRITE_DATA_TO_RF
ENDM
; ================================================
READ  MACRO     #CON, REG         // BB register read MACRO
     MOV       A, #CON
     MOV       RFAAR, A
     CALL      READ_DATA_FROM_RF
     MOV       REG, A
ENDM
```

9 Universal Serial Bus (USB)

9.1 Block Diagram

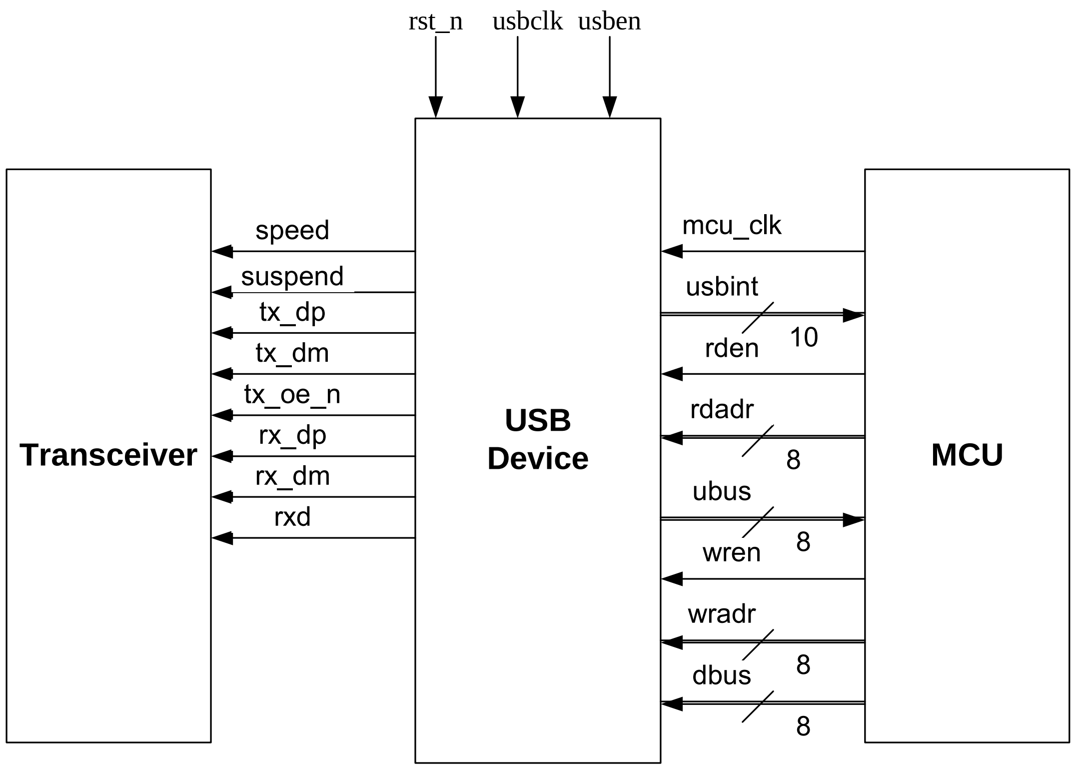


Fig. 9-1 USB Function Block Diagram of the EM77930

9.2 USB FIFO Allocation

End Point Number	End Point Type	FIFO Size
0	Control	64 byte IN 64 byte OUT
1	Interrupt / Bulk / Isochronous	64 byte IN / OUT
2	Interrupt / Bulk / Isochronous	64 byte IN / OUT
3	Interrupt / Bulk / Isochronous	64 byte IN / OUT

9.3 Pin Description

Pin	I/O	Description
usben	I	USB module enable
usbclk	I	48MHz clock for USB device
rst_n	I	Reset Active low hardware reset signal to the USB.
speed	O	Speed USB device speed 1: full speed device 0: low speed device
suspend	O	Transceiver suspend Enable /disable transceiver when port suspend 1: Disable transceiver 0: Enable transceiver
tx_dp	O	USB output data puls
tx_dm	O	USB output data minus
tx_oe_n	O	USB data output enable
rx_dp	I	USB input data plus
rx_dm	I	USB input data minus
rxd	I	USB Input data
mcuclk	I	Clock signal from mcu
usbint[9:0]	O	Interrrup output Active high signals generated by the USB to the MCU.
rden	I	Read enable The signal is asserted high for a read operation.
rdadr[7:0]	I	Read address bus Read address generated by MCU for the USB register. selection.
ubus[7:0]	O	Data output Data bus output to MCU
wren	I	Write enable The signal is asserted high for a write operation
wradr[7:0]	I	Write address bus Write address generated by MCU for the USB register. selection
dbus[7:0]	I	Data input Data bus input to MCU

9.4 Timing Diagram of MCU Interface

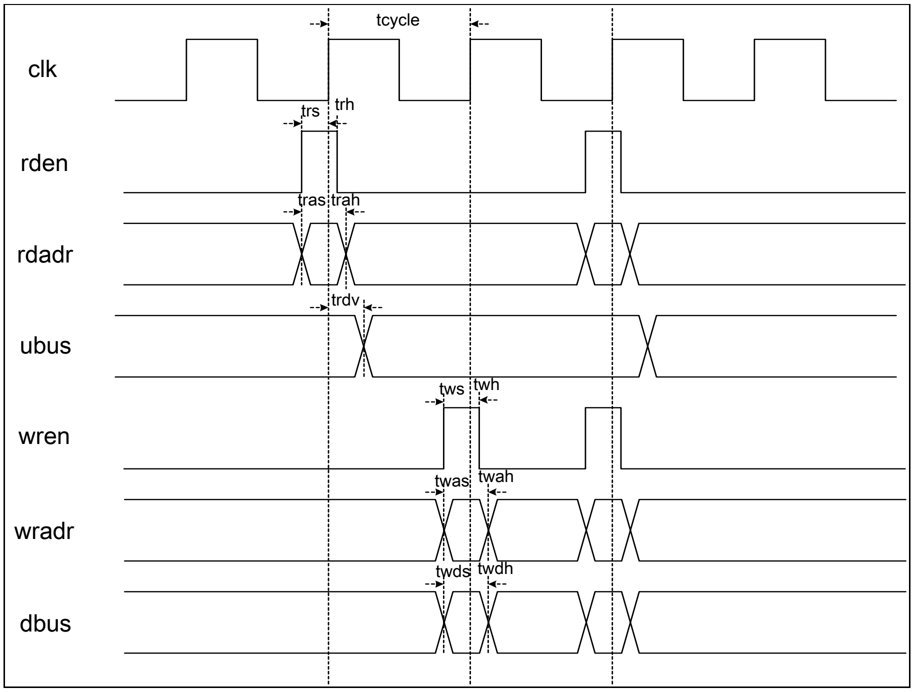


Fig. 9-2 MCU Interface Timing Diagram

Symbol	Parameter	Min	Max
tcycle	MCU clock cycle time	20ns	–
trs	Read enable setup time	3ns	–
trh	Read enable hold time	0.1ns	–
tras	Read address setup time	3ns	–
trah	Read address hold time	0.1ns	–
trdv	Read data valid time	–	5ns
tws	Write enable setup time	3ns	–
twh	Write enable hold time	0.1ns	–
twas	Write address setup time	3ns	–
twah	Write address hold time	0.1ns	–
twds	Write data setup time	3ns	–
twdh	Write data hold time	0.1ns	–

9.5 USB Device Register Summary

Register	ADDR	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCNTR	0x1CD	–	SPD	–	–	–	RESUME	SUSPEND	PLUG	URST
			P	–	–	–	P/H	P/H	P	P/H
EP1CNTR	0x1CE	P/H/S	–	–	EPEN	–	–	EPDIR	EPTYPE1	EPTYPE0
EP2CNTR	0x1CF	P/H/S	–	–	EPEN	–	–	EPDIR	EPTYPE1	EPTYPE0
EP3CNTR	0x1D0	P/H/S	–	–	EPEN	–	–	EPDIR	EPTYPE1	EPTYPE0
EPINTR	0x1D1	P	–	–	INT3	INT2	INT1	INT0IN	INT0TX	INT0RX
EPINTE	0x1D2	P	–	–	INT3E	INT2E	INT1E	INT0INE	INT0TXE	INT0RXE
STAINTR	0x1D3	P	–	–	–	–	–	RUEINT	IDLEINT	RSTINT
			–	–	–	–	–	P/H	P/H	P
STAINTE	0x1D4	P	–	–	–	–	–	RUEINTE	IDLEINTE	RSTINTE
FAR	0x1D5	P	–	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
EP0RXTR	0x1D6	P	–	–	–	–	–	SETUPOW	SETUP	OUT
EP0RXCSR	0x1D7	P/H/S	CDTOG	ERRSTS	STALLSTS	ACKSTS	DTOGERR	DTOG	SESTALL	RXEN
EP0TXCSR	0x1D8	P/H/S	CDTOG	ERRSTS	STALLSTS	ACKSTS	–	DTOG	SESTALL	TXEN
EP1CSR	0x1D9	P/H/S	CDTOG1	ERRSTS1	STALLSTS1	ACKSTS1	DTOGERR1	DTOG1	SESTALL1	RXTXEN1
EP2CSR	0x1DA	P/H/S	CDTOG2	ERRSTS2	STALLSTS2	ACKSTS2	DTOGERR2	DTOG2	SESTALL2	RXTXEN2
EP3CSR	0x1DB	P/H/S	CDTOG3	ERRSTS3	STALLSTS3	ACKSTS3	DTOGERR3	DTOG3	SESTALL3	RXTXEN3
EP0RXCTR	0x1DC	X	–	EP0RXCT6	EP0RXCT5	EP0RXCT4	EP0RXCT3	EP0RXCT2	EP0RXCT1	EP0RXCT0
EP0TXCTR	0x1DD	H/S	–	EP0TXCT6	EP0TXCT5	EP0TXCT4	EP0TXCT3	EP0TXCT2	EP0TXCT1	EP0TXCT0
EP1CTR	0x1DE	H/S	–	EP1CT6	EP1CT5	EP1CT4	EP1CT3	EPCT2	EPCT1	EPCT0
EP2CTR	0x1DF	H/S	–	EP2CT6	EP2CT5	EP2CT4	EP2CT3	EPCT2	EPCT1	EPCT0
EP3CTR	0x1E0	H/S	–	EP3CT6	EP3CT5	EP3CT4	EP3CT3	EPCT2	EPCT1	EPCT0
EP0RXDAR	0x1E1	X	DATA7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
EP0TXDAR	0x1E2	X	DATA7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
EP1DAR	0x1E3	X	DATA7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
EP2DAR	0x1E4	X	DATA7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
EP3DAR	0x1E5	X	DATA7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
HINTR	0x1E7	X	–	SOFINT	–	–	–	–	–	–
HINTE	0x1E8	X	–	SOFINTE	–	–	–	–	–	–
FNLR	0x1FE	X	FNLR7	FNLR6	FNLR5	FNLR4	FNLR3	FNLR2	FNLR1	FNLR0
FNHR	0x1FF	X	–	–	–	–	–	FNHR10	FNHR9	FNHR8

Legend: "P" = Power-on reset **"H"** = Hardware reset **"S"** = Software reset

9.5.1 General Control Register (GCNTR)

Bit	Field	HW	SW	DF	Description
0	RESET	R/W0C	R/W	0	**Software Reset** S/W sets this bit and will reset the whole USB compound device. All registers return to their default value and the USB compound device will be in the default state. H/W will clear this bit after the reset is completed.
1	PLUG	R	R/W	0	**Connect USB device** When set to 1 by S/W, 1 will be driven to the connecting pin, thus the pull-high resistance is connected to the USB bus, and the USB compound device is connected to the USB bus. When cleared to 0 by S/W, 0 will be driven to the connecting pin, thus the pull-high resistance is not connected to the USB bus, and the USB compound device is not connected to the USB bus. This bit will be reset by SW reset and USB reset.
2	SUSPEND	R/W0C	R/W	0	**Suspend State Enable** Set by SW to force the USB device to enter suspend state. SW is allowed to set this bit if the USB bus has been in the idle state for more than 3ms. The USB device will leave the suspend state if the SW clears this bit or the resume bit is set. This bit will be cleared by HW if the resume bit is set. This bit will be reset by SW reset and USB reset.
3	RESUME	R/W0C	R/W	0	**Send Resume to USB Bus** When set to 1, the USB device will send resume signal to the USB bus after the USB bus has been in the idle state for more than 5ms. The resume signal will be driven for 5ms. HW will clear this bit after completing resume sending.
6-4	Reserved				
7	SPD	R	R/W	1	**USB function speed setting** 0: Low-speed device 1: Full-speed device

9.5.2 Endpoint n Control Register (EP1/2/3CNTR)

Endpoint 1 Control Register (EP1CNTR)

Endpoint 2 Control Register (EP2CNTR)

Endpoint 3 Control Register (EP3CNTR)

Bit	Field	HW	SW	DF	Description
1-0	EPTYPE	R	R/W	3	Endpoint Type. These bits program the type of endpoint. **Bit 1 Bit 0 Type** 0 0 Un-used 0 1 Isochronous 1 0 Bulk 1 1 Interrupt
2	EPDIR	R	R/W	1	Endpoint Direction 0=OUT 1=IN
4-3	Reserved				
5	EPEN	R	R/W	0	Endpoint Enable/Disable 0=Disable endpoint 1=Enable endpoint
7-6	Reserved				

9.5.3 Endpoint Interrupt Event Register (EPINTR)

Bit	Field	HW	SW	DF	Description
0	INT0RX	R/W	R	0	**EP0 USB RX Event** Set by HW when either SETUP transaction ends with ACK or OUT transaction ends with ACK or STALL. It is also set when SETUPOW (EP0RXTR Register) bit is set. Needs to check EP0RXCSR Register for details. When SW clears all the OUT, SETUP and SETUPOW bits in the EP0RXTR Register, this bit will be cleared automatically.
1	INT0TX	R/W	R/W0C	0	**EP0 USB TX Event** Set by HW when IN transaction ends with ACK or STALL. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.

Bit	Field	HW	SW	DF	Description
2	INT0IN	R/W	R/W0C	0	**EP0 USB IN Token Event** Set by HW when a valid IN token is received. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
3	INT1	R/W	R/W0C	0	**EP1 Interrupt** Set by HW when IN transaction (Interrupt IN / Bulk IN / Isochronous IN) ends with ACK or STALL or OUT transaction (Bulk OUT / Isochronous OUT) ends with ACK or STALL. IN or OUT transaction is determined by Endpoint Type. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
4	INT2	R/W	R/W0C	0	**EP2 Interrupt** Set by HW when IN transaction (Interrupt IN / Bulk IN / Isochronous IN) ends with ACK or STALL or OUT transaction (Bulk OUT / Isochronous OUT) ends with ACK or STALL. IN or OUT transaction is determined by Endpoint Type. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
5	INT3	R/W	R/W0C	0	**EP3 Interrupt** Set by HW when IN transaction (Interrupt IN / Bulk IN / Isochronous IN) ends with ACK or STALL or OUT transaction (Bulk OUT / Isochronous OUT) ends with ACK or STALL. IN or OUT transaction is determined by Endpoint Type. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
6	Reserved				
7	Reserved				

9.5.4 Endpoint Interrupt Event Enable Register (EPINTE)

Bit	Field	HW	SW	DF	Description
0	INT0RXE	R	R/W	0	EP0 USB RX Event Enable
1	INT0TXE	R	R/W	0	EP0 USB TX Event Enable
2	INT0INE	R	R/W	0	EP0 USB IN Token Event Enable
3	INT1E	R	R/W	0	EP1 interrupt Enable
4	INT2E	R	R/W	0	EP2 interrupt Enable
5	INT3E	R	R/W	0	EP3 interrupt Enable
6	Reserved				
7	Reserved				

9.5.5 State Interrupt Event Register (STAINTR)

Bit	Field	HW	SW	DF	Description
0	RSTINT	R/W	R/W0C	0	**USB Bus Reset Event Detect** Set by HW when reset signal is detected on the USB bus. After a USB bus reset, all registers return to their default value and the USB device will be in the default state. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
1	IDLEINT	R/W	R/W0C	0	**USB Bus Suspend Detect** Set by HW when the USB bus is idle every 3ms. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
2	RUEINT	R/W	R/W0C	0	**USB Bus Resume Detect** Set by HW when resume signal is detected. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs. H/W write operation has a higher priority if H/W write and S/W write occur at the same time.
7-3	Reserved				

9.5.6 State Interrupt Event Enable Register (STAINTE)

Bit	Field	HW	SW	DF	Description
0	RSTINTE	R	R/W	0	Enable USB Bus Reset Event Detect
1	IDLEINTE	R	R/W	0	Enable USB Bus Suspend 3ms Detect
2	RUEINTE	R	R/W	0	Enable USB Bus Resume Detect
7-3	Reserved				

9.5.7 Function Address Register (FAR)

Bit	Field	HW	SW	DF	Description
6-0	ADDR	R	R/W	0	USB Device Address
7	Reserved				

9.5.8 Endpoint 0 RX Token Register (EP0RXTR)

Bit	Field	HW	SW	DF	Description
0	OUT	R/W	R/W0C	0	**RX OUT Token** Set by HW to indicate OUT token is received and transaction ends with ACK or STALL. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs.
1	SETUP	R/W	R/W0C	0	**RX SETUP Token** Set by HW to indicate SETUP token is received and transaction ends with ACK. When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs.
2	SETUPOW	R/W	R/W0C	0	**SETUP Overwrite** Set by HW to indicate SETUP token is received when RX FIFO is not empty (regardless whether it is ended with error or ACK). When S/W writes a 0, it will clear this bit, when 1 is written, no change occurs.
7-3	Reserved				

9.5.9 Endpoint 0 RX Command/Status Register (EP0RXCSR)

Bit	Field	HW	SW	DF	Description
0	RXEN	R/W0C	R/W	1	**RX Enable** Set by SW to enable rx USB data. USB data will be written to FIFO and ACK will be returned if the bit “SESTALL” is not set. Clear by HW to indicate transaction ends with ACK or STALL. If this bit is 0,USB data will be discarded and NAK will be returned. SETUP packets will be written to FIFO even this bit is not set and ACK will be returned always. This register will be reset by USB reset or SW reset.
1	SESTALL	R/W	R/W	1	**Send STALL** If set, STALL will be returned to the OUT transaction. SW is allowed to set or clear this bit. HW clears this bit when SETUP transaction ends with ACK. HW sets this bit when STALL is returned to any EP0 transaction.

Bit	Field	HW	SW	DF	Description
2	DTOG	R/W	R	0	**Data Toggle Bit** Updated by HW to indicate the data toggle bit for current USB transaction.
3	DTOGERR	R/W	R	0	**Data Toggle Error** Set by HW to indicate toggle error occurs. Cleared when SW writes a 0 to clear the EP0 RX event interrupt status.
4	ACKSTS	R/W	R	0	**ACK Status** Set by HW when a transaction is completed with ACK handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
5	STALLSTS	R/W	R	0	**STALL Status** Set by HW when a transaction is completed with STALL handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
6	ERRSTS	R/W	R	0	**Error Status** Set by HW to indicate either USB PID error, CRC error, bit stuffing error or no data phase from USB host occur. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL) or when SETUPOW (EP0RXTR Register) is set.
7	CDTOG	R/W0C	W	0	**Clear Endpoint Toggle.** When SW writes a 1 to this bit, it will clear the DTOG bit which is in the same register.

9.5.10 Endpoint 0 TX Command/Status Register (EP0TXCSR)

Bit	Field	HW	SW	DF	Description
0	TXEN	R/W0C	R/W	0	**TX Enable** Set by SW to enable Tx USB data. USB data Is ready in the FIFO and will be sent to USB bus if the bit “SESTALL” is not set. SW should write data then byte count the enabled Tx. Cleared by HW in two cases: Indicate IN transaction ends with ACK or STALL.. After SETUP transaction ends with ACK. This register will be reset by USB reset or SW reset.
1	SESTALL	R/W	R/W	1	**Send STALL** If set, STALL will be returned to the IN transaction. SW is allowed to set or clear this bit. HW clears this bit when SETUP transaction ends with ACK. HW sets this bit when STALL is returned to any EP0 transaction.

Bit	Field	HW	SW	DF	Description
2	DTOG	R/W	R	1	**Data Toggle Bit** Updated by HW to indicate the data toggle bit for current USB transaction.
3	Reserved				
4	ACKSTS	R/W	R	0	**ACK Status** Set by HW when a transaction is completed with ACK handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
5	STALLSTS	R/W	R	0	**STALL Status** Set by HW when a transaction is completed with STALL handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
6	ERRSTS	R/W	R	0	**Error Status** Set by HW to indicate either USB PID error, CRC error, bit stuffing error or no data phase from USB host occur. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL) or when SETUPOW (EP0RXTR Register) is set.
7	CDTOG	R/W0C	W	0	**Clear endpoint Toggle**. When SW writes a 1 to this bit, it will clear the DTOG bit which is in the same register.

9.5.11 Endpoint 0 RX Count Register (EP0RXCTR)

Bit	Field	HW	SW	DF	Description
0-6	EP0RXCT	R/W	R	0	**RX Byte Count** When receive enable is set to 1, this field specifies the receive byte counts in the receive FIFO. This register will be reset by USB reset or SW reset.
7	Reserved				

9.5.12 Endpoint 0 TX Count Register (EP0TXCTR)

Bit	Field	HW	SW	DF	Description
0-6	EP0TXCT	R	R/W	0	**TX Byte Count** When transmit enable is set to 1, this field specifies the transmit byte counts in the transmit FIFO. HW always accesses the FIFO from address0. This register will be reset by USB reset or SW reset.
7	Reserved				

9.5.13 Endpoint 0 RX Data Register (EP0RXDAR)

Bit	Field	HW	SW	DF	Description
0-7	DATA	R/W	R	0	**RX Data** Receive FIFO data will be read by SW through read this register.

9.5.14 Endpoint 0 TX Data Register (EP0TXDAR)

Bit	Field	HW	SW	DF	Description
0-7	DATA	R	W	0	**TX Data** SW writes data to this register will be written to transmit FIFO.

9.5.15 Endpoint n Command/Status Register (EPnCSR)

Endpoint 1 command/status Register (EP1CSR)

Endpoint 2 command/status Register (EP2CSR)

Endpoint 3 command/status Register (EP3CSR)

Bit	Field	HW	SW	DF	Description
0	RXTXEN	R/W0C	R/W	0	RX Enable (Interrupt Out / Bulk Out / Isochronous Out) Set by SW to enable rx USB data. USB data will be written to FIFO and ACK will be returned if the bit “SESTALL” is not set. Cleared by HW to indicate transaction ends with ACK or STALL. If this bit is 0, the USB data will be discarded and NAK will be returned. TX Enable (Interrupt In/Bulk In /Isochronous IN) Set by SW to enable Tx USB data. USB data is ready in the FIFO and will be sent to the USB bus if the bit “SESTALL” is not set. SW should write data then byte count the enabled Tx. Cleared by HW when the IN transaction ends with ACK or STALL. If the transaction ends with ACK, the following USB transaction will be returned with NAK if the bit “SESTALL” is not set. The register will be reset by USB reset or SW reset.
1	SESTALL	R/W	R/W	1	Send STALL If set, STALL will be returned for the transaction. SW is allowed to set or clear this bit. Reserved (Isochronous IN or Isochronous OUT)
2	DTOG	R/W	R	0	Data Toggle Bit (Interrupt IN / Interrupt OUT / Bulk IN / Bulk OUT) Updated by HW to indicate the data toggle bit for current USB transaction. Reserved (Isochronous IN or Isochronous OUT)

Bit	Field	HW	SW	DF	Description
3	DTOGERR	R/W	R	0	Data Toggle Error (Interrupt OUT / Bulk OUT) Reserved (Interrupt In / Bulk In / Isochronous IN / Isochronous OUT) Set by HW to indicate toggle error occurs. Cleared when SW writes a 0 to clear the EPn OUT event interrupt status.
4	ACKSTS	R/W	R	0	ACK Status Set by HW when a transaction is completed with ACK handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
5	STALLSTS	R/W	R	0	STALL Status Set by HW when a transaction is completed with STALL handshake. This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
6	ERRSTS	R/W	R	0	Error Status Set by HW to indicate either USB PID error, CRC error, bit stuffing error, time out without handshake response from USB host (for IN transaction) or no data phase from USB host occur (OUT transaction). This bit will be updated automatically at the next valid transaction (ends with ACK or STALL).
7	CDTOG	R/W0C	W	0	Clear endpoint Toggle. When SW writes 1 to this bit, it will clear the DTOG bit which is in the same register. Reserved (Isochronous IN or Isochronous OUT)

The following table lists the meaning of the Endpoint n command/status Register (EPnCSR) for different Endpoint-Type.

Bit	Interrupt IN	Interrupt OUT	Bulk IN	Bulk OUT	Isochronous IN	Isochronous OUT
0	RXTXEN (TX Enable)	RXTXEN (RX Enable)	RXTXEN (TX Enable)	RXTXEN (RX Enable)	RXTXEN (TX Enable)	RXTXEN (RX Enable)
1	SESTALL	SESTALL	SESTALL	SESTALL	Reserved	Reserved
2	DTOG	DTOG	DTOG	DTOG	Reserved	Reserved
3	Reserved	DTOGERR	Reserved	DTOGERR	Reserved	Reserved
4	ACKSTS	ACKSTS	ACKSTS	ACKSTS	ACKSTS	ACKSTS
5	STALLSTS	STALLSTS	STALLSTS	STALLSTS	STALLSTS	STALLSTS
6	ERRSTS	ERRSTS	ERRSTS	ERRSTS	ERRSTS	ERRSTS
7	CDTOG	CDTOG	CDTOG	CDTOG	Reserved	Reserved

9.5.16 Endpoint n Count Register (EPnCTR)

Endpoint 1 count Register (EP1CTR)

Endpoint 2 count Register (EP2CTR)

Endpoint 3 count Register (EP3CTR)

Bit	Field	HW	SW	DF	Description
0-7	EPnCT	R/W	R/W	0	RX Byte Count (Bulk Out / Isochronous Out) When receive enable is set to 1, this field specifies the receive byte counts in the receive FIFO. TX Byte Count (Interrupt In / Bulk In / Isochronous In) When transmit enable is set to 1, this field specifies the transmit byte counts in the transmit FIFO. HW always accesses the FIFO from Address 0. This register will be reset by USB reset or SW reset.
7	Reserved				

9.5.17 Endpoint n Data Register (EPnDAR)

Endpoint 1 Data Register (EP1DAR)

Endpoint 2 Data Register (EP2DAR)

Endpoint 3 Data Register (EP3DAR)

Bit	Field	HW	SW	DF	Description
0-7	DATA	R/W	R or W	0	RX Data (Bulk Out / Isochronous Out) Receive FIFO data will be read by SW through reading this register. TX Data (Interrupt In / Bulk In / Isochronous In) SW writes data to this register will be written to transmit FIFO.

9.5.18 USB Device SOF Event Register (HINTR)

Bit	Field	HW	SW	DF	Description
0-5	Reserved				
6	SOFINT	R/W	R/W0C	0	Start of frame interrupt. Asserted after the receipt of a valid SOF.
7	Reserved				

9.5.19 USB Device SOF Event Enable Register (HINTE)

Bit	Field	HW	SW	DF	Description
0-5	Reserved				
6	SOFINTE	R	R/W	0	SOF Interrupt Event Enable.
7	Reserved				

9.5.20 Frame Number Low-Byte Register (FNLR)

Bit	Field	HW	SW	DF	Description
0-7	FNLR	R/W	R	0	Bits 0~7 of Frame Number (11 bits)

9.5.21 Frame Number High-Byte Register (FNHR)

Bit	Field	HW	SW	DF	Description
0-2	FNHR	R/W	R	0	Bits 8~10 of Frame Number (11 bits)
3-7	Reserved				

10 Pulse Width Modulation (PWM)

10.1 Overview

The EM77930 has one PWM output with 16-bit resolution. Fig. 10-1 shows the functional block diagram. A PWM output has a period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the period. Fig. 10-2 depicts the relationships between a period and a duty cycle.

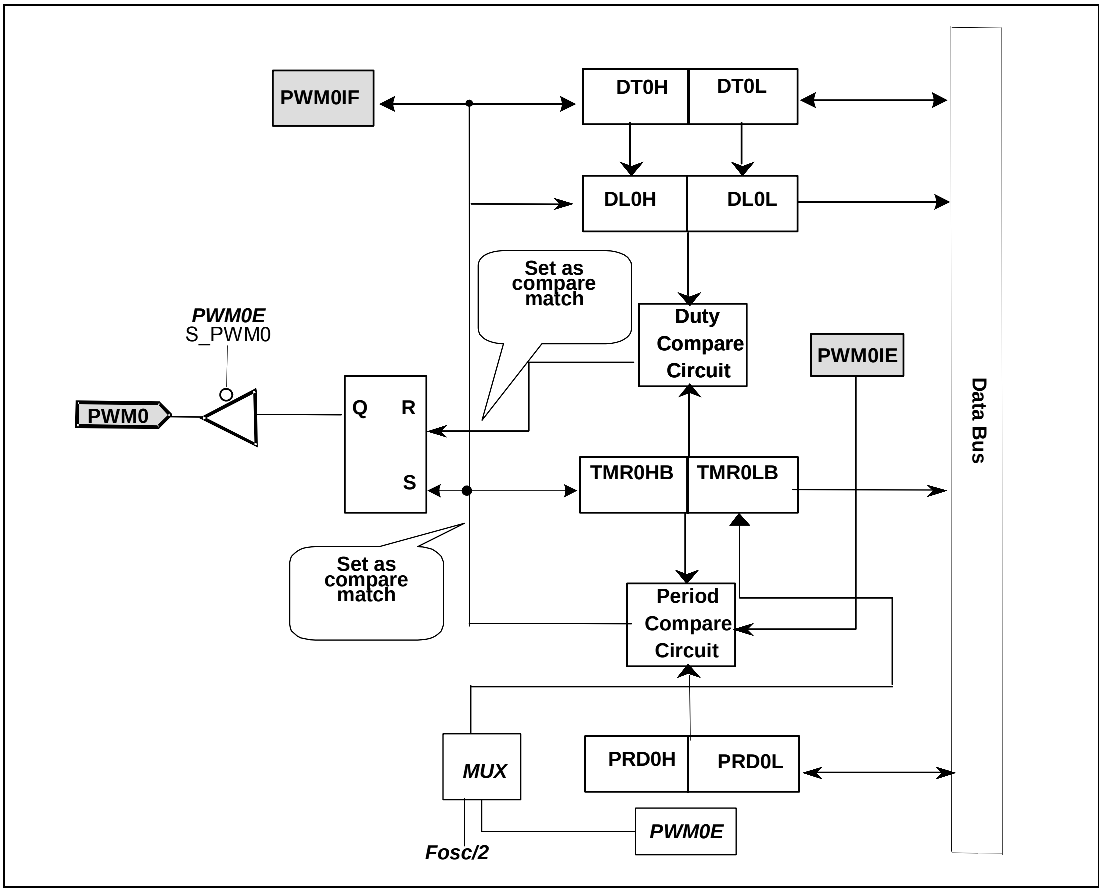


Fig. 10-1 PWM Functional Block Diagram

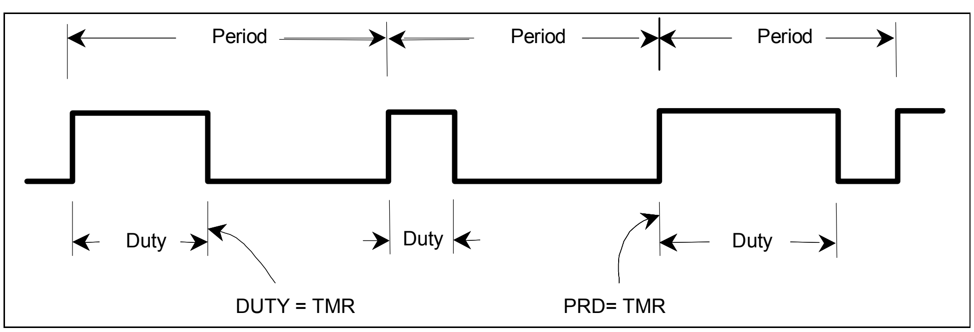


Fig. -2 PWM Output Timing Diagram

10.2 PWM Control Registers

As the PWM mode is defined, the related registers of this operation are shown below:

INTF (0x11): Interrupt flag

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	PWM0IF	EINT1F	EINT0F	TCCOF	FRCOF

DT0L (0x21): Duty of PWM0 low byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT07	DT06	DT05	DT04	DT03	DT02	DT01	DT00

DT0H (0x22): Duty of PWM0 high byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT0F	**DT0E**	**DT0D**	**DT0C**	**DT0B**	**DT0A**	**DT09**	**DT08**

DL0L (0x25): Duty latch of PWM0 low byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DL07	DL06	DL05	DL04	DL03	DL02	DL01	DL00

DL0H (0x26): Duty latch of PWM0 high byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DL0F	DL0E	DL0D	DL0C	DL0B	DL0A	DL09	DL08

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded at any time. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX+1) * (2/Fosc)

PRD0L (0x23): Period of PWM0 low byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD07	PRD06	PRD05	PRD04	PRD03	PRD02	PRD01	PRD00

PRD0H (0x24): Period of PWM0 high byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD0F	PRD0E	PRD0D	PRD0C	PRD0B	PRD0A	PRD09	PRD08

The PWM period is defined by writing to PRDX. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared
- The PWMX pin is set to 1.

- The PWMX duty cycle is latched from DTPS to DUTY.

> **NOTE**
> *The PWMX will not be set if the duty cycle is 0.*

- The PWMXIF pin is set to 1.
- The following formula describes how to calculate the PWM period:

PERIOD = (PRD +2) * (2/Fosc)

The PWM function must be disabled before a new period is executed. In other words, bit PWMXE has to be reset in advance, if the contents of PRDX are reloaded.

PRIE (0x80): Peripherals enable control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	USBE	BBE	-	-	PWM0E	TCCE	FRCE

INTE (0x81): Interrupt enable control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	-	-	PWM0IE	EINT1E	EINT0E	TCCOE	FRCOE

PWMCR (0x98): PWM control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	S_PWM0	-	-

10.3 PWM Programming Procedures/Steps

(1) Load PRDX with the PWMX period.

(2) Load DTX with the PWMX Duty Cycle.

(3) Enable interrupt function by setting PWMXIE in the INTE register, if required.

(4) Set the PWM pin as output by setting PWMCR.S_PWMX.

(5) Enable the PWM function by setting the PWMXE bit in the PRIE register.

(6) Write the desired new duty to DTX before TMRX is equal to PRDX, then this new DTX will be latched into DLX if various duty cycle is required for next the PWMX operation.

(7) Clear the PWMXE bit and write the desired new period to PRDX, then enable it again if various periods are required for the next PWMX operation.

(8) Clear the PWMXIF before the next operation if interrupt PWMXIE is employed.

11 Interrupts

11.1 Introduction

The EM77930 has 17 interrupt sources. By priority, these interrupts are classified into three levels, namely; peripherals, baseband, and USB, and described as following:

The interrupt status registers record the interrupt requests in the corresponding control bits in the interrupt control registers. The global interrupt (GIE) is enabled by the ENI instruction and is disabled by the DISI instruction. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flags in the Interrupt Status Register are set regardless of the status of their corresponding mask bits or the execution of DISI. Note that the logic AND of an interrupt flag and its corresponding interrupt control bit is 1 which makes the program counter point to the right interrupt vector. Refer to Fig. 11. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

Before the interrupt subroutine is executed, the contents of ACC, SR, RAMBS0 and ROMPS will be saved by the hardware. After the interrupt service routine is finished, ACC, SR, RAMBS0 and ROMPS will be pushed back.

In the EM77930, individual interrupt sources have their own interrupt vectors, depicted in the following table:

No	Mnemonic		Priority	Vector	Function	Mask		Status	
	Mask	Status				Register	Bit	Register	Bit
1	KWUAE KWUBE	KWUAIF KWUBIF	1	0x10	Key Wake Up	0x82 0x83	3~0 All	0x12 013	3~0 All
2	EINT0E EINT1E	EINT0F EINT1F	1	0x18	External Interrupt	0x81	2 3	0x11	2 3
3	FRCOE	FRCOF	1	0x20	FRC Overflow	0x81	0	0x11	0
4	TCCOE	TCCOF	1	0x28	TCC Overflow	0x81	1	0x11	1
5	PWM0IE	PWM0IF	1	0x40	PWM period complete	0x81	4	0x11	4
6	CSDE	CSDF	2	0x48	Carrier sense interrupt	0x99	7	0x30	7
7	TX_AEE	TX_AEF	2	0x50	TX FIFO almost empty	0x99	6	0x30	6
8	RX_AFE	RX_AFF	2	0x58	RX FIFO almost full	0x99	5	0x30	5
9	TX_EMPTY	TX_EMPTYF	2	0x60	TX FIFO empty	0x99	4	0x30	4
10	RX_OFE	RX_OFF	2	0x68	RX FIFO overflow	0x99	3	0x30	3
11	LINK_DIS	LINK_DIS	2	0x70	LINK_DIS interrupt	0x99	2	0x30	2

No	Mnemonic		Priority	Vector	Function	Mask		Status	
	Mask	Status				Register	Bit	Register	Bit
12	LOCK_OUTE	LOCK_OUTF	2	0x78	Lock out interrupt	0x99	1	0x30	1
13	LOCK_INE	LOCK_INF	2	0x80	Lock in interrupt	0x99	0	0x30	0
14	INT0RXE	INT0RXF	3	0x88	EP0 USB RX Event	0x1D2	0	0x1D1	0
14	INT0TXE	INT0TXF	3		EP0 USB TX Event	0x1D2	1	0x1D1	1
14	INT0INE	INT0INF	3		EP0 USB IN Token Event	0x1D2	2	0x1D1	2
15	INT1E	INT1F	3	0x90	EP1 Interrupt	0x1D2	3	0x1D1	3
15	INT2E	INT2F	3		EP2 Interrupt	0x1D2	4	0x1D1	4
15	INT3E	INT3F	3		EP3 Interrupt	0x1D2	5	0x1D1	5
16	RSTINTE	RSTINTF	3	0x98	USB Bus Reset Event Detect	0x1D4	0	0x1D3	0
16	IDLEINTE	IDLEINTF	3		USB Bus Suspend Event Detect	0x1D4	1	0x1D3	1
16	RUEINTE	RUEINTF	3		USB Bus Resume Event Detect	0x1D4	2	0x1D3	2
16	FRWPINTE	FRWPINTF	3		Function Remote Wake-Up Interrupt	0x1D4	3	0x1D3	3
17	SOFINTE	SOFINTF	3	0XA8	Start Of Frame Interrupt	0x1E8	6	0x1E7	6

The interrupt priority is another useful feature provided by this IC. The latest interrupt, which has the highest priority than the others, will override and hold the currently executed interrupt until the interrupt is finished. Otherwise, the latest interrupt will be in queue right after all its peers.

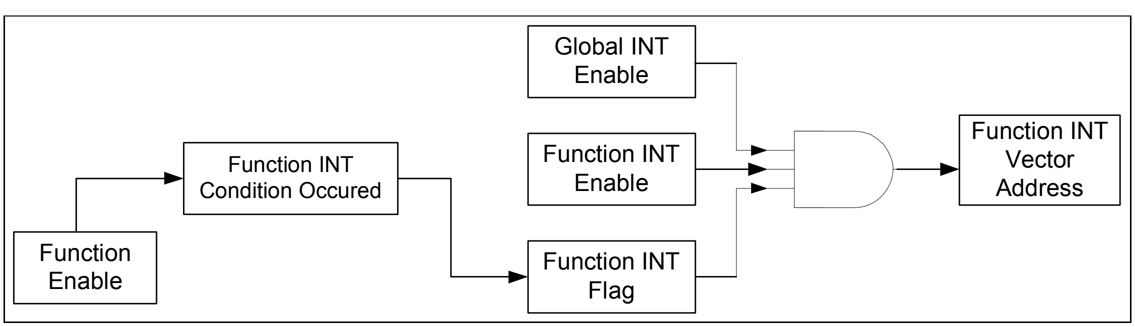


Fig. 11 Block Diagram of Interrupts

12 Circuitry of Input and Output Pins

12.1 Introduction

The EM77930 has five parallel ports, namely: Port A, Port B, Port C, Port D and Port F which only two least significant bits are available. That is, there are 30 available I/O pins. A control bit defines the configuration of its corresponding pin. Refer to Fig. 3-1 for the Pin Assignment.

The I/O registers, from Port A to Port F, are bidirectional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOCA, IOCB, IOCC, IOCD and IOCF) under program control. The I/O registers and I/O control registers are both readable and writable. Note that the source is different between the reading path of input and output pin while reading the I/O port.

13 Timer/Counter System

13.1 Introduction

The EM77930 provides two timer modules: 8-bit TCC (Timer Clock/Counter), and 16-bit FRC (Free Run Counter). The TCC clock source comes from one of the instruction cycle and low frequency oscillator (IRC). The FRC clock source is from either instruction cycle or low frequency oscillator (IRC).

13.2 Time Clock Counter (TCC)

An 8-bit counter is available as prescaler for the TCC. The prescaler ratio is determined by the PS0~PS2 bits. When in TCC mode, the prescaler is cleared each time an instruction writes to the TCC.

- TCC is an 8-bit timer/counter. If the TCC signal source is from the system clock, TCC will be incremented by 1 in every instruction cycle (without prescaler).
- If the TCC signal source is from the IRC clock input, the TCC will be incremented by 1 on every falling edge or rising edge of the TCC pin.
- The prescaler counter (PRC) can be read from Address 0x0F. In other words, the combination of TCC and PRC can be used as a 16-bit counter without prescaler.

13.2.1 Block Diagram of TCC

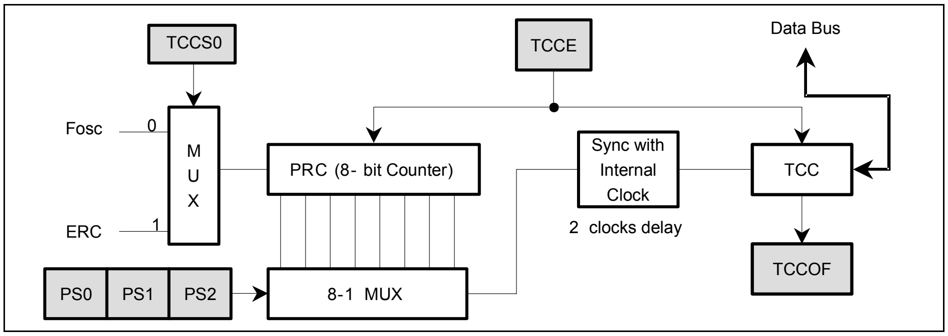


Fig. 13-1 Function Block Diagram of TCC

13.2.2 TCC Control Registers

As the TCC mode is defined, the related registers involved in this operation are shown below:

PRC (0x0F): Prescaler counter

TCC (0x10): Timer clock/counter

INTF (0x11): Interrupt flag

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	-	-	PWM0IF	EINT1F	EINT0F	TCCOF	FRCOF

PRIE (0x80): Peripherals enable control

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	USBE	BBE	-	-	PWM0E	TCCE	FRCE

INTE (0x81): Interrupt enable control

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
GIE	-	-	PWM0IE	EINT1E	EINT0E	TCCOE	FRCOE

TCCC (0x93): Timer clock/counter control

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	-	-	-	TCCS0	PS2	PS1	PS0

13.2.3 TCC Programming Procedures/Steps

(1) Load TCCC with the prescaler and TCC clock source.

(2) Load the TCC with the TCC overflow period.

(3) Enable the interrupt function by setting TCCOE in the INTE register, if required.

(4) Enable the TCC function by setting the TCCE bit in the PRIE register.

(5) Wait for either the interrupt flag to be set (TCCOF) or the TCC interrupt to occur.

(6) The following formula describes how to calculate the TCC overflow period:

$$TCC\ Timer = (0\times 100 - TCC) \times \mathrm{Pr}\,escaler\left(\frac{1}{ClockSource}\right)$$

where ***Clock Source = Fosc or IRC***

13.3 Free Run Counter

Dual 8-bit counters, high byte register and low byte register, make up the 16-bit software programmable counter. The driving clock source is either the system clock divided by 2 or the low frequency oscillator. A read of the low byte register allows full control of the corresponding timer function. On the contrary, accessing a high byte register will inhibit the specific timer function until the corresponding low byte is read as well.

13.3.1 Block Diagram of FRC

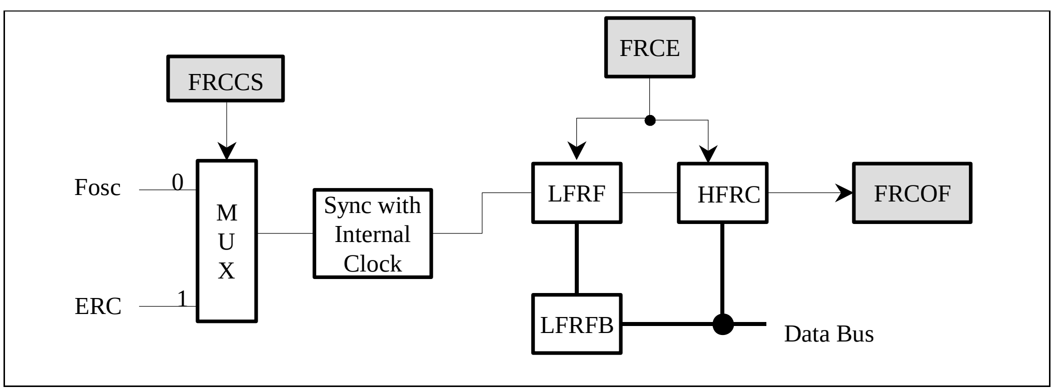


Fig. 13-2 Timer 1 Function Block Diagram

13.3.2 FRC Control Registers

As the FRC mode is defined, the related registers involved in this operation are shown below:

INTF (0x11): Interrupt flag.

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	-	-	PWM0IF	EINT1F	EINT0F	TCCOF	FRCOF

LFRC (0x1A): Least significant byte of 16-bit free run counter.

HFRC (0x1B): Most significant byte of 16-bit free run counter.

LFRCB (0x1C): Least significant byte buffer of 16-bit free run counter.

PRIE (0x80): Peripherals enable control

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	USBE	BBE	-	-	PWM0E	TCCE	FRCE

INTE (0x81): Interrupt enable control

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
GIE	-	-	PWM0IE	EINT1E	EINT0E	TCCOE	FRCOE

FRCC (0x94): Free run counter control.

Bit 7	Bit 76	Bit 75	Bit 74	Bit 73	Bit 72	Bit 71	Bit 70
-	OCSO2E	OSCO2SL1	OSCO2SL0	PPSCL2	PPSCL1	PPSCL0	FRCCS

13.3.3 FRC Programming Procedures/Steps

(1) Load the LFRCB with the FRC overflow period low byte.

(2) Load the HFRC with the TCC overflow period high byte. Then the LFRC will automatically load with the LFRCB.

(3) Enable the interrupt function by setting FRCOE in the INTE register, if required.

(4) Enable FRC function by setting the FRCE bit in the PRIE register.

(5) Wait for either the interrupt flag to be set (FRCOF) or the FRC interrupt to occur.

(6) A low byte access on the 16-bit counter receives the count value at the instance of reading. However, the low byte contents will be transferred to the buffer, the LFRCB register, if a high byte is read first. The value in the LFRCB register remains unchanged until the corresponding low byte is read.

(7) The following formula describes how to calculate the FRC overflow period:

$$FRC\ \ Timer = (0 \times 100 - HFRC : LFRC) \times \left(\frac{1}{ClockSource} \right)$$

where **Clock Source = Fosc or IRC**

14 Reset and Wake Up

14.1 Reset

The reset can be caused by one of the following:

(1) Power-on reset

(2) /RESET pin input "low", or

(3) Watchdog timer time-out (if enabled)

The device will remain in a reset condition for a period of 8-bit internal RC ripple counter (one oscillator start-up timer period) after the reset is detected. The initial Address is 000h.

14.2 The Status of RST, T, and P of STATUS Register

A reset condition can be caused by the following events:

(1) A power-on condition (external);

(2) A high-low-high pulse on the /RESET pin (external); and

(3) Watchdog timer time-out (internal).

The values of bits RST, T and P, listed in Table 14.1 can be used to check how the processor wakes up.

Table 14.1 Values of RST, T and P after a reset

Condition	RST	T	P
Power on	0	1	1
WDTC instruction	*P	1	*P
WDT timeout	*P	0	*P
SLEEP instruction	*P	*P	0
Wake-Up on pin change during Sleep mode	1	1	0

*P: Previous status before reset

14.3 System Set-up (SSU) Time

In order to have a successful start up, System Set-up Time (SSU) is employed to guarantee a stable clock for IC operation. It is made up of two delay sources:

(1) Internal RC Oscillation Set-up Delay (IRCOSUD): Internal RC oscillation shared with a watchdog timer divided by a 6-bit ripple counter. The RC delay controlled by bit IRCDE in the Code Option is optional.

(2) Main Oscillation Set-up Delay (MOSUD): A 10-bit ripple counter is used to filter unstable main clocks at the beginning of power-on before the chip starts to run. This delay is performed right after IRCOSUD, if enabled.

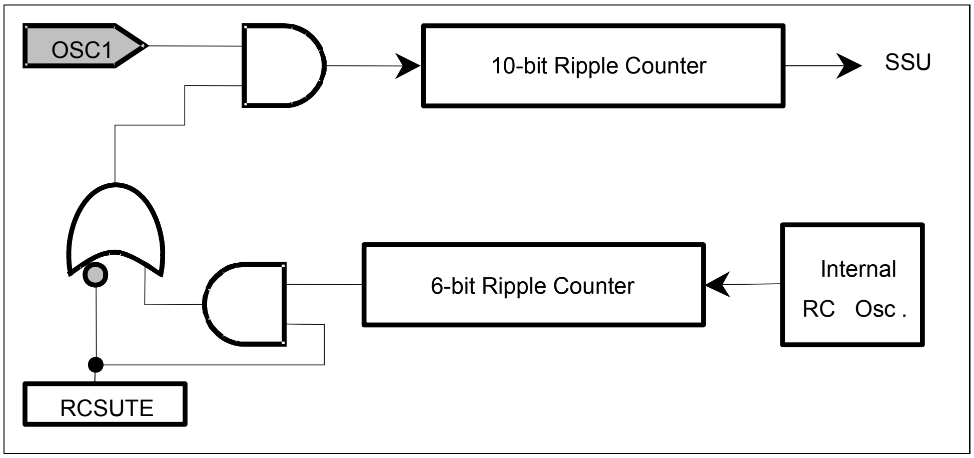


Fig. 13 System Set-up Time

14.4 Wake-up Procedure on Power-on Reset

Power-on Voltage Detector (POVD) will allow the VDD whose value is over the default threshold voltage (2.0 V for the EM77930) enter the IC, and the SSU delay starts. The following three cases may be taken into consideration:

(1) /RESET pin goes high with VDD at the same time. In hardware, this pin and VDD are tied together. The internal reset will remain low until the SSU delay is over.

(2) /RESET pin goes high during the SSU delay. It is similar to Case 1. The IC will start to operate as the SSU delay is over.

/RESET pin goes high after the SSU delay. The EM77930 will start program execution immediately.

15 Oscillators

15.1 Introduction

The EM77930 provides three main oscillators: One high frequency crystal oscillator (connected to OSCI), internal RC, and four PLL (Phase Lock Loop) Outputs. Versatile combinations of oscillation are provided for wild applications. On-chip clock sources can be either dual clocks or single clock.

15.2 Clock Signal Distribution

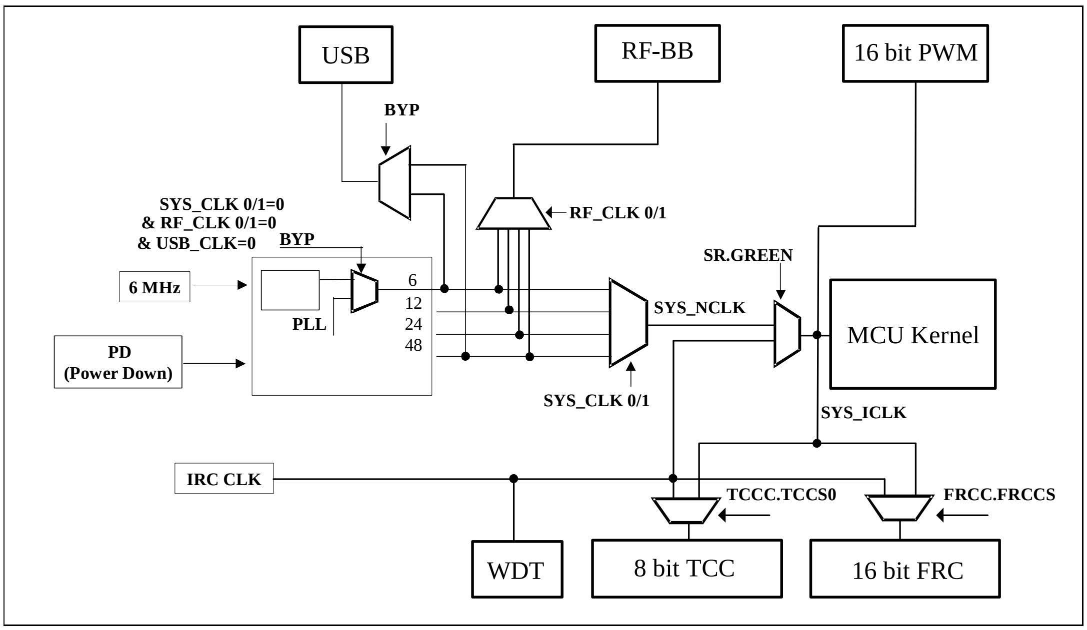


Fig. 14 Clock Tours

15.3 PLL Oscillator

The Phase-locked loop (PLL) technology is employed to produce four different frequencies: 6 MHz, 12MHz, 24MHz and 48 MHz (external 6MHz crystal). 6 MHz is the system clock source and 48 MHz is USB device and Hub clock source only. PLL is enabled except when entering Green and Sleep mode.

16 Low-Power Mode

16.1 Introduction

The EM77930 has two power-saving modes, green mode and sleep mode. Figure 16 shows the mode change diagram.

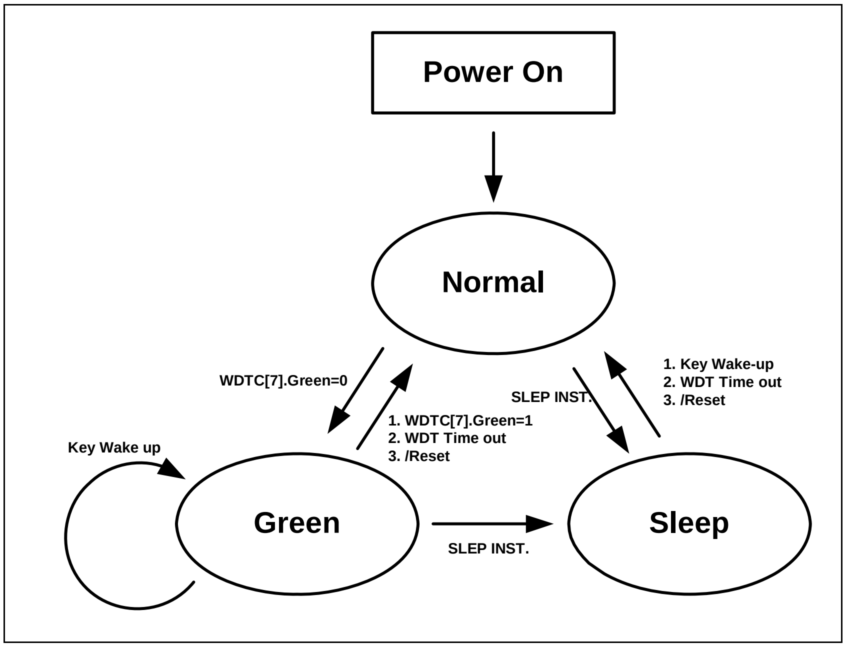


Fig. 16 Three Mode State

16.2 Green Mode

The “GREEN” bit of WDTC [7] register is the only control bit used for mode switching, between normal mode and green mode. Its initial value is “0”, normal mode. When “GREEN” bit is written with a 1, the MCU will switch to green mode from normal mode. In contrast, the MCU will go back to normal mode when the “GREEN” bit is written from 1 to 0. During green mode, the main oscillator will be turned off. The MCU and all the peripherals are driven by the external RC oscillator - IRC.

Once RF peripheral is functional and then switched into green mode, the clock source for all the other peripherals, except PLL, will be provided by IRC. PLL will keep running as RF circuit’s clock source.

16.3 Sleep Mode

The execution of “SLEP” instruction will turn the whole chip into Sleep mode. The main clock will be shut down. The IRC oscillator is halted also if the watchdog function is disabled. All registers, memory and I/O port remain in their previous states during sleep mode. The overflow of the watchdog timer driven by IRC will generate a reset to resume normal operation. Key Wake up (KWU) interrupt and /RESET pin are other methods to exit sleep mode. It is essential to wait for stable Oscillation start up time before normal operation. The stabilizing time is SST.

17 Instruction Description

17.1 Instruction Set Summary

Type	Instruction Binary				Mnemonic	Operation	Status Affected	Cycles
System Control	0000	0000	0000	0000	NOP	No operation	None	1
	0000	0000	0000	0001	WDTC	WDT ← 0	None	1
	0000	0000	0000	0010	RET	PC ← (Top of Stack)	None	1
	0000	0000	0000	0011	RETI	PC ← (Top of Stack); Enable Interrupt	None	1
	0000	0000	0000	0100	SLEP	WDT ← 0 Stop oscillator	None	1
	0000	0000	0000	0101	ENI	Enable Interrupt	None	1
	0000	0000	0000	0110	DISI	Disable Interrupt	None	1
	0000	0000	0000	0111	DAA	Decimal Adjust A	C	1
Table Look up	1010	0000	rrrr	rrrr	TBRDP r	r ← ROM[(TABPT[15:1])] TABPT ← TABPT+1	None	2
	1010	0001	rrrr	rrrr	TBRD r	r ← ROM[(TABPT[15:1])]	None	2
	1010	0010	rrrr	rrrr	TBRDM r	r ← ROM[(TABPT[15:1])] TABPT ← TABPT-1	None	2
	0000	0000	0000	1010	TBRDP A	A ← ROM[(TABPT[15:1])] TABPT ← TABPT+1	None	2
	0000	0000	0000	1011	TBRD A	A ← ROM[(TABPT[15:1])]	None	2
	0000	0000	0000	1100	TBRDM A	A ← ROM[(TABPT[15:1])] TABPT ← TABPT-1	None	2
	0011	1101	0000	0010	TBL	R2 ← R2+A	C, DC, Z	1
	1010	1011	kkkk	kkkk	RETL #k	A ← k PC ← [Top of Stack]	None	1

Type	Instruction Binary				Mnemonic	Operation	Status Affected	Cycles
Logic	0000	0001	rrrr	rrrr	OR A, r	A ← A .or. r	Z	1
	0000	0010	rrrr	rrrr	OR r, A	r ← r .or. A	Z	1
	0000	0011	kkkk	kkkk	OR A, #k	A ← A .or. k	Z	1
	0000	0100	Rrrr	rrrr	AND A, r	A ← A .and. r	Z	1
	0000	0101	Rrrr	rrrr	AND r, A	r ← r .and. A	Z	1
	0000	0110	kkkk	kkkk	AND A, #k	A ← A .and. k	Z	1
	0000	0111	Rrrr	rrrr	XOR A, r	A ← A .xor. r	Z	1
	0000	1000	rrrr	rrrr	XOR r, A	r ← r .xor. A	Z	1
	0000	1001	kkkk	kkkk	XOR A, #k	A ← A .xor. k	Z	1
	0000	1010	rrrr	rrrr	COMA r	A ← /r	Z	1
	0000	1011	rrrr	rrrr	COM r	r ← /r	Z	1
	1011	00kk	rrrr	rrrr	RRCA r, #k	[C,r] rotate right k bits to [C,A]	C	1
	1011	01kk	rrrr	rrrr	RRC r, #k	[C,r] rotate right k bits to [C,r]	C	1
	1011	10kk	rrrr	rrrr	RLCA r, #k	[C,r] rotate left k bits to [C,A]	C	1
	1011	11kk	rrrr	rrrr	RLC r, #k	[C,r] rotate left k bits to [C,r]	C	1
	0101	10kk	rrrr	rrrr	SHRA r, #k	[C,r] shift right k bits to A Insert C into high order bits	None	1
	0101	11kk	rrrr	rrrr	SHLA r, #k	[C,r] shift left k bits to A Insert C into low order bits	None	1
Compare Branch	0001 xxaa	0bbb aaaa	rrrr aaaa	rrrr aaaa	JBC r,b,addr	If r(b)=0, jump to addr	None	2/3*
	0001 xxaa	1bbb aaaa	rrrr aaaa	rrrr aaaa	JBS r,b,addr	If r(b)=1, jump to addr	None	2/3*
	0101 xxaa	0010 aaaa	rrrr aaaa	rrrr aaaa	DJZA r,addr	A ←r-1, jump to addr if zero	None	2/3*
	0101 xxaa	0011 aaaa	rrrr aaaa	rrrr aaaa	DJZ r,addr	r ←r-1, jump to addr if zero	None	2/3*
	0101 xxaa	0100 aaaa	rrrr aaaa	rrrr aaaa	JZA r,addr	A←r+1, jump to addr if zero	None	2/3*
	0101 xxaa	0101 aaaa	rrrr aaaa	rrrr aaaa	JZ r,addr	r ←r+1, jump to addr if zero	None	2/3*

Note: *Condition for successful instruction execution needs 2/3 cycles (jump to address).

Type	Instruction Binary				Mnemonic	Operation	Status Affected	Cycles
Process	0010	0bbb	rrrr	rrrr	BC r,b	r(b) ← 0	None	1
	0010	1bbb	rrrr	rrrr	BS r,b	r(b) ← 1	None	1
	0011	0bbb	rrrr	rrrr	BTG r,b	r(b) ← /r(b)	None	1
	0011	1000	rrrr	rrrr	SWAP r	r(0:3) ↔ r(4:7)	None	1
	0011	1001	rrrr	rrrr	SWAPA r	A(4:7) ← r(0:3) A(0:3) ← r(4:7)	None	1
	1010	1100	rrrr	rrrr	ZCHK r	Z ← 0 if r < > 0	Z	1
	0000	0000	0000	1101	RPT	Single repeat CS times on next TBRD instruction	None	1
	1010	1111	rrrr	rrrr	CLR r	r ← 0	Z	1
Arithmetic	0011	1100	rrrr	rrrr	ADD A,r	A ← A+r	C, DC, Z	1
	0011	1101	rrrr	rrrr	ADD r,A	r ← r+A	C, DC, Z	1
	0011	1110	kkkk	kkkk	ADD A,#k	A ← A+k	C, DC, Z	1
	0100	0010	rrrr	rrrr	SUB A,r	A ← r-A	C, DC, Z	1
	0100	0011	rrrr	rrrr	SUB r,A	f ← r-A	C, DC, Z	1
	0100	0100	kkkk	kkkk	SUB A,#k	A ← k-A	C, DC, Z	1
	0100	1110	rrrr	rrrr	INCA r	A ← r+1	C, DC, Z	1
	0100	1111	rrrr	rrrr	INC r	r ← r+1	C, DC, Z	1
	0101	0000	rrrr	rrrr	DECA r	A ← r-1	C, DC, Z	1
	0101	0001	rrrr	rrrr	DEC r	r ← r-1	C, DC, Z	1
Move	1010	1000	rrrr	rrrr	MOV A,r	A ← r	Z	1
	1010	1001	rrrr	rrrr	MOV r,A	r ← A	None	1
	0110	r_2 r_2 r_2 r_2	r_2 r_2 r_1 r_1	r_1 r_1 r_1 r_1	MOVRR r_1, r_2	Register r_1 ← Register r_2	None	1
	1010	0111	kkkk	kkkk	MOV A,#k	A ← k	None	1
Branch	110a	aaaa	aaaa	aaaa	JMP addr	PC ← addr PC[13..16] unchange	None	1
	111a	aaaa	aaaa	aaaa	CALL addr	[Top of Stack] ← PC + 1 PC ← addr PC [13..16] unchange	None	1
Bank	1010	1110	0000	0kkk	BANK #k	R4(RAMBS0) ← k (0~6)	None	1
Page	1010	1101	0000	000k	PAGE #k	R5(PAGES) ← k (0~1)	None	1

18 Electrical Specification

18.1 Absolute Maximum Ratings

Temperature Under Bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+3.6V
Output voltage	-0.3V	to	+3.6V

18.2 DC Electrical Characteristic

Ta=0°C ~ 70 °C, VDD=3.3V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD ~ 2.75V	One cycle with one clock	DC	–	48.0	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±2	μA
VIH	Input High Voltage	Port A ~ Port F	0.8xVDD	–	–	V
VIL	Input Low Voltage	Port A ~ Port F	VSS	–	0.2xVSS	V
VIHT	Input High Threshold Voltage	/RST	2.0	–	–	V
VILT	Input Low Threshold Voltage	/RST	–	–	0.8	V
VIHX	Clock Input High Voltage	OSCI, OSCO	2.5	–	–	V
VILX	Clock Input Low Voltage	OSCI, OSCO	–	–	1.0	V
VOH1	Output High Voltage: PTA, PTC, PTD, PTE, PTF	IOH = -8.0 mA	2.4	–	–	V
VOH2	Output High Voltage: PTB; RFIO	IOH = -8.0 mA	2.4	–	–	V
VOL1	Output Low Voltage: PTA, PTC, PTD, PTE, PTF	IOL = 8.0 mA	–	–	0.4	V
VOL2	Output Low Voltage: (1) PTB; RFIO	IOL = 8.0 mA	–	–	0.4	V
IPH	Pull-high current	Pull-high active, input pin at VSS	–	-6.5	–	μA
ISB	Power down current	All input and I/O pins at VDD, Output pin floating, WDT and all peripherals disabled.	–	–	–	μA
ICC1	Operating supply current (VDD = 3.3V)	/RESET = 'High', Fosc = 32kHz (RC type), Output pin floating, WDT and all peripherals disabled.	–	10	–	μA
ICC3	Operating supply current (VDD = 3.3V)	/RESET= 'High', Fosc = 6MHz (Crystal type), Output pin floating, and all peripherals disabled.	–	6	–	mA

18.3 Voltage Detector Electrical Characteristic

Ta=25°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Vdet	Detect voltage	–	1.8	2.0	2.2	V
Vrel	Release voltage	–	–	Vdet × 1.05	–	V
Iss	Current consumption	VDD = 3V	–	–	0.8	µA
Vop	Operating voltage	–	0.7*	–	3.5	V
ΔVdet/ΔTa	Vdet Temperature characteristic	0°C ≤Ta≤ 70°C	–	–	-2	MV/°C

* When the voltage of VDD rises between Vop=0.7V and Vdet, the voltage detector output must be "Low".

18.4 AC Electrical Characteristic

18.4.1 MCU

Ta=0°C ~ 70 °C, VDD=3.3 V±5%, VSS=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type RC type	125 500	–	DC DC	ns ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	9	18	30	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	9	18	30	ms
Tset	Input pin setup time	–	–	0	–	ms
Thold	Input pin hold time	–	–	20	–	ms
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ms

* N= selected prescaler ratio.

18.4.2 BB

Ta=0°C ~ 70 °C, VDD=3.3 V±5%, VSS=0V

Symbol	Parameter	Min	Max	Unit
$1/t_{OSC}$	Oscillator frequency	0.1	24	MHz
t_{RDPW}	RD pulse width	3*t_{OSC}+ Δ	–	ns
t_{CSRD}	CS low to RD low	tOSC	–	ns
t_{ADRD}	Address valid for RD low	0	–	ns
t_{RDDV}	RD low to Data valid	–	3*tOSC+Δ	ns
t_{RHDT}	Data float after RD.	–	tOSC	ns
t_{DHAR}	Data hold after RD	0	–	ns
t_{RHDT}	Time between consecutive RD pulses	2*tOSC	–	ns
t_{RDAN}	Address valid after RD low	3*tOSC+Δ	–	ns

Δ>0 will be determined according to cell library simulation.

The values above were determined according to behavioral simulations. They take into account only the BB digital state-machine. Thus, such values are for reference only.

19 Application Circuit

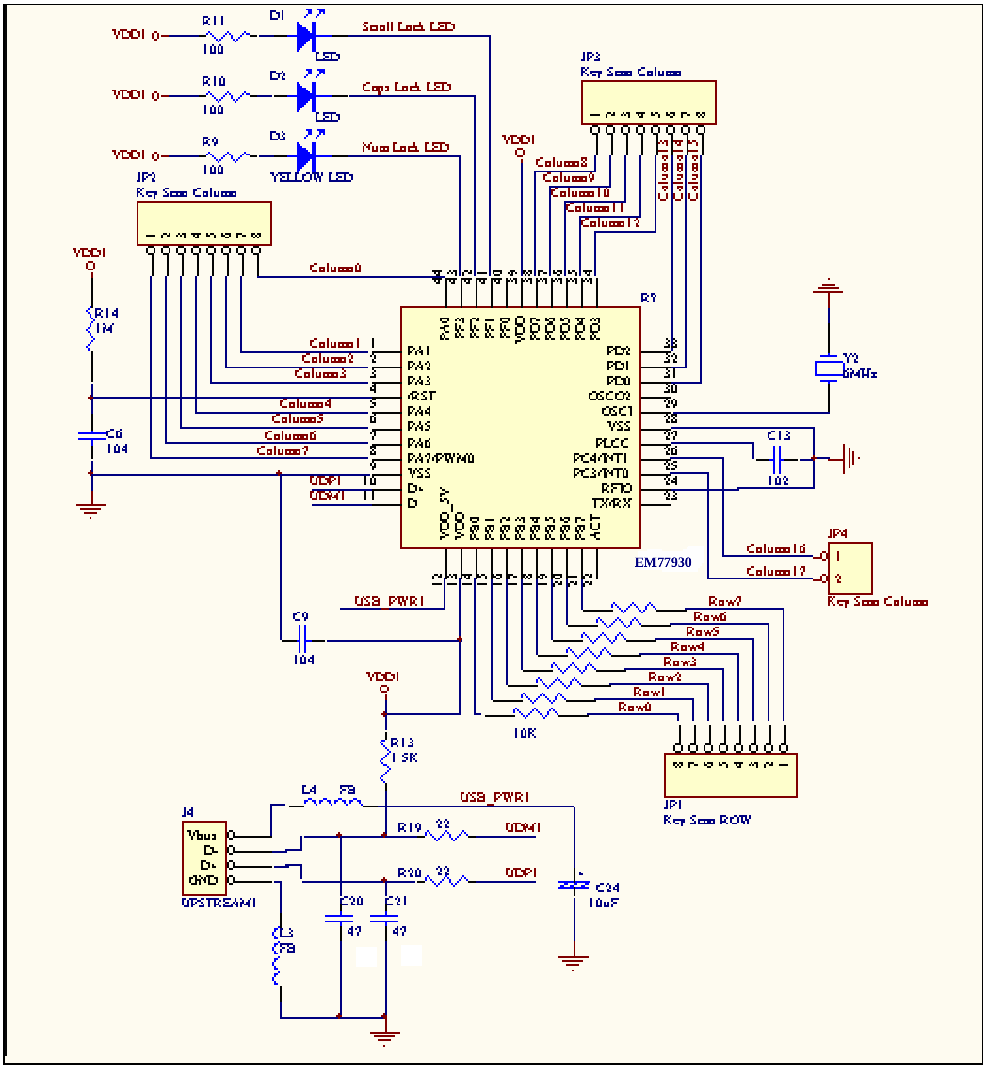


Fig. 18 USB Keyboard Circuit

Keyboard Setting:

Port A, Port C, Port D: Key Scan Column

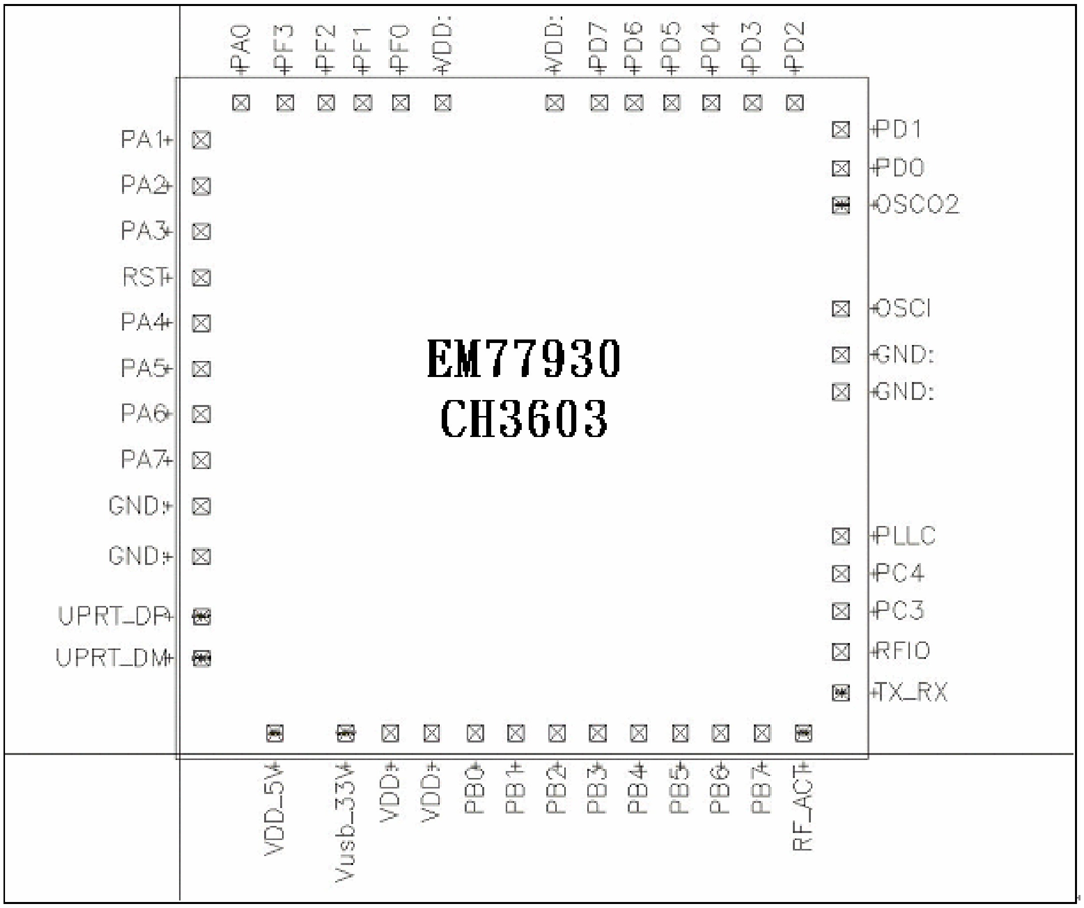
Port B: Key Scan Row

Port F.1: Scroll Lock LED

Port F.2: Caps Lock LED

Port F.3: Num Lock LED

20 Pad Description



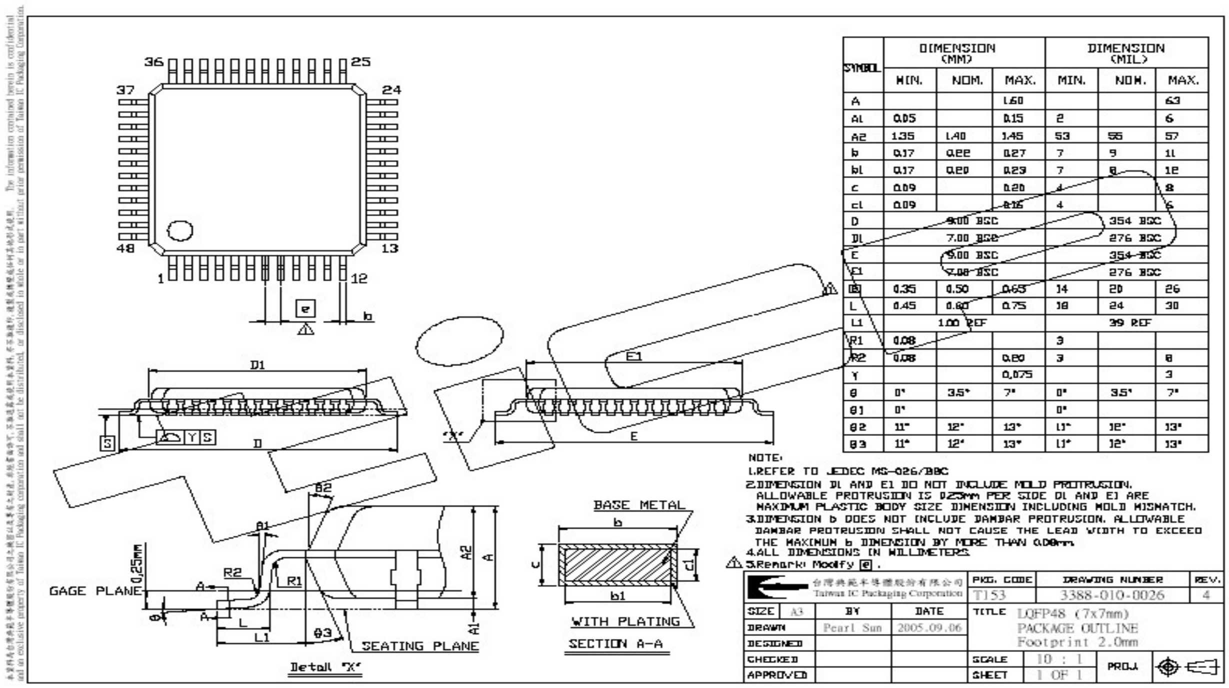
Pad Name & Pad Coordinates Table							
Structure Name: EM77930				Structure Name:			
Chip Size：3114 X 3116							
Pin No.	**Pad Name**	**X**	**Y**	**Pin no.**	**Pad Name**	**X**	**Y**
1	PA1	97.1	2844.874	23	TX_RX	3016.428	283.77
2	PA2	97.1	2632.001	24	RFIO	3016.428	473.951
3	PA3	97.1	2421.65	25	PC3	3016.428	659.981
4	RST	97.1	2207.793	26	PC4	3016.428	834.832
5	PA4	97.1	1996.14	27	PLLC	3016.428	1008.099
6	PA5	97.1	1783.585	28	GND:	3016.428	1677.167
7	PA6	97.1	1574.051	28	GND:	3016.428	1849.461
8	PA7	97.1	1359.377	29	OSCI	3016.428	2062.597
9	GND:	97.1	1147.191	30	OSCO2	3016.428	2543.513
9	GND:	97.1	915.239	31	PD0	3016.428	2714.764
10	UPRT_DP	100.508	637.237	32	PD1	3016.428	2891.764
11	UPRT_DM	100.508	442.737	33	PD2	2804.123	3017.411
12	VDD_5V	433.316	97.1	34	PD3	2613.123	3017.411
13	VUSB_33V	757.53	97.1	35	PD4	2424.929	3017.411
13	VDD:	961.252	97.1	36	PD5	2243.899	3017.411
13	VDD:	1149.099	97.1	37	PD6	2072.155	3017.411
14	PB0	1348.453	97.1	38	PD7	1913.055	3017.411
15	PB1	1532.693	97.1	39	VDD:	1709.377	3017.411
16	PB2	1719.98	97.1	39	VDD:	1197.71	3017.411
17	PB3	1907.234	97.1	40	PF0	1007.255	3017.411
18	PB4	2094.063	97.1	41	PF1	834.279	3017.411
19	PB5	2282.768	97.1	42	PF2	667.244	3017.411
20	PB6	2466.56	97.1	43	PF3	479.878	3017.411
21	PB7	2656.054	97.1	44	PA0	279.011	3017.411
22	RF_ACT	2844.284	97.1				

APPENDIX

A Package Type

ET NO	Package Type	Pin Count	Package Size
EM77930	LQFP48	48	7X7MM

B Package Information



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.35	0.50	0.65	14	20	26
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°