12-Mbit (512K X 24) Static RAM

Features

- **High speed**
  - **— t_{AA} = 8 ns**
- **Low active power**
  - **— I_{CC} = 185 mA @ 8 ns**
- **Low CMOS standby power**
  - **— I_{SB2} = 25 mA**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Available in Lead Pb-Free Standard 119-ball PBGA**

Functional Description

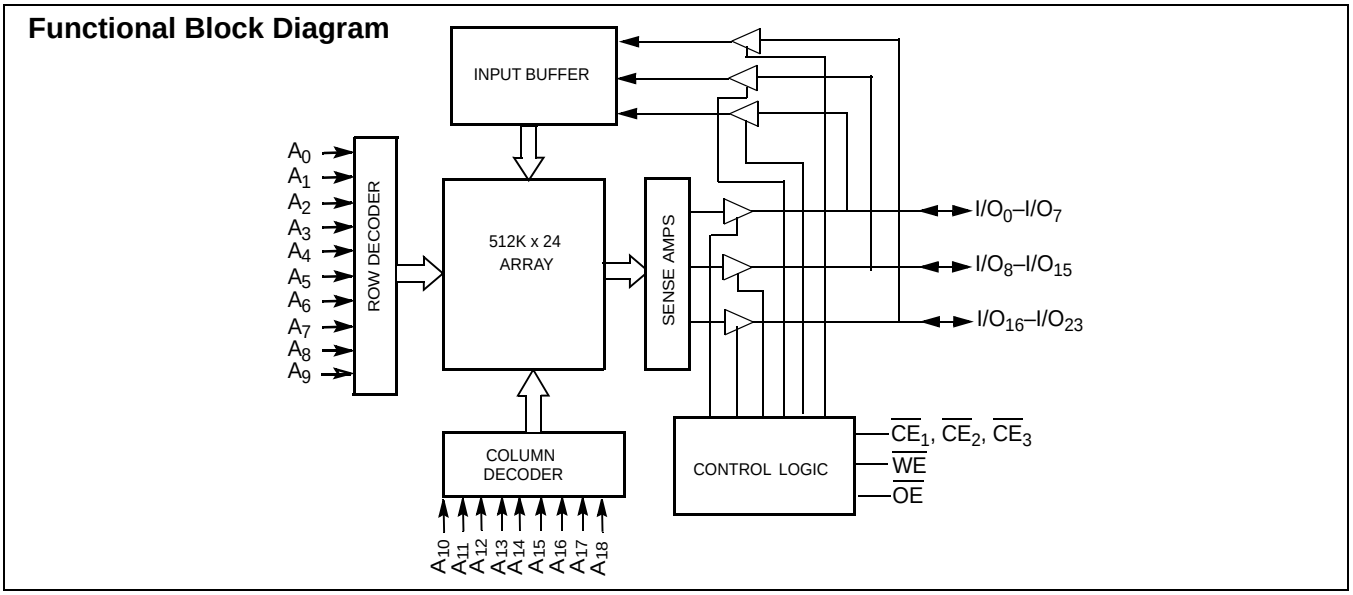
The CY7C1012DV33 is a high-performance CMOS static RAM organized as 512K words by 24 bits. Each data byte is separately controlled by the individual chip selects ($\overline{CE_1}$, $\overline{CE_2}$, $\overline{CE_3}$). $\overline{CE_1}$ controls the data on the I/O_0–I/O_7, while $\overline{CE_2}$ controls the data on I/O_8–I/O_{15}, and $\overline{CE_3}$ controls the data on the data pins I/O_{16}–I/O_{23}. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing the data bytes into the SRAM is accomplished when the chip select controlling that byte is LOW and the write enable input ($\overline{WE}$) input is LOW. Data on the respective input/output (I/O) pins is then written into the location specified on the address pins (A_0–A_{18}). Asserting all of the chip selects LOW and write enable LOW will write all 24 bits of data into the SRAM. Output enable ($\overline{OE}$) is ignored while in WRITE mode.

Data bytes can also be individually read from the device. Reading a byte is accomplished when the chip select controlling that byte is LOW and write enable ($\overline{WE}$) HIGH while output enable ($\overline{OE}$) remains LOW. Under these conditions, the contents of the memory location specified on the address pins will appear on the specified data input/output (I/O) pins. Asserting all the chip selects LOW will read all 24 bits of data from the SRAM.

The 24 I/O pins (I/O_0–I/O_{23}) are placed in a high-impedance state when all the chip selects are HIGH or when the output enable ($\overline{OE}$) is HIGH during a READ mode. For further details, refer to the truth table of this data sheet.

Functional Block Diagram



Selection Guide

	–8	Unit
Maximum Access Time	8	ns
Maximum Operating Current	185	mA
Maximum CMOS Standby Current	25	mA

Pin Configurations[1]

119 PBGA
Top View

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE}_1$	A	A	NC
C	I/O_{12}	NC	$\overline{CE}_2$	NC	$\overline{CE}_3$	NC	I/O_0
D	I/O_{13}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_1
E	I/O_{14}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_2
F	I/O_{15}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
G	I/O_{16}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
H	I/O_{17}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	NC
K	I/O_{18}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_6
L	I/O_{19}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_7
M	I/O_{20}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
N	I/O_{21}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
P	I/O_{22}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
R	I/O_{23}	A	NC	NC	NC	A	I/O_{11}
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Note:
1. NC pins are not connected on the die

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[2] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... .....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions[7]	–8		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}[2]	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC} I_{OUT} = 0 mA CMOS levels		185	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		30	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		25	mA

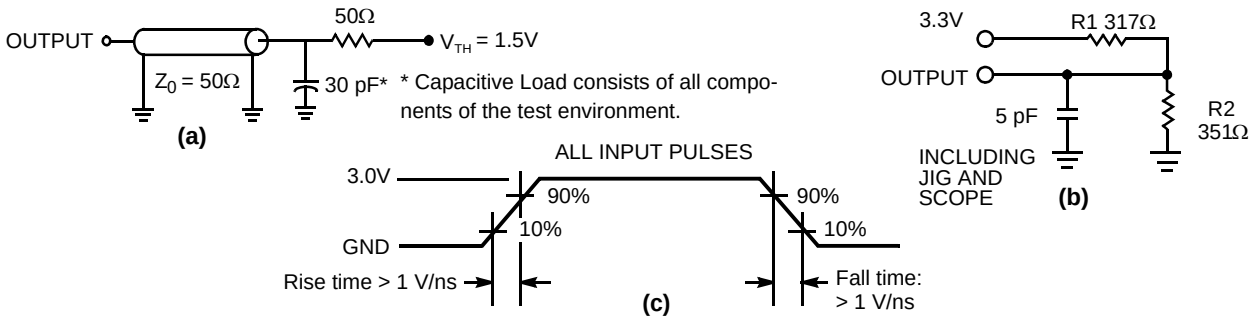
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		10	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	All - Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

AC Test Loads and Waveforms[4]



Notes:

2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.
4. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.

[+] Feedback

AC Switching Characteristics Over the Operating Range [5]

Parameter	Description	–8		Unit
		Min.	Max.	
Read Cycle				
t_{power}[6]	V_{CC}(typical) to the first access	100		µs
t_{RC}	Read Cycle Time	8		ns
t_{AA}	Address to Data Valid		8	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ active LOW to Data Valid[7]		8	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8]		5	ns
t_{LZCE}	$\overline{CE}$ active LOW to Low-Z[7, 8]	3		ns
t_{HZCE}	$\overline{CE}$ deselect HIGH to High-Z[7, 8]		5	ns
t_{PU}	$\overline{CE}$ active LOW to Power-up[7, 9]	0		ns
t_{PD}	$\overline{CE}$ deselect HIGH to Power-down[7, 9]		8	ns
t_{DBE}	Byte Enable to Data Valid		5	ns
t_{LZBE}	Byte Enable to Low-Z[8]	1		ns
t_{HZBE}	Byte Disable to High-Z[8]		5	ns
Write Cycle[10, 11]				
t_{WC}	Write Cycle Time	8		ns
t_{SCE}	$\overline{CE}$ active LOW to Write End[7]	6		ns
t_{AW}	Address Set-up to Write End	6		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		ns
t_{SD}	Data Set-up to Write End	5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8]		5	ns
t_{BW}	Byte Enable to End of Write	6		ns

Notes:

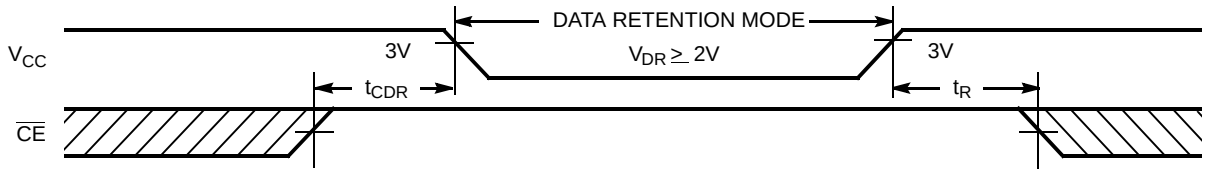
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V. Test conditions for the read cycle use output loading as shown in part a) of the AC test loads, unless specified otherwise.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
7. $\overline{CE}$ indicates a combination of all three chip enables. When active LOW, $\overline{CE}$ indicates the $\overline{CE_1}$ or $\overline{CE_2}$ or $\overline{CE_3}$ LOW. When deselect HIGH, $\overline{CE}$ indicates the $\overline{CE_1}$ and $\overline{CE_2}$ and $\overline{CE_3}$ HIGH
8. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
9. These parameters are guaranteed by design and are not tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ or $\overline{CE_2}$ or $\overline{CE_3}$ LOW and $\overline{WE}$ LOW. The chip enables must be active and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

[+] Feedback

Data Retention Characteristics (Over the Operating Range)

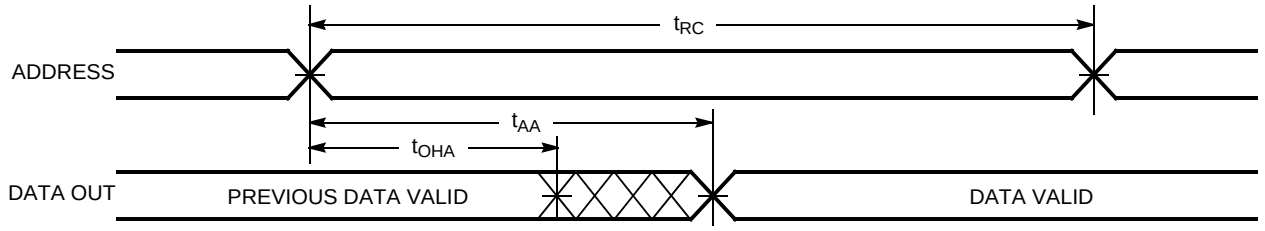
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2			V
I_{CCDR}	Data Retention Current	$V_{CC} = 2V$, $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			25	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R[12]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform

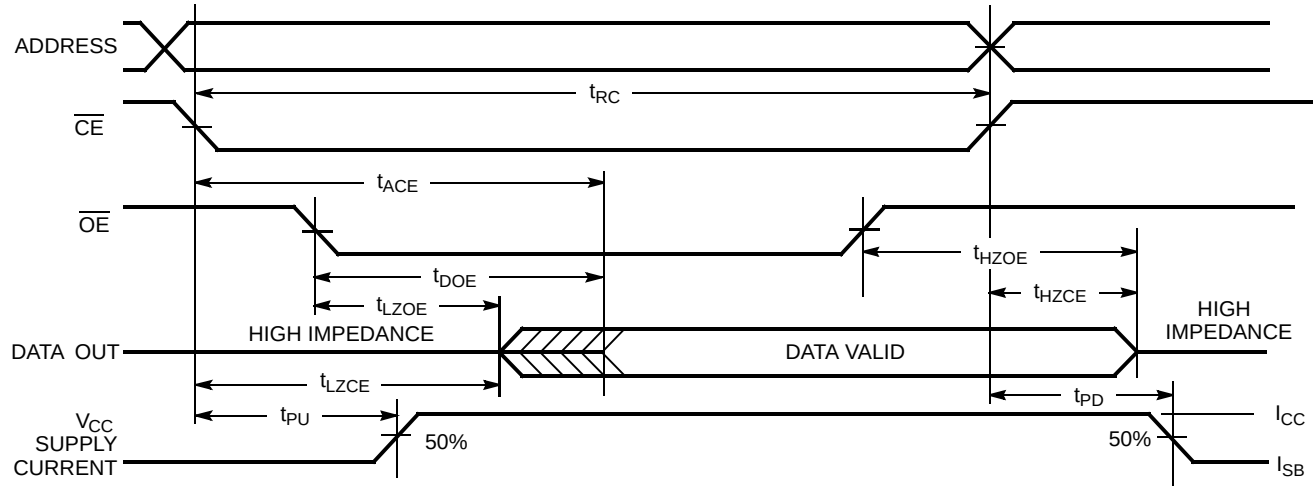


Switching Waveforms

Read Cycle No. 1[13, 14]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[7, 14, 15]

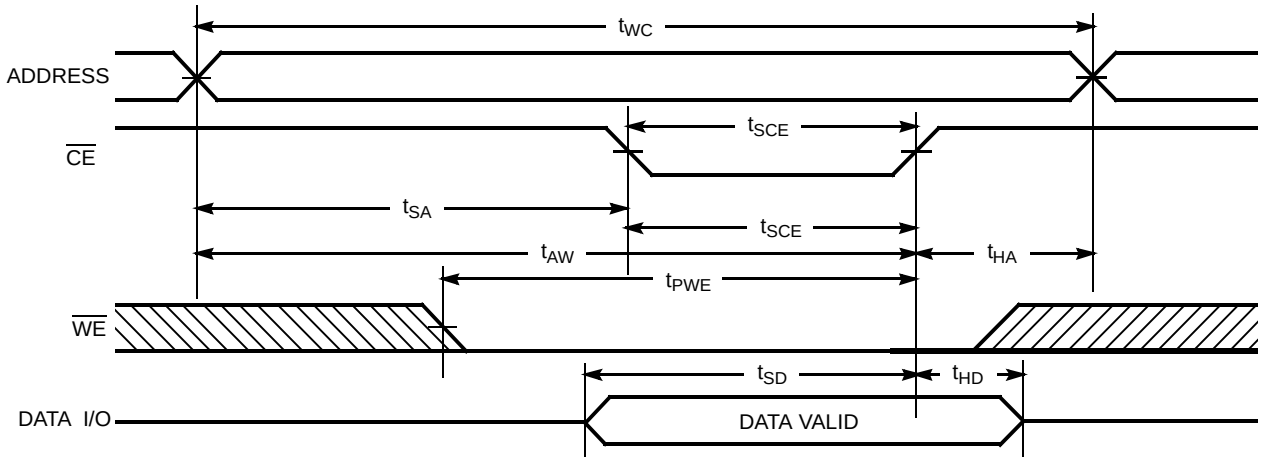


Notes:
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\,\mu s$ or stable at $V_{CC(min.)} \geq 50\,\mu s$
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

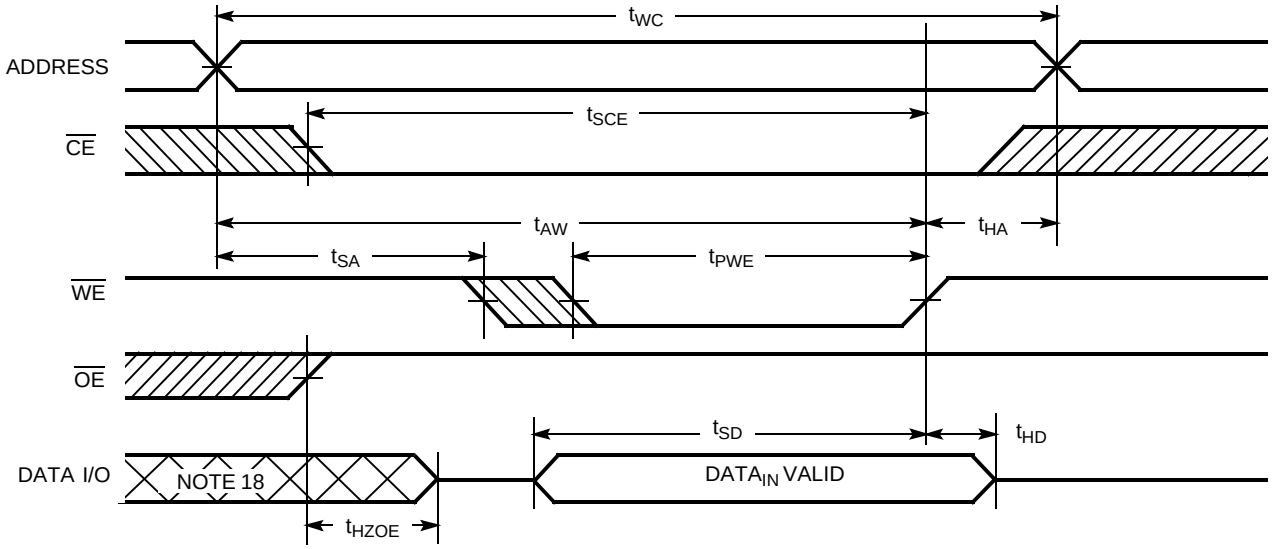
[+] Feedback

Switching Waveforms (continued)

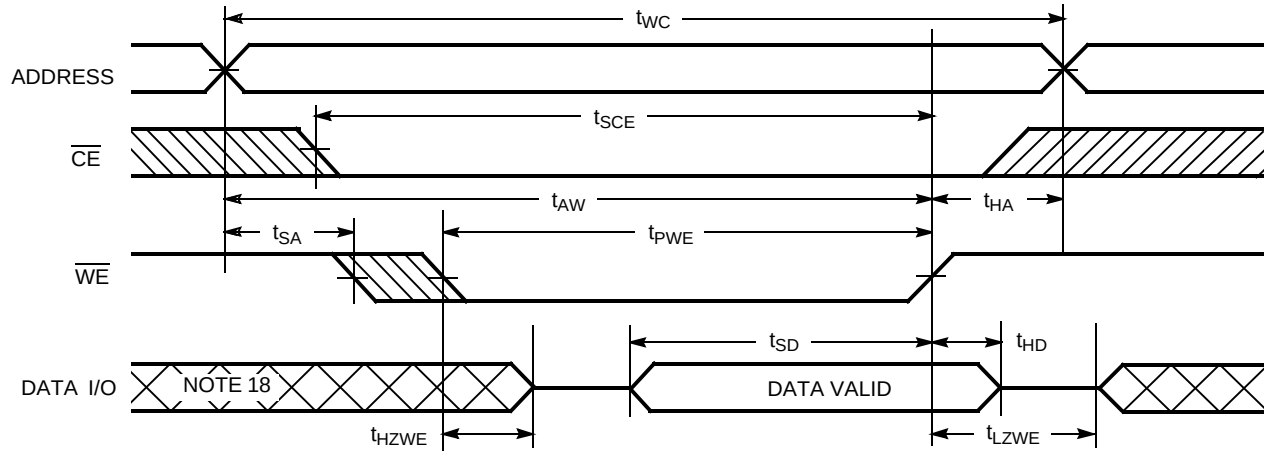
Write Cycle No. 1 ($\overline{CE}$ Controlled)[7, 16, 17]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[16, 17]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[7, 17]



Notes:
16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
18. During this period the I/Os are in the output state and input signals should not be applied.

[+] Feedback

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	I/O_{16}–I/O_{23}	Mode	Power
H	H	H	X	X	High-Z	High-Z	High-Z	Power-down	Standby (I_{SB})
L	H	H	L	H	Data Out	High-Z	High-Z	Read	Active (I_{CC})
H	L	H	L	H	High-Z	Data Out	High-Z	Read	Active (I_{CC})
H	H	L	L	H	High-Z	High-Z	Data Out	Read	Active (I_{CC})
L	L	L	L	H	Full Data Out	Full Data Out	Full Data Out	Read	Active (I_{CC})
L	H	H	X	L	Data In	High-Z	High-Z	Write	Active (I_{CC})
H	L	H	X	L	High-Z	Data In	High-Z	Write	Active (I_{CC})
H	H	L	X	L	High-Z	High-Z	Data In	Write	Active (I_{CC})
L	L	L	X	L	Full Data In	Full Data In	Full Data In	Write	Active (I_{CC})
L	L	L	H	H	High-Z	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

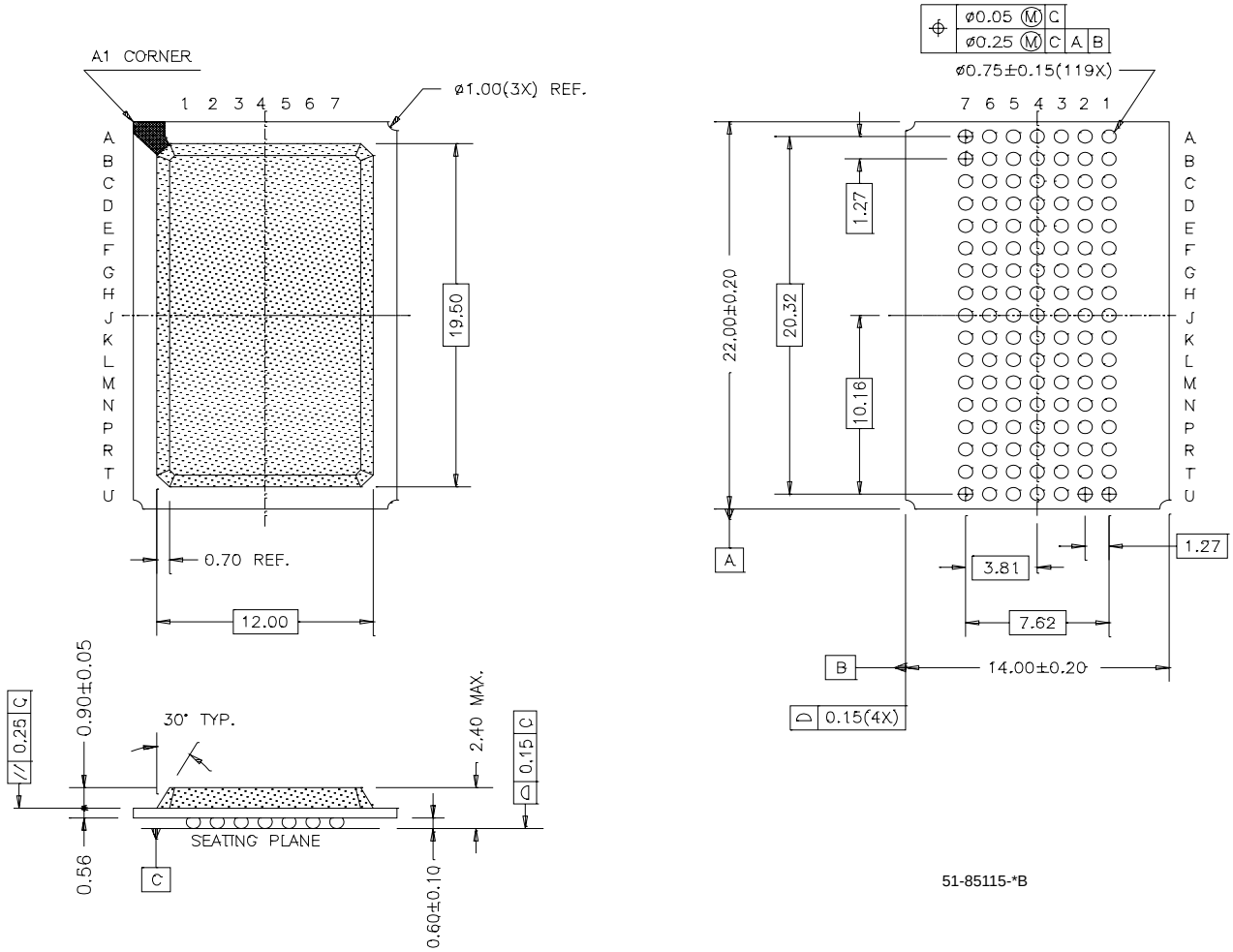
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1012DV33-8BGXC	51-85115	119-ball Plastic Ball Grid Array (14 x 22 x 2.4 mm) (Pb-free)	Commercial

[+] Feedback

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)



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Document History Page

Document Title: CY7C1012DV33 12-Mbit (512K X 24) Static RAM Document Number: 38-05610				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	250650	See ECN	SYT	New Data Sheet
*A	469517	See ECN	NXR	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed –10 and –12 speed bins from product offering Changed J7 ball of BGA from DNU to NC Removed Industrial Operating range from product offering Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page #3 Changed $I_{CC(Max)}$ from 220 mA to 150 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot spec in footnote # 1 Updated the Truth Table Updated the ordering Information table
*B	499604	See ECN	NXR	Added note# 1 for NC pins Changed I_{CC} spec from 150 mA to 185 mA Updated Test Condition for I_{CC} in DC Electrical Characteristics table Added note for t_{ACE}, t_{LZCE}, t_{HZCE}, t_{PU}, t_{PD}, t_{SCE} in AC Switching Characteristics Table on page# 4

[+] Feedback