CY22801

Universal Programmable Clock Generator (UPCG)

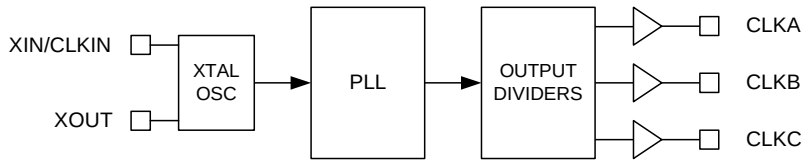
Features

- Integrated phase-locked loop (PLL)
- Field programmable
- Input frequency range:
  - — Crystal: 8–30 MHz
  - — CLKIN: 1–133 MHz
- Output frequency:
  - — LVCMOS: 1–200 MHz
- Low jitter, high accuracy outputs
- 3.3V operation
- 8-pin SOIC package

Benefits

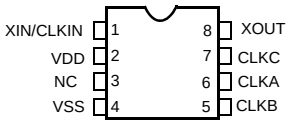
- Inventory of only one device, CY22801, is needed to use in various applications
- In-house programming of samples and prototype quantities is available using the CY36800 InstaClock Kit
- Can customize the input and output frequencies to suit your needs
- High-performance PLL tailored for multiple applications
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Logic Block Diagram



Pin Configuration

CY22801
8-pin SOIC



Pin Description

Name	Pin Number	Description
XIN	1	Reference Input: Crystal or External Clock
VDD	2	3.3V Voltage Supply
NC	3	No Connect; leave this pin floating
VSS	4	Ground
CLKB	5	Clock Output B
CLKA	6	Clock Output A
CLKC	7	Clock Output C
XOUT	8	Reference Output: Connect to external crystal. When the reference is an external clock signal, this pin is not used and must be left floating.

General Description

The CY22801 is a flash-programmable clock generator that supports various applications in consumer and communications markets. The device uses a Cypress proprietary PLL to drive up to three configurable outputs in an 8-pin SOIC.

The CY22801 can be programmed with an easy-to-use programmer dongle, the CY36800, in conjunction with the CyClocksRT™ software. This enables fast sample generation of prototype builds for user-defined frequencies.

Field Programming the CY22801

The CY22801 is programmed using the CY36800 USB programmer dongle. The CY22801 is flash-technology based, so the parts can be reprogrammed up to 100 times. This enables fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed using the CY36800 programmer. Cypress's value added distribution partners and third party programming systems from BP Microsystems, HiLo Systems, and others, are available for large production quantities.

CyClocksRT Software

CyClocksRT is an easy-to-use software application that enables the user to custom-configure the CY22801. Users can specify the XIN/CLKIN frequency, crystal load capacitance, and output frequencies. CyClocksRT then creates an industry-standard JEDEC file, which is used to program the CY22801.

When needed, an advanced mode is available that enables users to override the automatically generated VCO frequency and output divider values.

CyClocksRT is a component of the CyberClocks™ software, which can be downloaded free of charge from the Cypress website at http://www.cypress.com.

CY36800 InstaClock™ Kit

The Cypress CY36800 InstaClock Kit comes with everything needed to design the CY22801 and program samples and small prototype quantities. The CyClocksRT software is used to quickly create a JEDEC programming file, which is then downloaded directly to the portable programmer that is included in the CY36800 InstaClock Kit. The JEDEC file can also be saved for use in a production programming system for larger volumes.

The CY36800 also comes with five samples of the CY22800, which can be programmed with preconfigured JEDEC files using the InstaClock software.

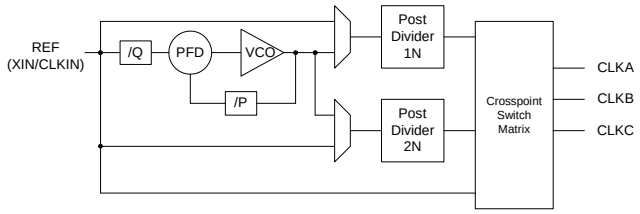
Output Clock Frequencies

The CY22801 is a very flexible clock generator with up to three individual outputs, generated from an integrated PLL. Details are shown in Figure 1.

The output of the PLL runs at high frequency and is divided down to generate the output clocks. Two programmable dividers are available for this purpose. Thus, although the output clocks may be different frequencies, they must be related, based on the PLL frequency.

It is also possible to direct the reference clock input to any of the outputs, thereby bypassing the PLL. Lastly, the reference clock may be passed through either divider.

Figure 1. Basic PLL Block Diagram



Reference Crystal Input

The input crystal oscillator of the CY22801 is an important feature because of the flexibility it allows the user in selecting a crystal as a reference clock source. The oscillator inverter has programmable gain, enabling maximum compatibility with a reference crystal, based on manufacturer, process, performance, and quality.

Input load capacitors are placed on the CY22801 die to reduce external component cost. These capacitors are true parallel-plate capacitors, designed to reduce the frequency shift that occurs when nonlinear load capacitance is affected by load, bias, supply, and temperature changes.

The value of the input load capacitors is determined by eight bits in a programmable register. Total load capacitance is determined by the formula:

$$CapLoad = (C_L - C_{BRD} - C_{CHIP})/0.09375\ pF$$

In CyClocksRT, enter the crystal capacitance (C_L). The value of CapLoad will be determined automatically and programmed into the CY22801.

Applications

Controlling Jitter

Jitter is defined in many ways, including:

- Phase noise
- Long-term jitter
- Cycle-to-cycle jitter
- Period jitter
- Absolute jitter
- Deterministic jitter

These jitter terms are usually given in terms of RMS, peak-to-peak, or in the case of phase noise, dBC/Hz with respect to the fundamental frequency. Actual jitter is dependent on

- XIN jitter and edge rate
- Number of active outputs
- Output frequencies
- Supply voltage
- Temperature
- Output load

Power supply noise and clock output loading are two major system sources of clock jitter. Power supply noise can be mitigated by proper power supply decoupling (0.1-µF ceramic cap) of the clock and ensuring a low impedance ground to the chip. Reducing capacitive clock output loading to a minimum lowers current spikes on the clock edges and thus reduces jitter.

Reducing the total number of active outputs also reduces jitter in a linear fashion. However, it is better to use two outputs to drive two loads than one output to drive two loads.

For additional information, refer to the application note, *Jitter in PLL-based Systems: Causes, Effects, and Solutions*, available at http://www.cypress.com.

Cypress Programmable Clocks

Cypress offers a wide range of programmable clock synthesizers that can generate any other frequencies not covered by the CY22801. Table 1 summarizes all Cypress programmable devices including CY22801.

Table 1. Cypress Programmable Clocks[1]

Part #	No. of PLL	Input Freq.	Output Freq.	Package	No. of Outputs	Spread Spectrum	VCXO	I^2C
CY22800	1	0.5–100	1–200	8-SOIC	up to 3	Yes	Yes	No
CY22801	1	1–133	1–200	8-SOIC	up to 3	No	No	No
CY22050	1	1–133	0.08–200	16-TSSOP	up to 6	No	No	No
CY22150	1	1–133	0.08–200	16-TSSOP	up to 6	No	No	Yes
CY25100	1	8–166	3–200	8-SOIC/TSSOP	up to 2	Yes	No	No
CY25200	1	3–166	3–200	16-TSSOP	up to 6	Yes	No	No
CY241V08	1	27/13.5	27/13.5	8-SOIC	up to 2	No	Yes	No
CY22392	3	1–166	1–200	16-TSSOP	up to 6	No	No	No
CY22381	3	1–166	1–200	8-SOIC	up to 3	No	No	No
CY22393	3	1–166	1–200	16-TSSOP	up to 6	No	No	Yes
CY22394/5	3	1–166	1–200	16-TSSOP	up to 5	No	No	No
CY22388/89/91	4	1–100	4.2–166	16/20-TSSOP, 32-QFN	up to 8	No	Yes	No

Note
1. The CY22800 and CY22801 are programmed using the programming dongle included in the CY36800 InstaClock Kit. The CY3672 programmer can be used to program all other Cypress Programmable Clocks.

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	4.6	V
T_S	Storage Temperature	–65	150	°C
T_J	Junction Temperature	–	125	°C
V_{IO}	Input and Output Voltage	V_{SS} – 0.5	V_{DD} + 0.5	V
ESD	Electro-Static Discharge Voltage per MIL-STD-833, Method 3015	2000	–	V

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance on the CLK output	–	–	15	pF
t_{PU}	Power up time for VDD to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Recommended Crystal Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, and AT cut	8	–	30	MHz
C_{LNOM}	Nominal Load Capacitance		6	–	30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	35	50	Ω
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

DC Electrical Specifications[2]

Parameter	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ (source)	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$ (sink)	12	24	–	mA
V_{IH}	Input High Voltage		$0.7*V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{SS} – 0.3$	–	$0.3*V_{DD}$	V
C_{IN1}	Input Capacitance	All input pins except XIN and XOUT	–	–	7	pF
C_{IN2}	Input Capacitance	XIN and XOUT pins	–	24	–	pF
I_{DD}[3, 4]	V_{DD} Supply Current		–	70	–	mA

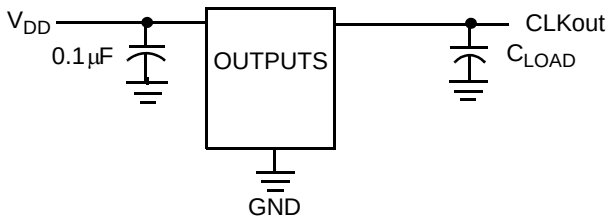
Notes
2. Not 100% tested, guaranteed by design.
3. I_{DD} current specified for three CLK outputs running at 100 MHz.
4. Use CyClocksRT™ to calculate actual I_{DD} for specific output frequency configurations.

AC Electrical Characteristics[2]

Parameter	Name	Description	Min	Typ	Max	Unit
f_{REFC}	Reference Frequency - crystal		8	–	30	MHz
f_{REFD}	Reference Frequency - driven		1	–	133	MHz
f_{OUT}	Output Frequency		1	–	200	MHz
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V_{DD}	0.8	1.4	–	V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of V_{DD}	0.8	1.4	–	V/ns
t_5[5]	Skew	Output-output skew between related outputs	–	–	250	ps
t_6[6]	Clock Jitter	Peak-to-peak period jitter	–	250	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Test Circuit

Figure 2. Test Circuit Diagram



Timing Definitions

Figure 3. Duty Cycle Definition; DC = t2/t1

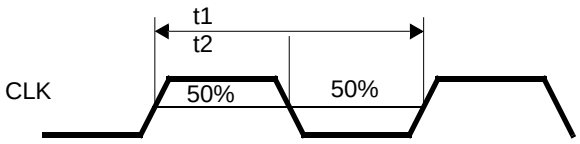
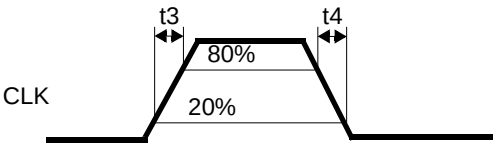


Figure 4. Rise and Fall Time Definitions



Notes

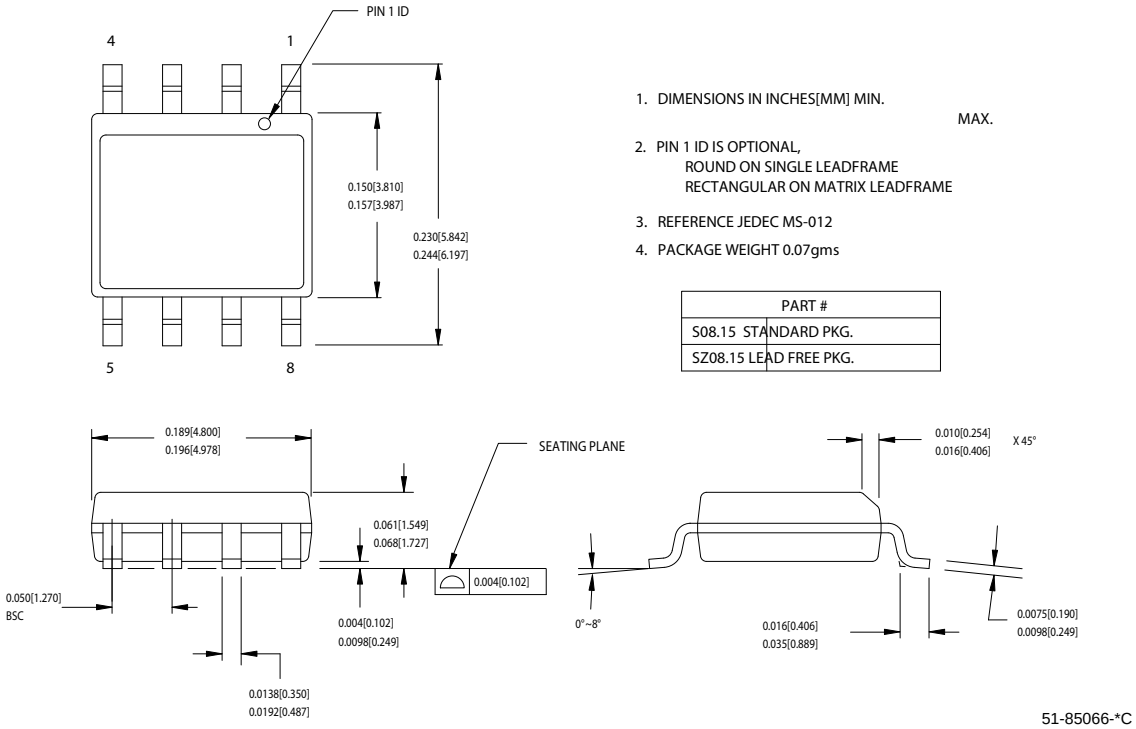
5. Skew value guaranteed when outputs are generated from the same divider bank.
6. Jitter measurement may vary. Actual jitter is dependent on input jitter and edge rate, number of active outputs, input and output frequencies, supply voltage, temperature, and output load. For more information, refer to the application note, *Jitter in PLL-based Systems: Causes, Effects, and Solutions*.

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY22801FXC	8-Pin SOIC	Commercial	3.3V

Package Diagram

Figure 5. 8-Lead (150-Mil) SOIC S8



Document History Page

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1058080	See ECN	KVM/ KKVTMP	New data sheet