

AK681024G 1,048,579 x 8 Bit CMOS Static Random Access Memory

DESCRIPTION

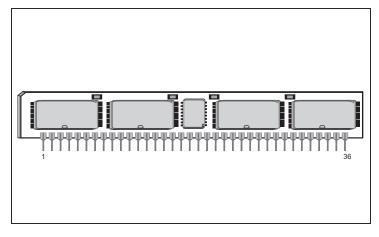
The Accutek AK681024G is a high density SRAM memory module organized in 1 Meg X 8 bit words. The assembly consists of four medium speed 128K X 8 SRAMs in thin TSOP packages, plus a CMOS decoder logic IC and four decoupling capacitor chips, mounted on the front side and four medium speed 128K x 8 SRAMS in thin TSOP packages and four decoupling capacitor chips mounted on the back side of a low-profile printed circuit board. The module configuration is a 36 pin leaded SIP.

The memory operates as a single asynchronous 1 Meg X 8 SRAM from a 5V supply, and has common I/O, chip enable, output enable and write enable functions. With the proper choice of SRAMs, it is available in three separate low-standby-power configurations, with access times of 55, 70, 85 or 100 nSEC.

The combination of low power, low profile and high density packaging offered by the AK681024G makes it ideal for use in applications where board space and available power are limited and extremely low access times are not required. It is especially useful in VMEbus designs and in places where very close module-to-module spacing is dictated.

FEATURES

- 1,048,576 x 8 bit organization
- JEDEC Standard 36 pin SIP format
- Common I/O, single OE, CE and WE functions
- Low 0.550 inch maximum seated height and thin profile allow maximum board density



- · Range of access times from 55 to 100 nSEC
- Low, low-low and ultra-low standby power level versions available
- · Single 5 volt power supply AK681024G
- Single 3.3 volt power supply AK681024G/3.3
- Operating free air temerature 0⁰C to 70⁰C (Industrial range version of -10⁰C to 85⁰C also available)
- Completely static and asynchronous, no clock or timing strobe required
- Low
 9.0 Watt Max Active
 120 μ Watt Max Standby

Low Low 9.0 Watt Max Active 80 µ Watt Standby

PIN NOMENCLATURE

	ASSI	\sim \sim		4364
PIN	A 100 TO		IVVI	- 121 1
	- 4-9 1-9 1			

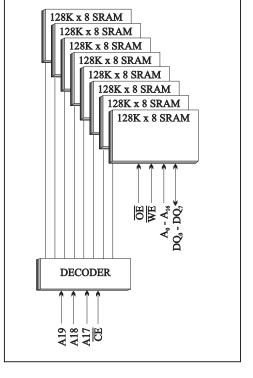
DQ ₀ - DQ ₇	Data In/Data Out
A ₀ - A ₁₉	Address Inputs
CE	Chip Enable
WE	Write Enable
ŌĒ	Output Enable
Vcc	5v Supply
Vss	Ground
NC	No Connection

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	NC	10	A ₄	19	CE	28	A ₇
2	Vcc	11	Vss	20	A ₁₅	29	A ₈
3	WE	12	DQ ₅	21	A ₁₆	30	A 9
4	DQ ₂	13	A ₁₀	22	A ₁₂	31	DQ ₇
5	DQ ₃	14	A ₁₁	23	A ₁₈	32	DQ ₄
6	DQ ₀	15	A ₅	24	A ₆	33	DQ ₆
7	A ₁	16	A ₁₃	25	DQ ₁	34	A ₁₇
8	A ₂	17	A ₁₄	26	Vss	35	Vcc
9	A ₃	18	A ₁₉	27	A ₀	36	ŌE

MODULE OPTIONS

Leaded SIP: AK681024G	

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8

1 Product

AK = Accutek Memory

2 Type

4 = Dynamic RAM

5 = CMOS Dynamic RAM

6 = Static RAM

3 Organization/Word Width

1 = by 1 16 = by 16 4 = by 4 32 = by 32

 $8 = by 8 \quad 36 = by 36$

9 = by 9

4 Size/Bits Depth

5 Package Type

G = Single In-Line Package (SIP)

S = Single In-Line Module (SIM)

D = Dual In-Line Package (DIP)

W = .050 inch Pitch Edge Connect

Z = Zig-Zag In-Line Package (ZIP)

Special Designation

P = Page Mode

N = Nibble Mode

K = Static Column Mode

W = Write Per Bit Mode

V = Video Ram

7 Separator

- = Commercial 0°C to +70°C

M = Military Equivalent Screened

(-55⁰C to +125⁰C)

I = Industrial Temperature Tested

 $(-45^{\circ}C \text{ to } +85^{\circ}C)$

X = Burned In

8 Speed (first two significant digits)

DRAMS SRAMS

60 = 60 nS 12 = 12 nS 70 = 70 nS 20 = 20 nS 80 = 80 nS 25 = 25 nS

 $10 = 100 \, \text{nS} \quad 35 = 35 \, \text{nS}$

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accutek if other information is required.

EXPAMPLES:

AK681024G-70LL

1 Meg x 8, 70 nSEC Low Low Power SRAM Module, SIP Configuration



ACCUTEK MICROCIRCUIT CORPORATION

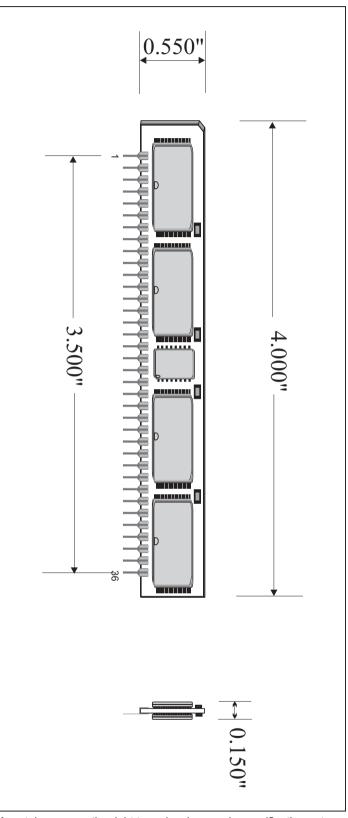
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MECHANICAL DIMENSIONS

Inches



Accutek reserves the right to make changes in specifications at any time and without notice. Accutek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.