TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

TC74LCX16244FT

Low-Voltage 16-Bit Bus Buffer with 5-V Tolerant Inputs and Outputs

The TC74LCX16244FT is a high-performance CMOS 16-bit bus buffer. Designed for use in 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (2.5-V or 3.3-V) V_{CC} applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

This device is non-inverting 3-state buffer having four active-low output enables. It can be used as four 4-bit buffers two 8-bit buffers or one 16-bit buffer. When the $\overline{OE}$ input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

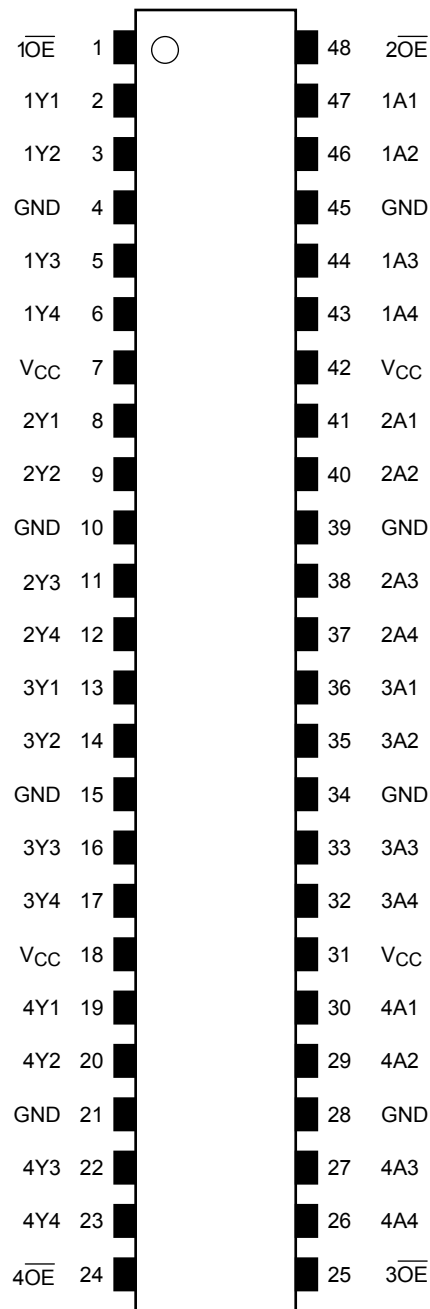All inputs are equipped with protection circuits against static discharge.

TSSOP48-P-0061-0.50A
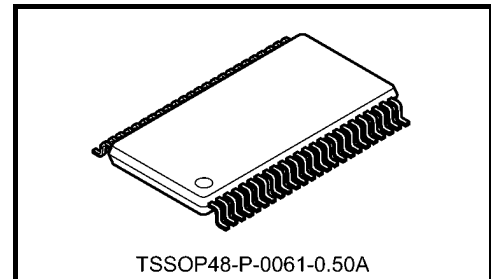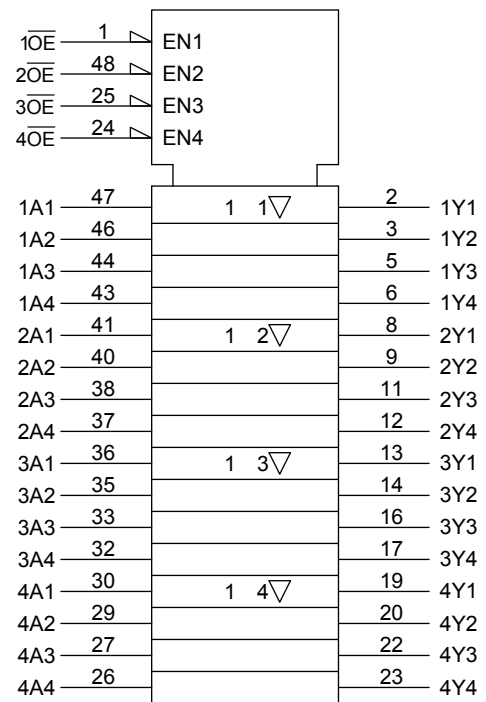
Weight: 0.25 g (typ.)

Features

- Low-voltage operation: V_{CC} = 2.0 to 3.6 V
- High-speed operation: t_{pd} = 4.5 ns (max) (V_{CC} = 3.0 to 3.6 V)
- Output current: $|I_{OH}|/I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: −500 mA
- Package: TSSOP
- Power-down protection provided on all inputs and outputs

Pin Assignment (top view)

1$\overline{OE}$	1		48	2$\overline{OE}$
1Y1	2		47	1A1
1Y2	3		46	1A2
GND	4		45	GND
1Y3	5		44	1A3
1Y4	6		43	1A4
V$_{CC}$	7		42	V$_{CC}$
2Y1	8		41	2A1
2Y2	9		40	2A2
GND	10		39	GND
2Y3	11		38	2A3
2Y4	12		37	2A4
3Y1	13		36	3A1
3Y2	14		35	3A2
GND	15		34	GND
3Y3	16		33	3A3
3Y4	17		32	3A4
V$_{CC}$	18		31	V$_{CC}$
4Y1	19		30	4A1
4Y2	20		29	4A2
GND	21		28	GND
4Y3	22		27	4A3
4Y4	23		26	4A4
4$\overline{OE}$	24		25	3$\overline{OE}$

IEC Logic Symbol

1$\overline{OE}$	1	EN1	
2$\overline{OE}$	48	EN2	
3$\overline{OE}$	25	EN3	
4$\overline{OE}$	24	EN4	

1A1	47	1 1▽	2	1Y1
1A2	46		3	1Y2
1A3	44		5	1Y3
1A4	43		6	1Y4
2A1	41	1 2▽	8	2Y1
2A2	40		9	2Y2
2A3	38		11	2Y3
2A4	37		12	2Y4
3A1	36	1 3▽	13	3Y1
3A2	35		14	3Y2
3A3	33		16	3Y3
3A4	32		17	3Y4
4A1	30	1 4▽	19	4Y1
4A2	29		20	4Y2
4A3	27		22	4Y3
4A4	26		23	4Y4

Truth Table

Inputs		Outputs
1$\overline{\text{OE}}$	1A1-1A4	1Y1-1Y4
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
2$\overline{\text{OE}}$	2A1-2A4	2Y1-2Y4
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
3$\overline{\text{OE}}$	3A1-3A4	3Y1-3Y4
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
4$\overline{\text{OE}}$	4A1-4A4	4Y1-4Y4
L	L	L
L	H	H
H	X	Z

X: Don't care

Z: High impedance

System Diagram
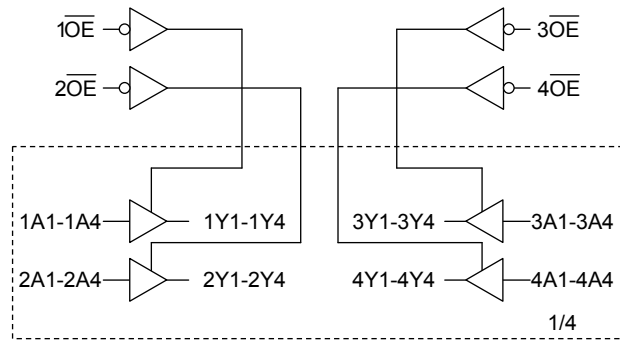
Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 6.0	V
Input voltage	V_{IN}	−0.5 to 7.0	V
Output voltage	V_{OUT}	−0.5 to 7.0 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 3)	V
		0 to V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	±24 (Note 5)	mA
		±12 (Note 6)	
		±8 (Note 7)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: Output in OFF state

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.7 to 3.0 V

Note 7: V_{CC} = 2.3 to 2.7 V

Note 8: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C)

Characteristics		Symbol	Test Condition		V$_{CC}$ (V)	Min	Max	Unit
Input voltage	H-level	V$_{IH}$	—		2.3 to 2.7	1.7	—	V
					2.7 to 3.6	2.0	—	
	L-level	V$_{IL}$	—		2.3 to 2.7	—	0.7	
					2.7 to 3.6	—	0.8	
Output voltage	H-level	V$_{OH}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −100 μA	2.3 to 3.6	V$_{CC}$ −0.2	—	V
				I$_{OH}$ = −8 mA	2.3	1.8	—	
				I$_{OH}$ = −12 mA	2.7	2.2	—	
				I$_{OH}$ = −18 mA	3.0	2.4	—	
				I$_{OH}$ = −24 mA	3.0	2.2	—	
	L-level	V$_{OL}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OL}$ = 100 μA	2.3 to 3.6	—	0.2	
				I$_{OL}$ = 8 mA	2.3	—	0.6	
				I$_{OL}$ = 12 mA	2.7	—	0.4	
				I$_{OL}$ = 16 mA	3.0	—	0.4	
				I$_{OL}$ = 24 mA	3.0	—	0.55	
Input leakage current		I$_{IN}$	V$_{IN}$ = 0 to 5.5 V		2.3 to 3.6	—	±5.0	μA
3-state output off-state current		I$_{OZ}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$ V$_{OUT}$ = 0 to 5.5 V		2.3 to 3.6	—	±5.0	μA
Power off leakage current		I$_{OFF}$	V$_{IN}$/V$_{OUT}$ = 5.5 V		0	—	10.0	μA
Quiescent supply current		I$_{CC}$	V$_{IN}$ = V$_{CC}$ or GND		2.3 to 3.6	—	20.0	μA
			V$_{IN}$/V$_{OUT}$ = 3.6 to 5.5 V		2.3 to 3.6	—	±20.0	
Increase in Icc per input		ΔI$_{CC}$	V$_{IH}$ = V$_{CC}$ − 0.6 V		2.3 to 3.6	—	500	

AC Characteristics (Ta = −40 to 85°C)

Characteristics	Symbol	Test Condition	V$_{CC}$ (V)	C$_L$(pF)	Min	Max	Unit
Propagation delay time	t$_{pLH}$ t$_{pHL}$	Figure 1, Figure 2	2.5 ± 0.2	30	1.5	5.4	ns
			2.7	50	1.5	5.2	
			3.3 ± 0.3	50	1.5	4.5	
3-state output enable time	t$_{pZL}$ t$_{pZH}$	Figure 1, Figure 3	2.5 ± 0.2	30	1.5	7.2	ns
			2.7	50	1.5	6.3	
			3.3 ± 0.3	50	1.5	5.5	
3-state output disable time	t$_{pLZ}$ t$_{pHZ}$	Figure 1, Figure 3	2.5 ± 0.2	30	1.5	6.5	ns
			2.7	50	1.5	5.7	
			3.3 ± 0.3	50	1.5	5.4	
Output to output skew	t$_{osLH}$ t$_{osHL}$	(Note)	2.5 ± 0.2	30	—	—	ns
			2.7	50	—	—	
			3.3 ± 0.3	50	—	1.0	

Note: Parameter guaranteed by design.
(t$_{osLH}$ = |t$_{pLHm}$ − t$_{pLHn}$|, t$_{osHL}$ = |t$_{pHLm}$ − t$_{pHLn}$|)

Dynamic Switching Characteristics
(Ta = 25°C, input: t_r = t_f = 2.5 ns, R_L = 500 Ω)

Characteristics		Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic	V_{OL}	V_{OLP}	V_{IH} = 2.5 V, V_{IL} = 0 V, C_L =30pF	2.5	0.6	V
			V_{IH} = 3.3 V, V_{IL} = 0 V, C_L =50pF	3.3	0.8	
Quiet output minimum dynamic	V_{OL}	$|V_{OLV}|$	V_{IH} = 2.5 V, V_{IL} = 0 V, C_L =30pF	2.5	0.6	V
			V_{IH} = 3.3 V, V_{IL} = 0 V, C_L =50pF	3.3	0.8	

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	7	pF
Output capacitance	C_{OUT}	—	3.3	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	3.3	25	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

AC Test Circuit
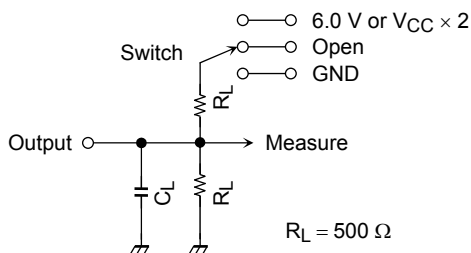
Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V
t_{pHZ}, t_{pZH}	GND	

Figure 1

AC Waveform
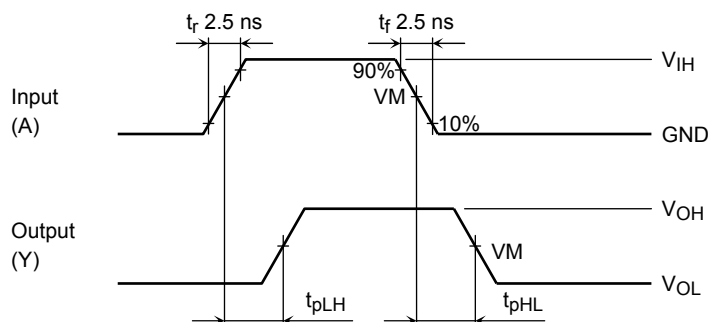
Figure 2 t_{pLH}, t_{pHL}
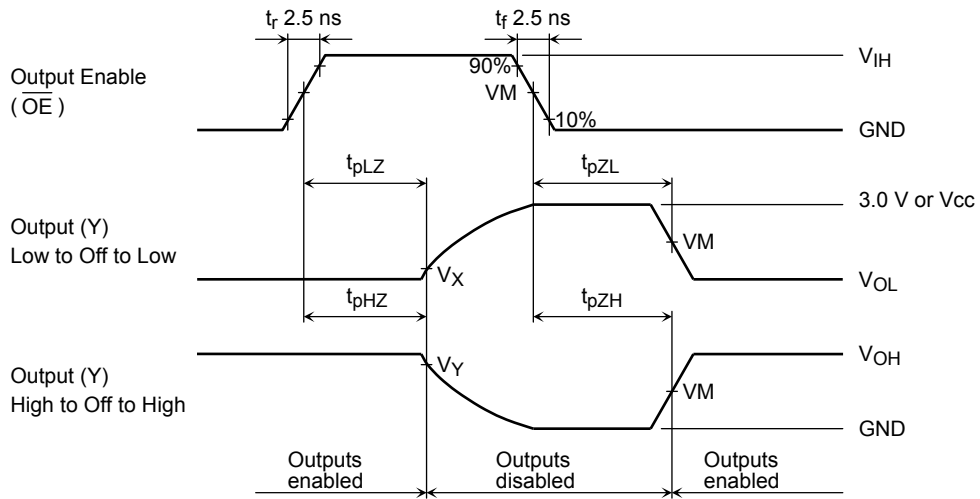
Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.7 V	2.5 ± 0.2 V
V_{IH}	2.7 V	2.7 V	V_{CC}
V_M	1.5 V	1.5 V	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V

Package Dimensions

TSSOP48-P-0061-0.50A   Unit: mm
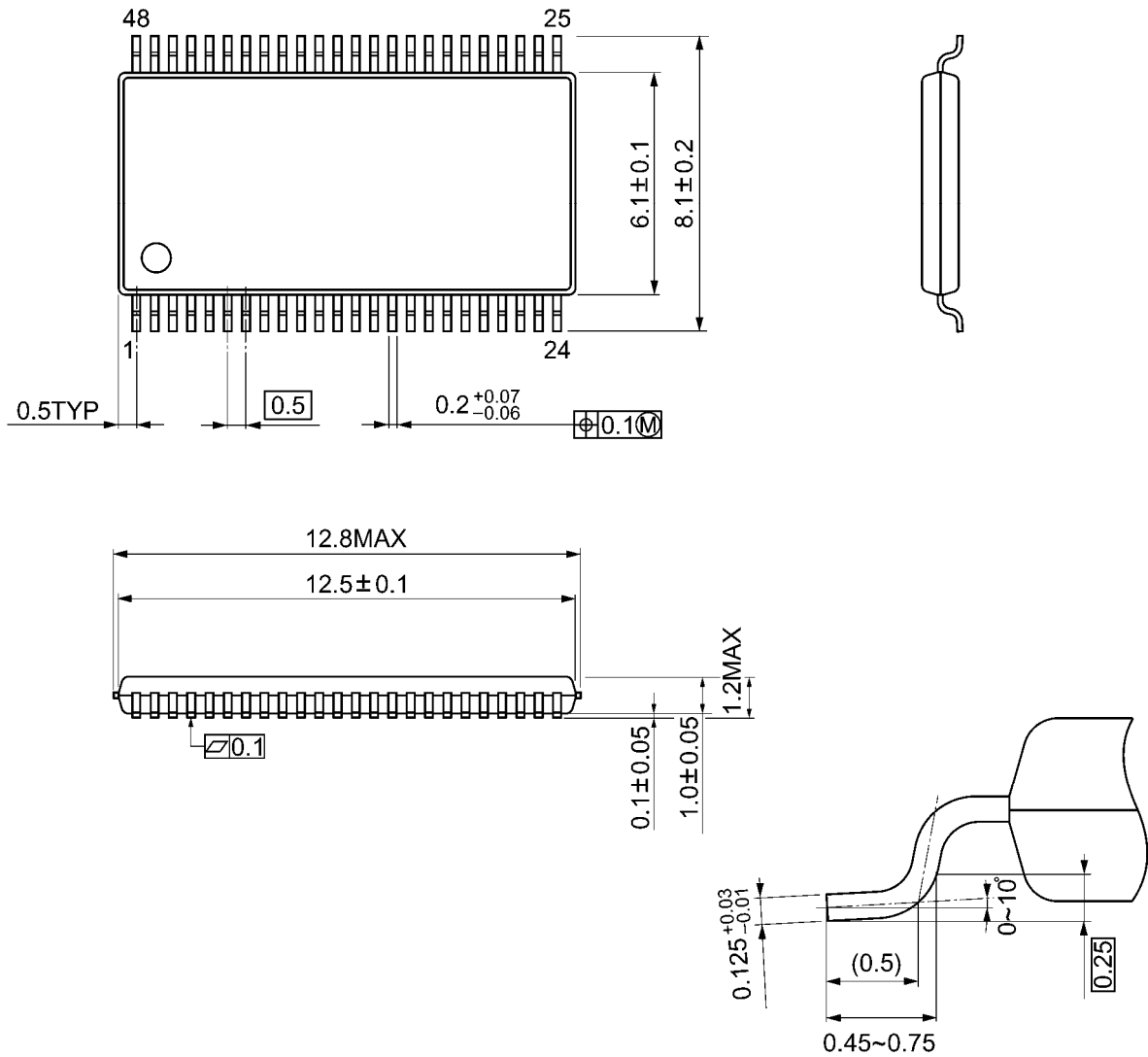
Weight: 0.25 g (typ.)

RESTRICTIONS ON PRODUCT USE