



STD90N4F3

STP90N4F3 - STU90N4F3

N-channel 40V - 5.4mΩ - 80A - DPAK - TO-220 - IPAK
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD90N4F3	40V	<6.5mΩ	80A	110W
STP90N4F3	40V	<6.5mΩ	80A	110W
STU90N4F3	40V	<6.5mΩ	80A	110W

- Standard threshold drive
- 100% avalanche tested

Applications

- Switching application

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics unique "single feature size" strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

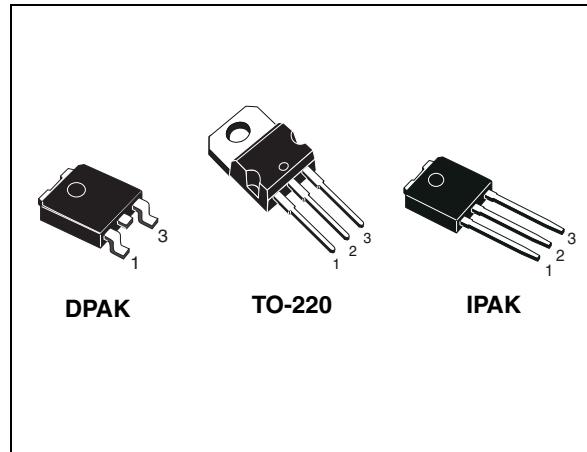


Figure 1. Internal schematic diagram

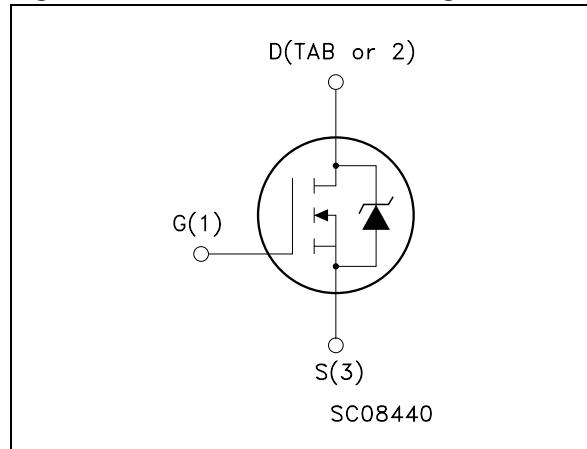


Table 1. Device summary

Order code	Marking	Package	Packaging
STD90N4F3	90N4F3	DPAK	Tape & reel
STP90N4F3	90N4F3	TO-220	Tube
STU90N4F3	90N4F3	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	65	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.73	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	8	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	400	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80 \text{ A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DS} \leq V_{(\text{BR})DSS}$, $T_j \leq T_{j\max}$
4. Starting $T_j = 25^\circ\text{C}$, $I_D = 40\text{A}$, $V_{DD} = 30\text{V}$

Table 3. Thermal resistance

Symbol	Parameter	Value			Unit
		TO-220	IPAK	DPAK	
$R_{thj\text{-case}}$	Thermal resistance junction-case max	1.36		$^\circ\text{C/W}$	
$R_{thj\text{-a}}$	Thermal resistance junction-ambient max	62.5	100	--	$^\circ\text{C/W}$
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-ambient max	--	--	50	$^\circ\text{C/W}$
T_I	Maximum lead temperature for soldering purpose	300	275	--	$^\circ\text{C}$

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}, V_{DS} = \text{Max rating}, T_c = 125^{\circ}\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 200	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$		5.4	6.5	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25 \text{ V}, I_D = 40 \text{ A}$		100		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		2200 580 40		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20 \text{ V}, I_D = 80 \text{ A}$ $V_{GS} = 10 \text{ V}$ <i>(see Figure 14)</i>		40 11 8	54	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=20\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)		15 50		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=20\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 16)		40 15		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=80\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=80\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=30\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 15)		45 60 2.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

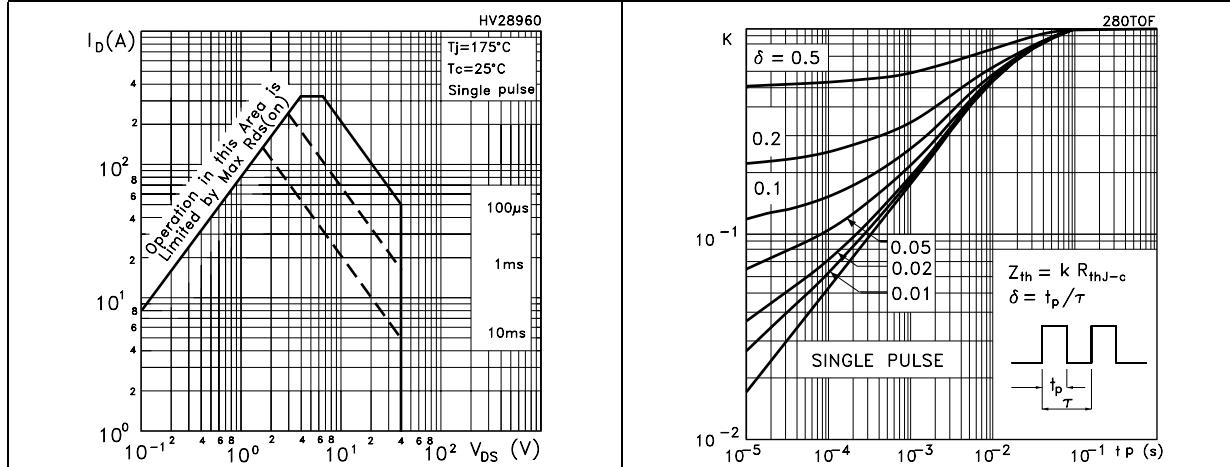


Figure 4. Output characteristics

Figure 5. Transfer characteristics

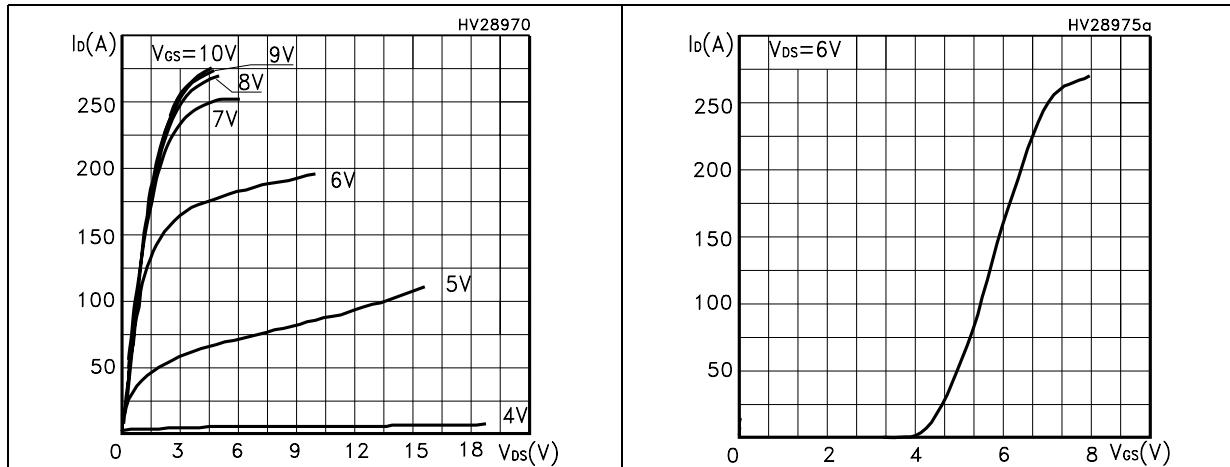


Figure 6. Static drain-source on resistance

Figure 7. Normalized BVDSS vs temperature

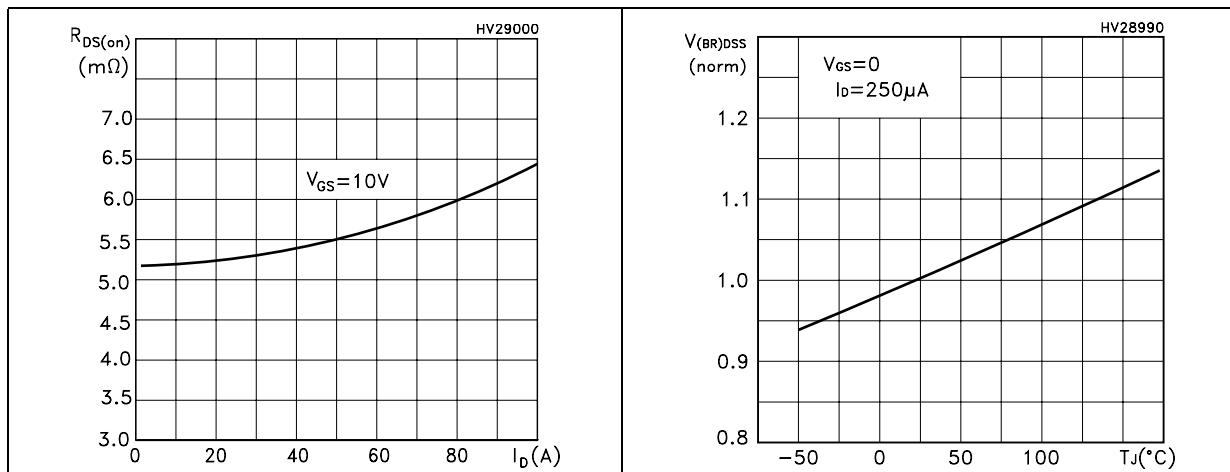
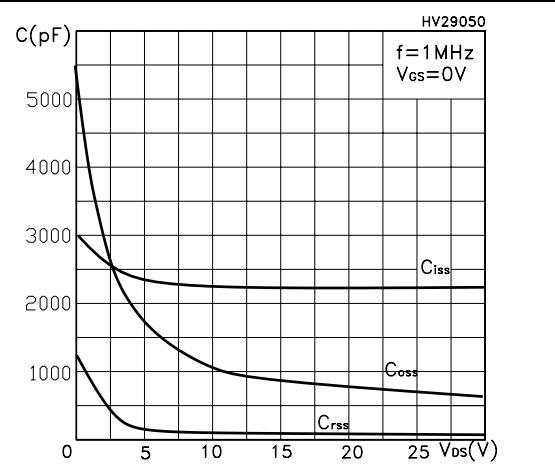
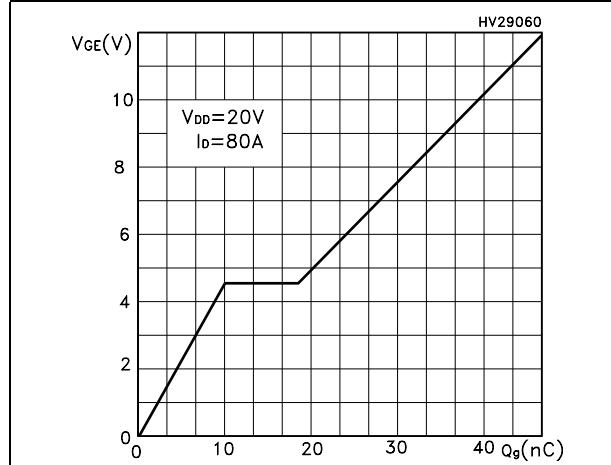
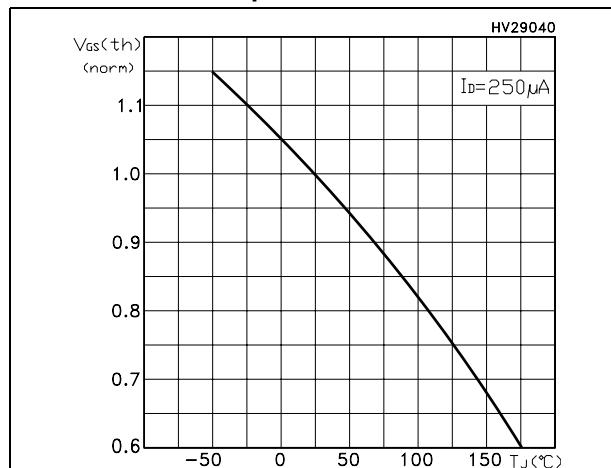
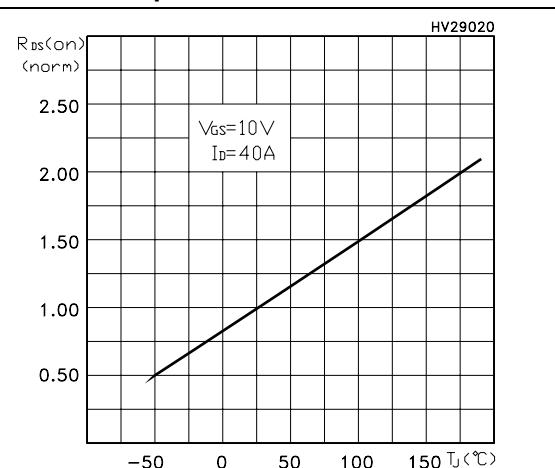
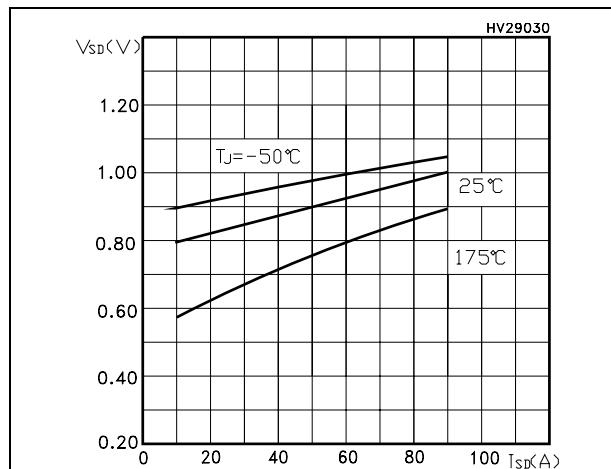


Figure 8. Gate charge vs gate-source voltage**Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics**

3 Test circuit

Figure 13. Switching times test circuit for resistive load

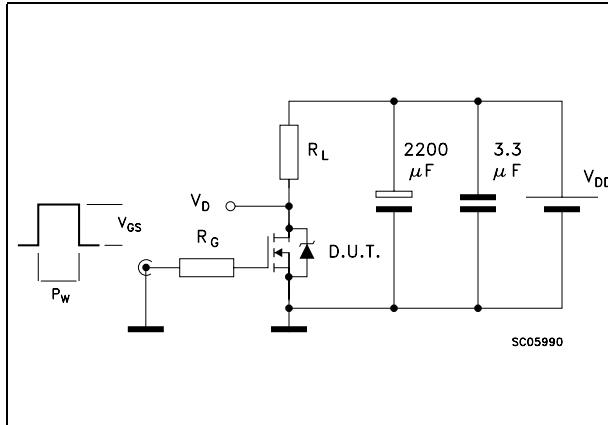


Figure 14. Gate charge test circuit

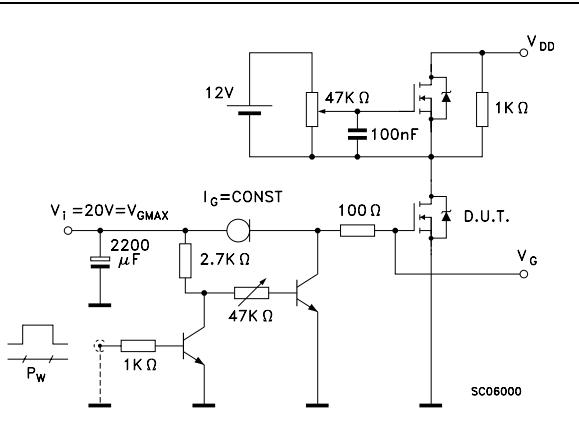


Figure 15. Test circuit for inductive load switching and diode recovery times

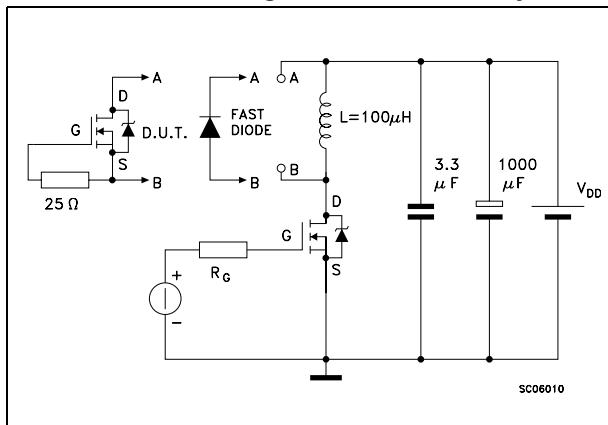


Figure 16. Unclamped Inductive load test circuit

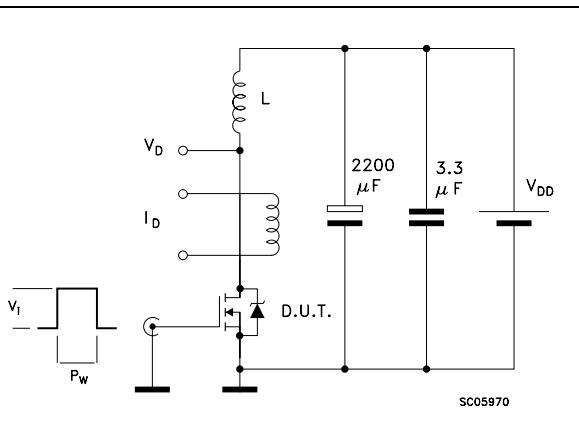


Figure 17. Unclamped inductive waveform

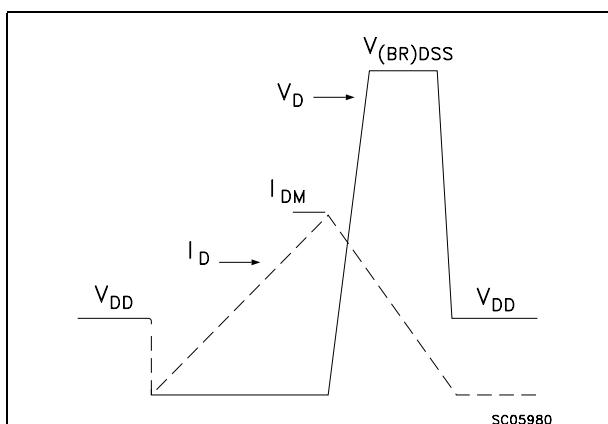
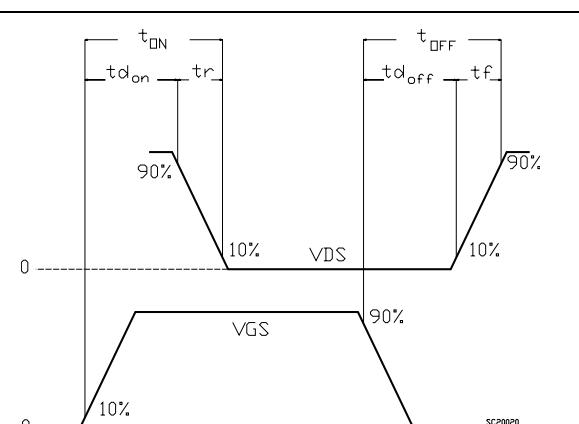


Figure 18. Switching time waveform

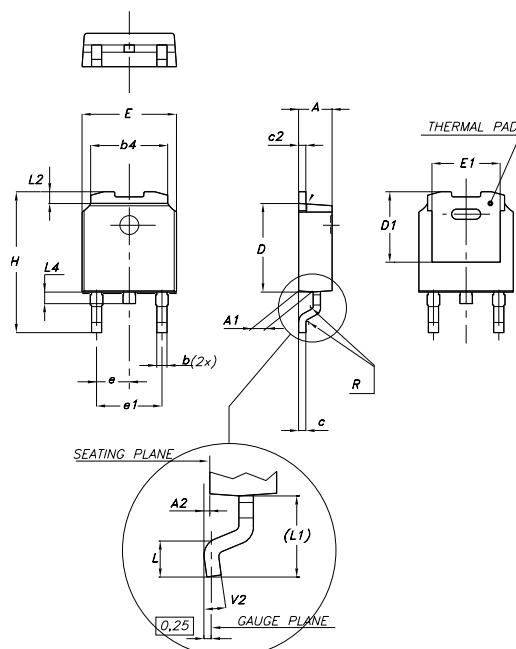


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

DPAK MECHANICAL DATA

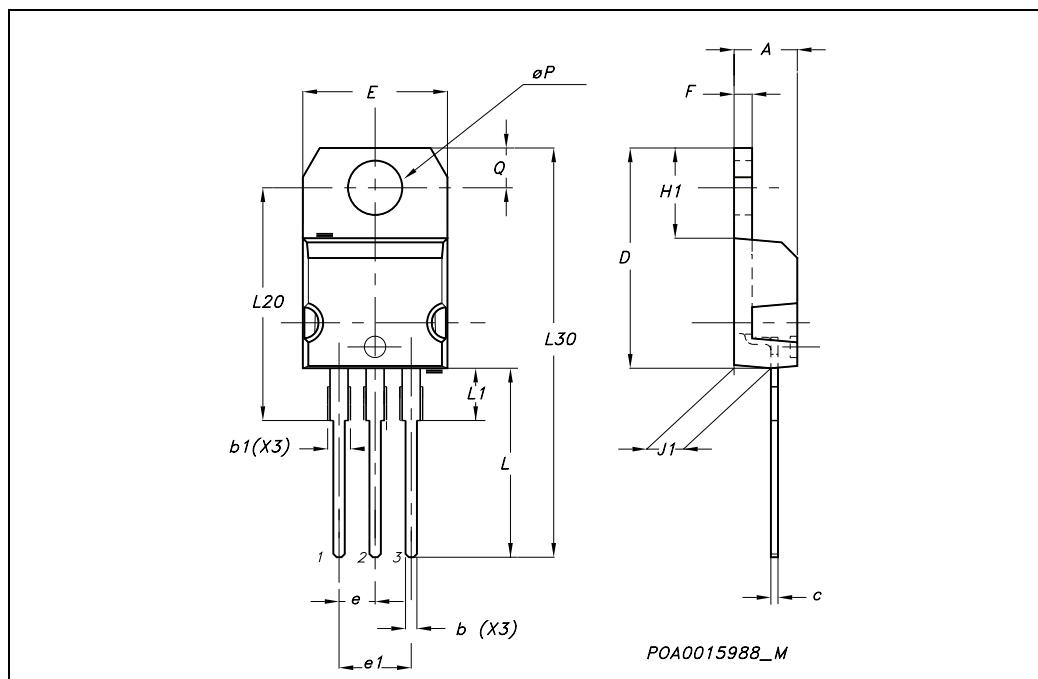
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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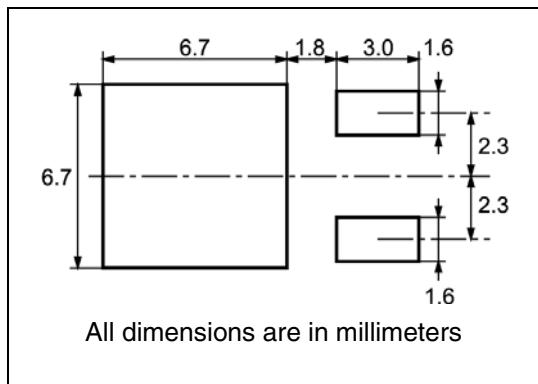
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ϕP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

BASE QTY **BULK QTY**

2500	2500
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For machine ref. only including draft and radii concentric around B0

User Direction of Feed

FEED DIRECTION →

Bending radius R min.

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
29-Nov-2007	1	First release

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