

8-bit Microcontrollers

CMOS

F²MC-8FX MB95130MB Series

MB95136MB/F133MBS/F133NBS/F133JBS/F134MBS/F134NBS/F134JBS/
MB95F136MBS/F136NBS/F136JBS/F133MBW/F133NBW/F133JBW/F134MBW/
MB95F134NBW/F134JBW/F136MBW/F136NBW/F136JBW/FV100D-103

■ DESCRIPTION

The MB95130MB series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8FX CPU core
 - Instruction set optimized for controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operations
 - Bit test branch instruction
 - Bit manipulation instructions etc.
- Clock
 - Main clock
 - Main PLL clock
 - Sub clock (for dual clock product)
 - Sub PLL clock (for dual clock product)

(Continued)

Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

MB95130MB Series

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- Timer
 - 8/16-bit compound timer × 1 channel
 - 8/16-bit PPG × 1 channel
 - 16-bit PPG × 1 channel
 - Timebase timer × 1 channel
 - Watch prescaler (for dual clock product) × 1 channel
- LIN-UART × 1 channel
 - LIN function, Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
 - Full duplex double buffer
- UART/SIO × 1 channel
 - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
 - Full duplex double buffer
- External interrupt × 8 channels
 - Interrupt by edge detection (rising, falling, or both edges can be selected)
 - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 8 channels
 - 8-bit or 10-bit resolution can be selected.
- Low-power consumption (standby) mode
 - Stop mode
 - Sleep mode
 - Watch mode (for dual clock product)
 - Timebase timer mode
- I/O port
 - The number of maximum ports
 - Single clock product : 20 ports
 - Dual clock product : 18 ports
 - Configuration
 - General-purpose I/O ports (COMS) : Single clock product : 20 ports
Dual clock product : 18 ports
- Programmable input voltage levels of port
Automotive input level / CMOS input level / hysteresis input level
- Flash memory security function
Protects the content of Flash memory (Flash memory device only)

MB95130MB Series

■ MEMORY LINEUP

| | Flash memory | RAM |
|-----------------------------|--------------|-----------|
| MB95F133MBS/F133NBS/F133JBS | 8 Kbytes | 256 bytes |
| MB95F133MBW/F133NBW/F133JBW | | |
| MB95F134MBS/F134NBS/F134JBS | 16 Kbytes | 512 bytes |
| MB95F134MBW/F134NBW/F134JBW | | |
| MB95F136MBS/F136NBS/F136JBS | 32 Kbytes | 1 Kbyte |
| MB95F136MBW/F136NBW/F136JBW | | |

MB95130MB Series

■ PRODUCT LINEUP

| Part number | MB95136MB | MB95 F133MBS/ F134MBS/ F136MBS | MB95 F133NBS/ F134NBS/ F136NBS | MB95 F133MBW/ F134MBW/ F136MBW | MB95 F133NBW/ F134NBW/ F136NBW | MB95 F133JBS/ F134JBS/ F136JBS | MB95 F133JBW/ F134JBW/ F136JBW |
|-------------------------------------|---|---|---|---|---|---|---|
| Type | MASK ROM product | Flash memory product | | | | | |
| ROM capacity*1 | 32 Kbytes (Max) | | | | | | |
| RAM capacity*1 | 1 Kbyte (Max) | | | | | | |
| Reset output | Yes | | | | | No | |
| Option*2 | Clock system | Selectable single/dual clock*3 | Single clock | | Dual clock | | Single clock Dual clock |
| | Low voltage detection reset | Yes/No | No | Yes | No | Yes | |
| | Clock supervisor | Yes/No | No | | | | Yes |
| CPU functions | Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 μs (at machine clock frequency 16.25 MHz) | | | | | | |
| Peripheral functions | General-purpose I/O port | <ul style="list-style-type: none"> • Single clock product : 20 ports • Dual clock product : 18 ports Programmable input voltage levels of port : Automotive input level / CMOS input level / hysteresis input level | | | | | |
| | Timebase timer (1 channel) | Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz) | | | | | |
| | Watchdog timer | Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Min 250 ms | | | | | |
| | Wild register | Capable of replacing 3 bytes of ROM data | | | | | |
| | UART/SIO (1 channel) | Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable | | | | | |
| | LIN-UART (1 channel) | Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave. | | | | | |
| 8/10-bit A/D converter (8 channels) | 8-bit or 10-bit resolution can be selected. | | | | | | |

(Continued)

MB95130MB Series

(Continued)

| Part number | MB95136MB | MB95 F133MBS/ F134MBS/ F136MBS | MB95 F133NBS/ F134NBS/ F136NBS | MB95 F133MBW/ F134MBW/ F136MBW | MB95 F133NBW/ F134NBW/ F136NBW | MB95 F133JBS/ F134JBS/ F136JBS | MB95 F133JBW/ F134JBW/ F136JBW |
|----------------------|--|---|---|---|---|---|---|
| Parameter | | | | | | | |
| Peripheral functions | 8/16-bit compound timer (1 channel) | Each channel of the timer can be used as “8-bit timer x 2 channels” or “16-bit timer x 1 channel”. Built-in timer function, PWC function, PWM function, capture function and square wave-form output Count clock: 7 internal clocks and external clock can be selected. | | | | | |
| | 16-bit PPG (1 channel) | PWM mode or one-shot mode can be selected. Counter operating clock: Eight selectable clock sources Support for external trigger start | | | | | |
| | 8/16-bit PPG (1 channel) | Each channel of the PPG can be used as “8-bit PPG x 2 channels” or “16-bit PPG x 1 channel”. Counter operating clock: Eight selectable clock sources | | | | | |
| | Watch counter (for dual clock product) (1 channel) | Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60) | | | | | |
| | Watch prescaler (for dual clock product) (1 channel) | Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s) | | | | | |
| | External interrupt (8 channels) | Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes. | | | | | |
| Flash memory | Supports automatic programming, Embedded Algorithm™*4 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB95F136MBS/F136NBS/F136JBS/F136MBW/F136NBW/F136JBW) | | | | | | |
| Standby mode | Sleep, stop, watch (for dual clock product), and timebase timer | | | | | | |

*1 : For ROM capacity and RAM capacity, refer to “■ MEMORY LINEUP”.

*2 : For details of option, refer to “■ MASK OPTION”.

*3 : Specify clock mode when ordering MASK ROM.

*4 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

Note : Part number of evaluation product in MB95130MB series is MB95FV100D-103.
When using it, the MCU board (MB2146-303A) is required.

MB95130MB Series

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown below.

| Oscillation stabilization wait time | Remarks |
|-------------------------------------|---|
| $(2^{14}-2) / F_{CH}$ | Approx. 4.10 ms (at main oscillation clock 4 MHz) |

■ PACKAGES AND CORRESPONDING PRODUCTS

| Part number Package | MB95136MB | MB95F133MBS MB95F133NBS MB95F134MBS MB95F134NBS MB95F136MBS MB95F136NBS MB95F133JBS MB95F134JBS MB95F136JBS | MB95F133MBW MB95F133NBW MB95F134MBW MB95F134NBW MB95F136MBW MB95F136NBW MB95F133JBW MB95F134JBW MB95F136JBW | MB95FV100D-103 |
|------------------------|-----------|---|---|----------------|
| FPT-28P-M17 | ○ | ○ | ○ | × |
| FPT-30P-M02 | ○ | ○ | ○ | × |
| BGA-224P-M08 | × | × | × | ○ |

- : Available
 × : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

- Notes on using evaluation products

The Evaluation product has not only the functions of the MB95130MB series but also those of other products to support software development for multiple series and models of the F²MC-8FX. The I/O addresses for peripheral resources not used by the MB95130MB series are therefore access-barred. Read/write access to those access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to an odd-numbered-byte address in the prohibited areas (If such access is used, the address may be read or written unexpectedly) .

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the flash memory and mask ROM products, do not use these values in the software processing.

The Evaluation product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. No particular precautions are required to the flash memory and mask ROM products, as they have the identical read/write operation to the evaluation products.

- Difference of memory spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

- Current consumption

- The current consumption of Flash memory product is greater than for MASK ROM product.

- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

- Package

For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

- Operating voltage

The operating voltage is different among the Evaluation, Flash memory, and MASK ROM products.

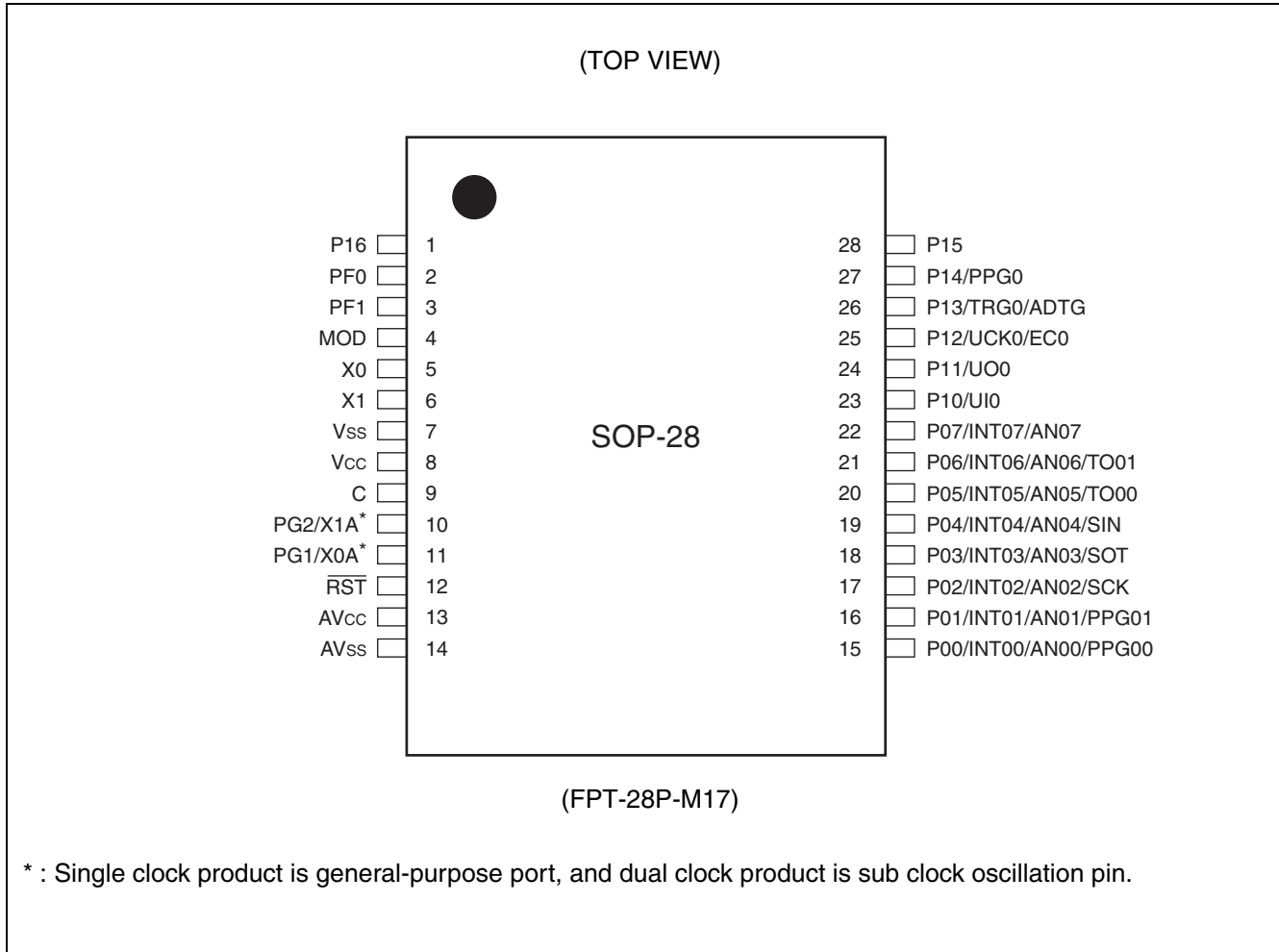
For details of the operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

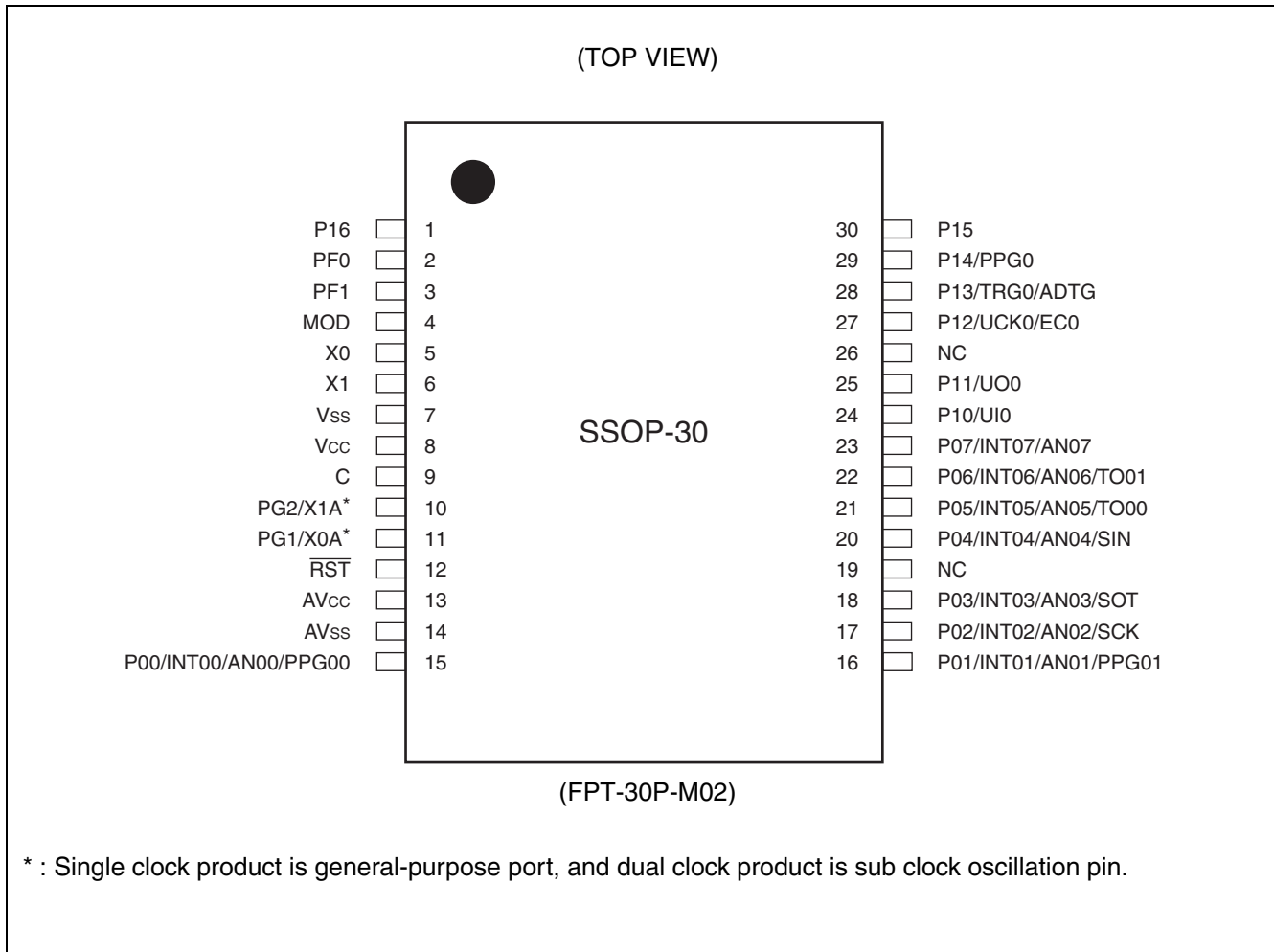
- Difference MOD Pins

A pull-down resistor is provided for the MOD pin of the MASK ROM product.

MB95130MB Series

■ PIN ASSIGNMENT





MB95130MB Series

■ PIN DESCRIPTION

| Pin no. | | Pin name | I/O circuit type*3 | Function |
|---------|-------|------------------------------|--------------------|---|
| SSOP*1 | SOP*2 | | | |
| 1 | 1 | P16 | H | General-purpose I/O port |
| 2 | 2 | PF0 | K | General-purpose I/O port for large current |
| 3 | 3 | PF1 | | |
| 4 | 4 | MOD | B | Operating mode designation pin |
| 5 | 5 | X0 | A | Main clock oscillation input pin |
| 6 | 6 | X1 | | Main clock oscillation input/output pin |
| 7 | 7 | V _{SS} | — | Power supply pin (GND) |
| 8 | 8 | V _{CC} | — | Power supply pin |
| 9 | 9 | C | — | Capacity connection pin |
| 10 | 10 | PG2/X1A | H/A | Single clock product is general-purpose port (PG2) . Dual clock product is sub clock input/output oscillation pin (32 kHz) . |
| 11 | 11 | PG1/X0A | | Single clock product is general-purpose port (PG1) . Dual clock product is sub clock input oscillation pin (32 kHz) . |
| 12 | 12 | RST | B' | Reset pin |
| 13 | 13 | AV _{CC} | — | A/D converter power supply pin |
| 14 | 14 | AV _{SS} | — | A/D converter power supply pin (GND) |
| 15 | 15 | P00/INT00/ AN00/ PPG00 | D | General-purpose I/O port Shared with external interrupt input (INT00), A/D converter analog input (AN00) and 8/16-bit PPG ch.0 output (PPG00). |
| 16 | 16 | P01/INT01/ AN01/ PPG01 | | General-purpose I/O port Shared with external interrupt input (INT01), A/D converter analog input (AN01) and 8/16-bit PPG ch.0 output (PPG01). |
| 17 | 17 | P02/INT02/ AN02/SCK | | General-purpose I/O port Shared with external interrupt input (INT02), A/D converter analog input (AN02) and LIN-UART clock I/O (SCK). |
| 18 | 18 | P03/INT03/ AN03/SOT | | General-purpose I/O port Shared with external interrupt input (INT03), A/D converter analog input (AN03) and LIN-UART data output (SOT). |
| 20 | 19 | P04/INT04/ AN04/SIN | E | General-purpose I/O port Shared with external interrupt input (INT04), A/D converter analog input (AN04) and LIN-UART data input (SIN). |
| 21 | 20 | P05/INT05/ AN05/TO00 | D | General-purpose I/O port Shared with external interrupt input (INT05 & INT06), A/D converter analog input (AN05 & AN06) and 8/16-bit compound timer ch.0 output (TO00 & TO01). |
| 22 | 21 | P06/INT06/ AN06/TO01 | | |
| 23 | 22 | P07/INT07/ AN07 | | General-purpose I/O port Shared with external interrupt input (INT07) and A/D converter analog input (AN07). |

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MB95130MB Series

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| Pin no. | | Pin name | I/O circuit type*3 | Function |
|---------|-------|-------------------|--------------------|---|
| SSOP*1 | SOP*2 | | | |
| 24 | 23 | P10/UIO | G | General-purpose I/O port Shared with UART/SIO ch.0 data input (UI0) |
| 25 | 24 | P11/UO0 | H | General-purpose I/O port Shared with UART/SIO ch.0 data output (UO0) |
| 27 | 25 | P12/UCK0/ EC0 | | General-purpose I/O port Shared with UART/SIO ch.0 clock I/O (UCK0) and 8/16-bit compound timer ch.0 clock input (EC0) |
| 28 | 26 | P13/TRG0/ ADTG | | General-purpose I/O port Shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG) |
| 29 | 27 | P14/PPG0 | | General-purpose I/O port Shared with 16-bit PPG ch.0 output (PPG0) |
| 30 | 28 | P15 | | General-purpose I/O port |
| 19,26 | — | NC | — | Internally connected pins. Be sure to leave it open. |

*1 : FPT-30P-M02

*2 : FPT-28P-M17

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

MB95130MB Series

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|---|
| A | | <ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • Low-speed side Feedback resistance: approx. 10 MΩ |
| B | | <ul style="list-style-type: none"> • Only for input • Hysteresis input only for MASK ROM product • Pull-down resistor available only to MASK ROM product |
| B' | | <ul style="list-style-type: none"> • Hysteresis input only for MASK ROM product • Reset output |
| D | | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Analog input • Pull-up control available • Automotive input |

(Continued)

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| Type | Circuit | Remarks |
|------|--|--|
| E | <p>The circuit for Type E features a pull-up resistor R connected to a P-channel MOSFET (P-ch). The gate of this P-ch MOSFET is controlled by a 'Pull-up control' signal. The drain of the P-ch MOSFET is connected to the output node, which also serves as the 'Digital output'. An N-channel MOSFET (N-ch) is connected between the output node and ground, with its gate controlled by another 'Digital output' signal. The output node is also connected to an 'Analog input'. The circuit includes several control inputs: 'A/D control', 'Standby control', and 'External interrupt control', which are connected to various logic gates (AND and OR) that control the gates of the P-ch and N-ch MOSFETs. Additionally, there are inputs for 'CMOS input', 'Hysteresis input', and 'Automotive input'.</p> | <ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input • Analog input • Pull-up control available • Automotive input |
| G | <p>The circuit for Type G is similar to Type E but lacks the 'Analog input' and 'A/D control' inputs. It features a pull-up resistor R, a P-channel MOSFET (P-ch) controlled by 'Pull-up control', and an N-channel MOSFET (N-ch) controlled by a 'Digital output' signal. The output node is labeled 'Digital output'. Control inputs include 'Standby control', 'CMOS input', 'Hysteresis input', and 'Automotive input', which are connected to logic gates controlling the MOSFET gates.</p> | <ul style="list-style-type: none"> • CMOS output • CMOS input • Hysteresis input • Pull-up control available • Automotive input |
| H | <p>The circuit for Type H is similar to Type G but lacks the 'CMOS input' input. It features a pull-up resistor R, a P-channel MOSFET (P-ch) controlled by 'Pull-up control', and an N-channel MOSFET (N-ch) controlled by a 'Digital output' signal. The output node is labeled 'Digital output'. Control inputs include 'Standby control', 'Hysteresis input', and 'Automotive input', which are connected to logic gates controlling the MOSFET gates.</p> | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available • Automotive input |
| K | <p>The circuit for Type K is the simplest, featuring a pull-up resistor R, a P-channel MOSFET (P-ch) controlled by a 'Digital output' signal, and an N-channel MOSFET (N-ch) controlled by another 'Digital output' signal. The output node is labeled 'Digital output'. Control inputs include 'Standby control', 'Hysteresis input', and 'Automotive input', which are connected to logic gates controlling the MOSFET gates.</p> | <ul style="list-style-type: none"> • CMOS output • Hysteresis input • Automotive input |

MB95130MB Series

■ HANDLING DEVICES

- Preventing latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when the devices are used.

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if voltage higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

- Stable supply voltage

Supply voltage should be stabilized.

A sudden change in power supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power supply voltage.

For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50 / 60 Hz) not to exceed 10% of the standard V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

- Precautions for use of external clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from the sub clock mode or stop mode.

PIN CONNECTION

- Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k Ω .

Any unused input/output pins may be set to the output mode and left open, or set to the input mode and treated the same as unused input pins. If there is any unused output pin, make it open.

- Treatment of power supply pins on A/D converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 μ F ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

- Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, all the pins must be connected to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μ F between V_{CC} and V_{SS} pins near this device.

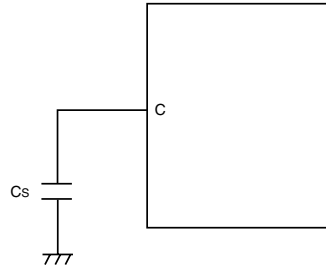
- Mode pin (MOD)

Connect the mode pin directly to V_{CC} or V_{SS} pins.

To prevent the device unintentionally entering the test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_s . For connection of smoothing capacitor C_s , refer to the diagram below.

- C Pin Connection Diagram



- Analog power supply

Always set the same potential to AV_{CC} and V_{CC} . When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

- NC pins

Any pins marked "NC"(not connected) must be left open.

MB95130MB Series

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported parallel programmers and adapters

The following table lists supported parallel programmers and adapters.

| Package | Applicable adapter model | Parallel programmers |
|-------------|--------------------------|--|
| FPT-28P-M17 | TEF110-95F136HSPF | AF9708 (Since Rev 02.43E) AF9709/B (Since Rev 02.43E) |
| FPT-30P-M02 | TEF110-95F136MB | |

Note : For information about applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector configuration

The following table shows sector-specific addresses for data access by CPU and by the parallel programmer.

• MB95F136MBS/F136NBS/F136MBW/F136NBW/F136JBS/F136JBW (32 Kbytes)

| Flash memory | CPU address | Programmer address* |
|--------------|-------------------|---------------------|
| 32 Kbytes | 8000 _H | 18000 _H |
| | FFFF _H | 1FFFF _H |

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• Programming method

- 1) Set the type code of the parallel programmer to "17237".
- 2) Load program data to programmer addresses 18000_H to 1FFFF_H.
- 3) Write data with the parallel programmer.

• MB95F134MBS/F134NBS/F134JBS/F134MBW/F134NBW/F134JBW (16 Kbytes)

| Flash memory | CPU address | Programmer address* |
|--------------|-------------------|---------------------|
| 16 Kbytes | C000 _H | 1C000 _H |
| | FFFF _H | 1FFFF _H |

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• Programming method

- 1) Set the type code of the parallel programmer to "17237".
- 2) Load program data to programmer addresses 1C000_H to 1FFFF_H.
- 3) Write data with the parallel programmer.

- MB95F133MBS/F133NBS/F133JBS/F133MBW/F133NBW/F133JBW (8 Kbytes)

| Flash memory | CPU address | Programmer address* |
|--------------|-------------------|---------------------|
| 8 Kbytes | E000 _H | 1E000 _H |
| | FFFF _H | 1FFFF _H |

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.

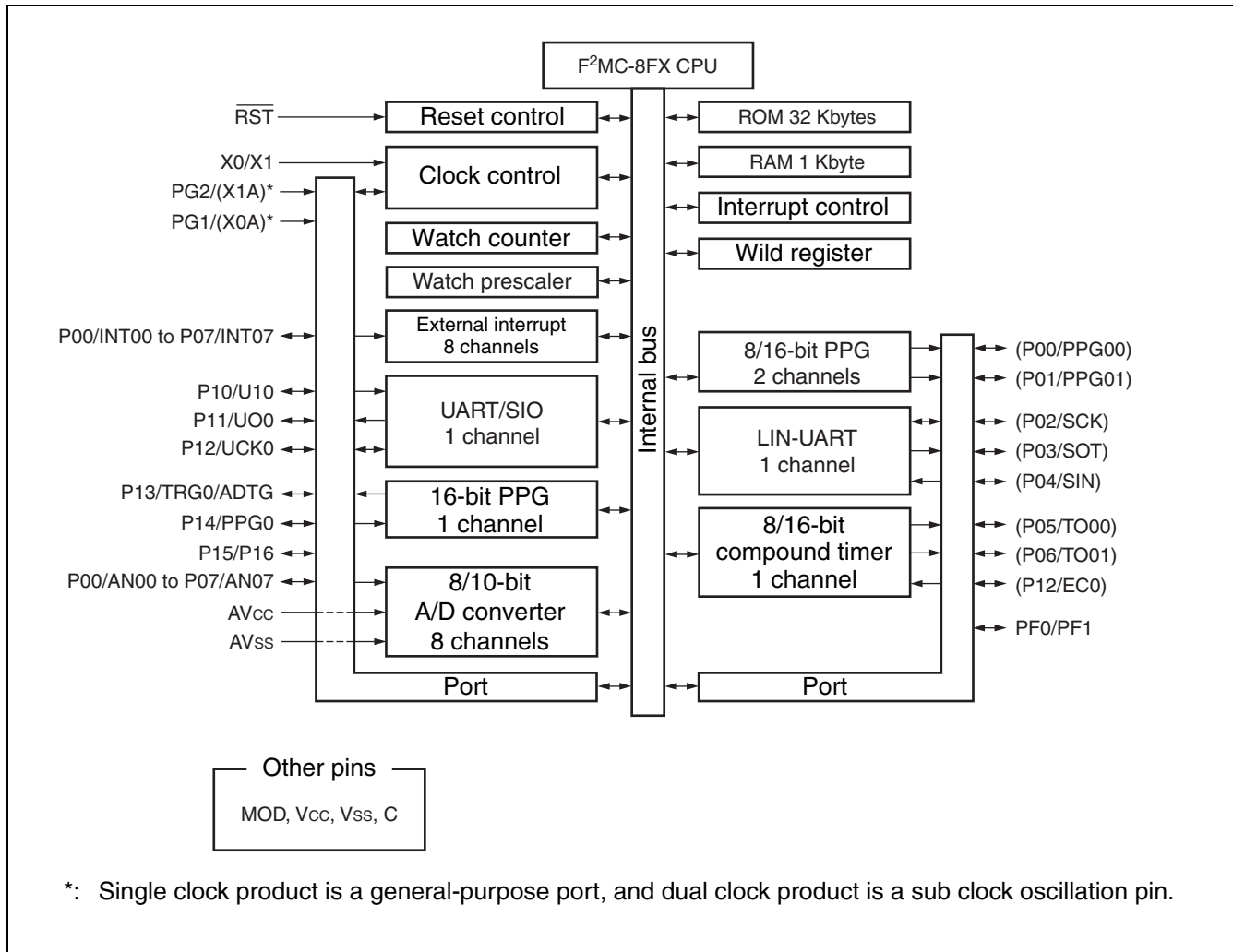
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

- **Programming method**

- 1) Set the type code of the parallel programmer to "17237".
- 2) Load program data to programmer addresses 1E000_H to 1FFFF_H.
- 3) Write data with the parallel programmer.

MB95130MB Series

■ BLOCK DIAGRAM

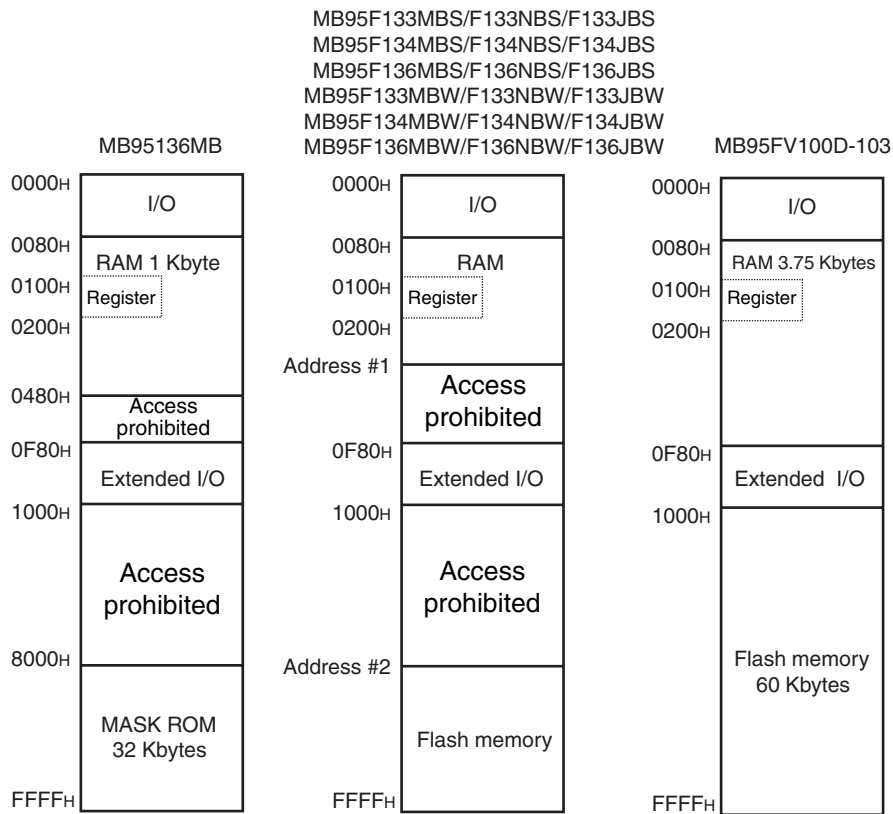


■ CPU CORE

1. Memory Space

Memory space of the MB95130MB series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95130MB series is shown below.

• Memory Map



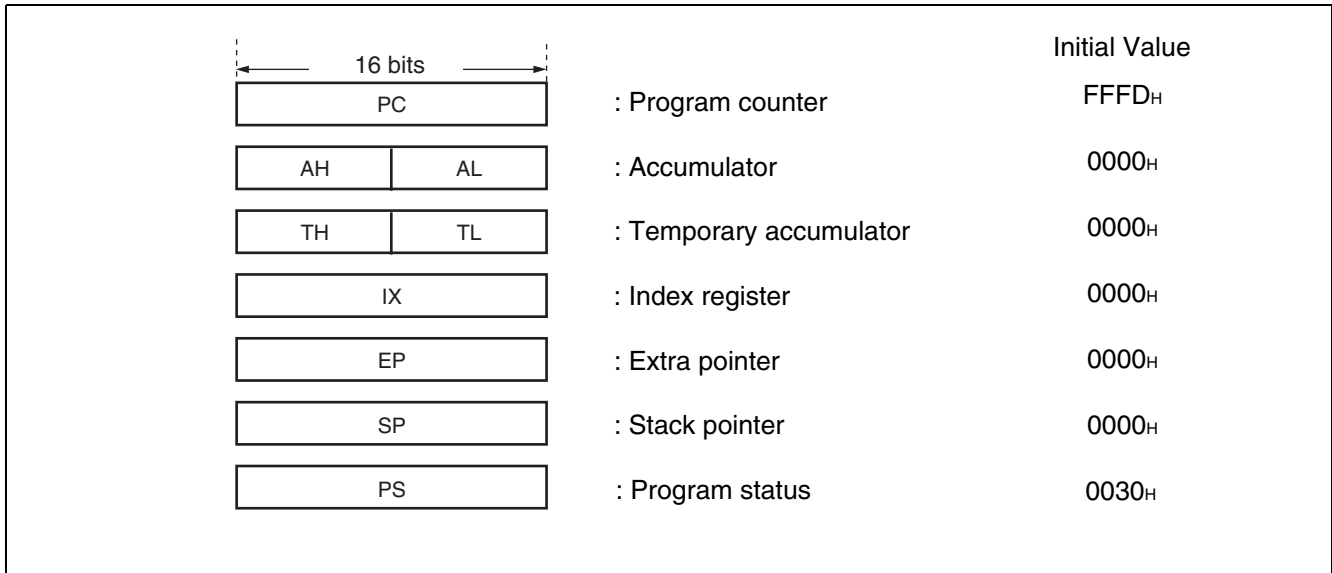
| | Flash memory | RAM | Address #1 | Address #2 |
|-----------------------------|--------------|-----------|-------------------|-------------------|
| MB95F133MBS/F133NBS/F133JBS | 8 Kbytes | 256 bytes | 0180 _H | E000 _H |
| MB95F133MBW/F133NBW/F133JBW | | | | |
| MB95F134MBS/F134NBS/F134JBS | 16 Kbytes | 512 bytes | 0280 _H | C000 _H |
| MB95F134MBW/F134NBW/F134JBW | | | | |
| MB95F136MBS/F136NBS/F136JBS | 32 Kbytes | 1 Kbyte | 0480 _H | 8000 _H |
| MB95F136MBW/F136NBW/F136JBW | | | | |

MB95130MB Series

2. Register

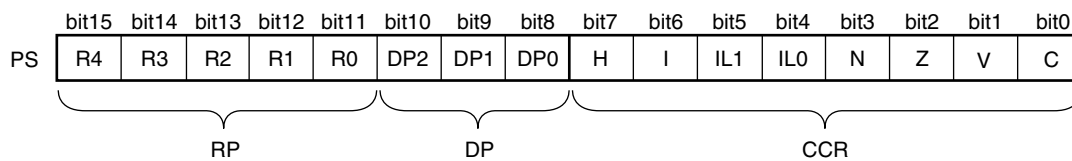
The MB95130MB series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as include:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.
- Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1-byte is used.
- Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1-byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer to point to a memory address.
- Stack pointer (SP) : A 16-bit register to indicate a stack area.
- Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register

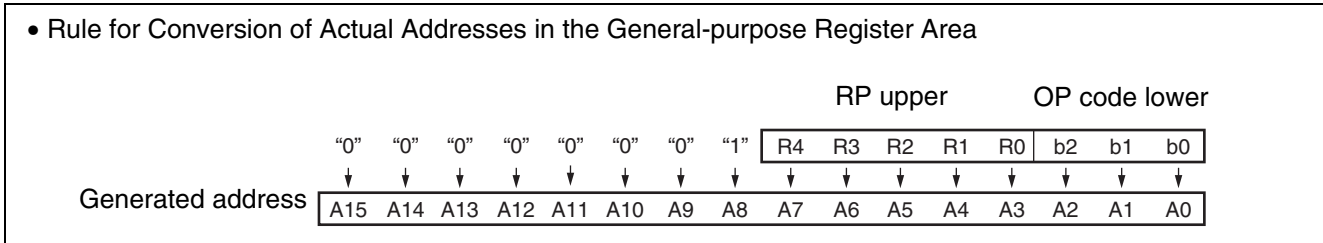


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (Refer to the diagram below.)

• Structure of the program status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different types of instructions such as MOV A and dir) using direct addresses to 0080H to 00FFH.

| Direct bank pointer (DP2 to DP0) | Specified address area | Mapping area |
|---|--|--|
| XXX _B (no effect to mapping) | 0000 _H to 007F _H | 0000 _H to 007F _H (without mapping) |
| 000 _B (initial value) | 0080 _H to 00FF _H | 0080 _H to 00FF _H (without mapping) |
| 001 _B | | 0100 _H to 017F _H |
| 010 _B | | 0180 _H to 01FF _H |
| 011 _B | | 0200 _H to 027F _H |
| 100 _B | | 0280 _H to 02FF _H |
| 101 _B | | 0300 _H to 037F _H |
| 110 _B | | 0380 _H to 03FF _H |
| 111 _B | | 0400 _H to 047F _H |

The CCR consists of the bits indicating arithmetic operation results or transfer data content and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is cleared to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

| IL1 | IL0 | Interrupt level | Priority |
|-----|-----|-----------------|---|
| 0 | 0 | 0 | High ↑ ↓ Low (no interruption) |
| 0 | 1 | 1 | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in "0". Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

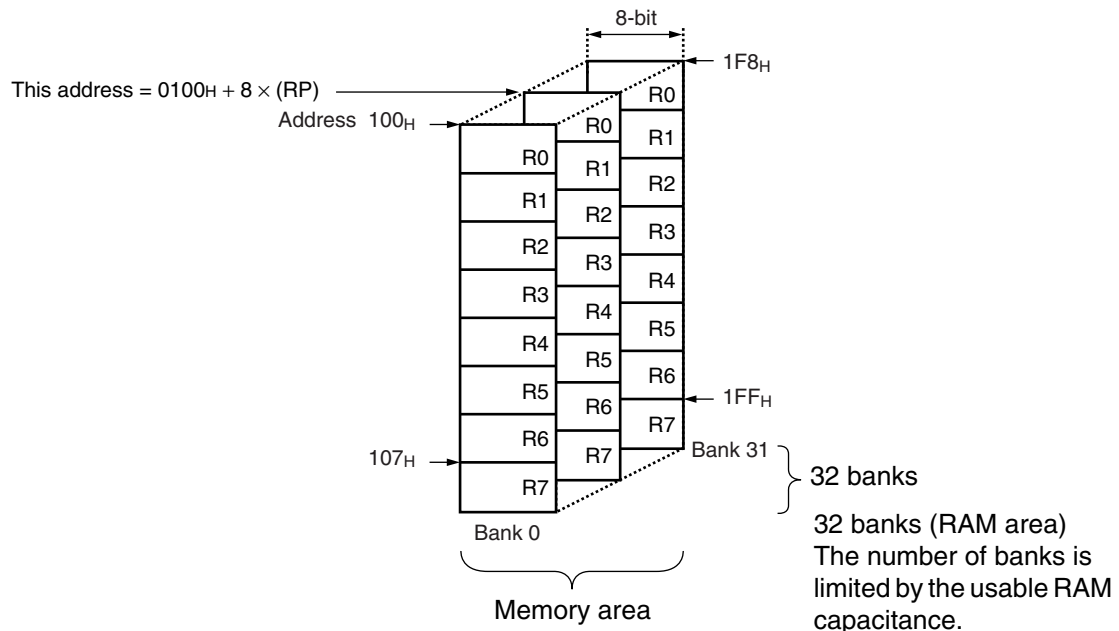
MB95130MB Series

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8 registers. Up to a total of 32 banks can be used on the MB95130MB series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



■ I/O MAP

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0000 _H | PDR0 | Port 0 data register | R/W | 00000000 _B |
| 0001 _H | DDR0 | Port 0 direction register | R/W | 00000000 _B |
| 0002 _H | PDR1 | Port 1 data register | R/W | 00000000 _B |
| 0003 _H | DDR1 | Port 1 direction register | R/W | 00000000 _B |
| 0004 _H | — | (Disabled) | — | — |
| 0005 _H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111 _B |
| 0006 _H | PLLC | PLL control register | R/W | 00000000 _B |
| 0007 _H | SYCC | System clock control register | R/W | 1010X011 _B |
| 0008 _H | STBC | Standby control register | R/W | 00000000 _B |
| 0009 _H | RSRR | Reset source register | R/W | XXXXXXXX _B |
| 000A _H | TBTC | Timebase timer control register | R/W | 00000000 _B |
| 000B _H | WPCR | Watch prescaler control register | R/W | 00000000 _B |
| 000C _H | WDTC | Watchdog timer control register | R/W | 00000000 _B |
| 000D _H to 0027 _H | — | (Disabled) | — | — |
| 0028 _H | PDRF | Port F data register | R/W | 00000000 _B |
| 0029 _H | DDRF | Port F direction register | R/W | 00000000 _B |
| 002A _H | PDRG | Port G data register | R/W | 00000000 _B |
| 002B _H | DDRG | Port G direction register | R/W | 00000000 _B |
| 002C _H | PUL0 | Port 0 pull-up register | R/W | 00000000 _B |
| 002D _H | PUL1 | Port 1 pull-up register | R/W | 00000000 _B |
| 002E _H to 0034 _H | — | (Disabled) | — | — |
| 0035 _H | PULG | Port G pull-up register | R/W | 00000000 _B |
| 0036 _H | T01CR1 | 8/16-bit compound timer 01 control status register 1 ch.0 | R/W | 00000000 _B |
| 0037 _H | T00CR1 | 8/16-bit compound timer 00 control status register 1 ch.0 | R/W | 00000000 _B |
| 0038 _H , 0039 _H | — | (Disabled) | — | — |
| 003A _H | PC01 | 8/16-bit PPG1 control register ch.0 | R/W | 00000000 _B |
| 003B _H | PC00 | 8/16-bit PPG0 control register ch.0 | R/W | 00000000 _B |
| 003C _H to 0041 _H | — | (Disabled) | — | — |
| 0042 _H | PCNTH0 | 16-bit PPG control status register (Upper byte) ch.0 | R/W | 00000000 _B |
| 0043 _H | PCNTL0 | 16-bit PPG control status register (Lower byte) ch.0 | R/W | 00000000 _B |

(Continued)

MB95130MB Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|---|-----|-----------------------|
| 0044 _H to 0047 _H | — | (Disabled) | — | — |
| 0048 _H | EIC00 | External interrupt circuit control register ch.0,ch.1 | R/W | 00000000 _B |
| 0049 _H | EIC10 | External interrupt circuit control register ch.2,ch.3 | R/W | 00000000 _B |
| 004A _H | EIC20 | External interrupt circuit control register ch.4,ch.5 | R/W | 00000000 _B |
| 004B _H | EIC30 | External interrupt circuit control register ch.6,ch.7 | R/W | 00000000 _B |
| 004C _H to 004F _H | — | (Disabled) | — | — |
| 0050 _H | SCR | LIN-UART serial control register | R/W | 00000000 _B |
| 0051 _H | SMR | LIN-UART serial mode register | R/W | 00000000 _B |
| 0052 _H | SSR | LIN-UART serial status register | R/W | 00001000 _B |
| 0053 _H | RDR/TDR | LIN-UART reception/transmission data register | R/W | 00000000 _B |
| 0054 _H | ESCR | LIN-UART extended status control register | R/W | 00000100 _B |
| 0055 _H | ECCR | LIN-UART extended communication control register | R/W | 000000XX _B |
| 0056 _H | SMC10 | UART/SIO serial mode control register 1 ch.0 | R/W | 00000000 _B |
| 0057 _H | SMC20 | UART/SIO serial mode control register 2 ch.0 | R/W | 00100000 _B |
| 0058 _H | SSR0 | UART/SIO serial status register ch.0 | R/W | 00000001 _B |
| 0059 _H | TDR0 | UART/SIO serial output data register ch.0 | R/W | 00000000 _B |
| 005A _H | RDR0 | UART/SIO serial input data register ch.0 | R | 00000000 _B |
| 005B _H to 006B _H | — | (Disabled) | — | — |
| 006C _H | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000 _B |
| 006D _H | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000 _B |
| 006E _H | ADDH | 8/10-bit A/D converter data register (Upper byte) | R/W | 00000000 _B |
| 006F _H | ADDL | 8/10-bit A/D converter data register (Lower byte) | R/W | 00000000 _B |
| 0070 _H | WCSR | Watch counter status register | R/W | 00000000 _B |
| 0071 _H | — | (Disabled) | — | — |
| 0072 _H | FSR | Flash memory status register | R/W | 000X0000 _B |
| 0073 _H | SWRE0 | Flash memory sector writing control register 0 | R/W | 00000000 _B |
| 0074 _H | SWRE1 | Flash memory sector writing control register 1 | R/W | 00000000 _B |
| 0075 _H | — | (Disabled) | — | — |
| 0076 _H | WREN | Wild register address compare enable register | R/W | 00000000 _B |
| 0077 _H | WROR | Wild register data test setting register | R/W | 00000000 _B |

(Continued)

MB95130MB Series

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0078 _H | — | (Register bank pointer (RP) Mirror of direct bank pointer (DP)) | — | — |
| 0079 _H | ILR0 | Interrupt level setting register 0 | R/W | 11111111 _B |
| 007A _H | ILR1 | Interrupt level setting register 1 | R/W | 11111111 _B |
| 007B _H | ILR2 | Interrupt level setting register 2 | R/W | 11111111 _B |
| 007C _H | ILR3 | Interrupt level setting register 3 | R/W | 11111111 _B |
| 007D _H | ILR4 | Interrupt level setting register 4 | R/W | 11111111 _B |
| 007E _H | ILR5 | Interrupt level setting register 5 | R/W | 11111111 _B |
| 007F _H | — | (Disabled) | — | — |
| 0F80 _H | WRARH0 | Wild register address setting register (Upper byte) ch.0 | R/W | 00000000 _B |
| 0F81 _H | WRARL0 | Wild register address setting register (Lower byte) ch.0 | R/W | 00000000 _B |
| 0F82 _H | WRDR0 | Wild register data setting register ch.0 | R/W | 00000000 _B |
| 0F83 _H | WRARH1 | Wild register address setting register (Upper byte) ch.1 | R/W | 00000000 _B |
| 0F84 _H | WRARL1 | Wild register address setting register (Lower byte) ch.1 | R/W | 00000000 _B |
| 0F85 _H | WRDR1 | Wild register data setting register ch.1 | R/W | 00000000 _B |
| 0F86 _H | WRARH2 | Wild register address setting register (Upper byte) ch.2 | R/W | 00000000 _B |
| 0F87 _H | WRARL2 | Wild register address setting register (Lower byte) ch.2 | R/W | 00000000 _B |
| 0F88 _H | WRDR2 | Wild register data setting register ch.2 | R/W | 00000000 _B |
| 0F89 _H to 0F91 _H | — | (Disabled) | — | — |
| 0F92 _H | T01CR0 | 8/16-bit compound timer 01 control status register 0 ch.0 | R/W | 00000000 _B |
| 0F93 _H | T00CR0 | 8/16-bit compound timer 00 control status register 0 ch.0 | R/W | 00000000 _B |
| 0F94 _H | T01DR | 8/16-bit compound timer 01 data register ch.0 | R/W | 00000000 _B |
| 0F95 _H | T00DR | 8/16-bit compound timer 00 data register ch.0 | R/W | 00000000 _B |
| 0F96 _H | TMCR0 | 8/16-bit compound timer 00/01 timer mode control register ch.0 | R/W | 00000000 _B |
| 0F97 _H to 0F9B _H | — | (Disabled) | — | — |
| 0F9C _H | PPS01 | 8/16-bit PPG1 cycle setting buffer register ch.0 | R/W | 11111111 _B |
| 0F9D _H | PPS00 | 8/16-bit PPG0 cycle setting buffer register ch.0 | R/W | 11111111 _B |
| 0F9E _H | PDS01 | 8/16-bit PPG1 duty setting buffer register ch.0 | R/W | 11111111 _B |
| 0F9F _H | PDS00 | 8/16-bit PPG0 duty setting buffer register ch.0 | R/W | 11111111 _B |
| 0FA0 _H to 0FA3 _H | — | (Disabled) | — | — |

(Continued)

MB95130MB Series

(Continued)

| Address | Register abbreviation | Register name | R/W | Initial value |
|--|-----------------------|--|-----|-----------------------|
| 0FA4 _H | PPGS | 8/16-bit PPG start register | R/W | 00000000 _B |
| 0FA5 _H | REVC | 8/16-bit PPG output inversion register | R/W | 00000000 _B |
| 0FA6 _H to 0FA9 _H | — | (Disabled) | — | — |
| 0FAA _H | PDCRH0 | 16-bit PPG down counter register (Upper byte) ch.0 | R | 00000000 _B |
| 0FAB _H | PDCRL0 | 16-bit PPG down counter register (Lower byte) ch.0 | R | 00000000 _B |
| 0FAC _H | PCSRH0 | 16-bit PPG cycle setting buffer register (Upper byte) ch.0 | R/W | 11111111 _B |
| 0FAD _H | PCSRL0 | 16-bit PPG cycle setting buffer register (Lower byte) ch.0 | R/W | 11111111 _B |
| 0FAE _H | PDUTH0 | 16-bit PPG duty setting buffer register (Upper byte) ch.0 | R/W | 11111111 _B |
| 0FAF _H | PDUTL0 | 16-bit PPG duty setting buffer register (Lower byte) ch.0 | R/W | 11111111 _B |
| 0FB0 _H to 0FBB _H | — | (Disabled) | — | — |
| 0FBC _H | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000 _B |
| 0FBD _H | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000 _B |
| 0FBE _H | PSSR0 | UART/SIO dedicated baud rate generator prescaler selection register ch.0 | R/W | 00000000 _B |
| 0FBF _H | BRSR0 | UART/SIO dedicated baud rate generator baud rate setting register ch.0 | R/W | 00000000 _B |
| 0FC0 _H to 0FC2 _H | — | (Disabled) | — | — |
| 0FC3 _H | AIDRL | A/D input disable register (Lower byte) | R/W | 00000000 _B |
| 0FC4 _H to 0FE2 _H | — | (Disabled) | — | — |
| 0FE3 _H | WCDR | Watch counter data register | R/W | 00111111 _B |
| 0FE4 _H to 0FE6 _H | — | (Disabled) | — | — |
| 0FE7 _H | ILSR2 | Input level select register 2 (option) | R/W | 00000000 _B |
| 0FE8 _H , 0FE9 _H | — | (Disabled) | — | — |
| 0FEA _H | CSVCR | Clock supervisor control register | R/W | 00011100 _B |
| 0FEB _H to 0FED _H | — | (Disabled) | — | — |
| 0FEE _H | ILSR | Input level select register | R/W | 00000000 _B |
| 0FEF _H | WICR | Interrupt pin control register | R/W | 01000000 _B |
| 0FF0 _H to 0FFF _H | — | (Disabled) | — | — |

- R/W access symbols
 - R/W : Readable / Writable
 - R : Read only
 - W : Write only
- Initial value symbols
 - 0 : The initial value of this bit is "0".
 - 1 : The initial value of this bit is "1".
 - X : The initial value of this bit is undefined.

Note : Do not write to the " (Disabled) ". Reading the " (Disabled) " returns an undefined value.

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■ INTERRUPT SOURCE TABLE

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Same level priority order (at simultaneous occurrence) |
|---------------------------------------|--------------------------|----------------------|-------------------|--|--|
| | | Upper | Lower | | |
| External interrupt ch.0 | IRQ0 | FFFA _H | FFFB _H | L00 [1 : 0] | <div style="text-align: center;">High</div> <div style="text-align: center;">↑</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Low</div> |
| External interrupt ch.4 | | | | | |
| External interrupt ch.1 | IRQ1 | FFF8 _H | FFF9 _H | L01 [1 : 0] | |
| External interrupt ch.5 | | | | | |
| External interrupt ch.2 | IRQ2 | FFF6 _H | FFF7 _H | L02 [1 : 0] | |
| External interrupt ch.6 | | | | | |
| External interrupt ch.3 | IRQ3 | FFF4 _H | FFF5 _H | L03 [1 : 0] | |
| External interrupt ch.7 | | | | | |
| UART/SIO ch.0 | IRQ4 | FFF2 _H | FFF3 _H | L04 [1 : 0] | |
| 8/16-bit compound timer ch.0 (Lower) | IRQ5 | FFF0 _H | FFF1 _H | L05 [1 : 0] | |
| 8/16-bit compound timer ch.0 (Higher) | IRQ6 | FFEE _H | FFEF _H | L06 [1 : 0] | |
| LIN-UART (reception) | IRQ7 | FFEC _H | FFED _H | L07 [1 : 0] | |
| LIN-UART (transmission) | IRQ8 | FFEA _H | FFEB _H | L08 [1 : 0] | |
| (Unused) | IRQ9 | FFE8 _H | FFE9 _H | L09 [1 : 0] | |
| (Unused) | IRQ10 | FFE6 _H | FFE7 _H | L10 [1 : 0] | |
| (Unused) | IRQ11 | FFE4 _H | FFE5 _H | L11 [1 : 0] | |
| 8/16-bit PPG ch.0 (Upper) | IRQ12 | FFE2 _H | FFE3 _H | L12 [1 : 0] | |
| 8/16-bit PPG ch.0 (Lower) | IRQ13 | FFE0 _H | FFE1 _H | L13 [1 : 0] | |
| (Unused) | IRQ14 | FFDE _H | FFDF _H | L14 [1 : 0] | |
| 16-bit PPG ch.0 | IRQ15 | FFDC _H | FFDD _H | L15 [1 : 0] | |
| (Unused) | IRQ16 | FFDA _H | FFDB _H | L16 [1 : 0] | |
| (Unused) | IRQ17 | FFD8 _H | FFD9 _H | L17 [1 : 0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6 _H | FFD7 _H | L18 [1 : 0] | |
| Timebase timer | IRQ19 | FFD4 _H | FFD5 _H | L19 [1 : 0] | |
| Watch prescaler/Watch counter | IRQ20 | FFD2 _H | FFD3 _H | L20 [1 : 0] | |
| (Unused) | IRQ21 | FFD0 _H | FFD1 _H | L21 [1 : 0] | |
| (Unused) | IRQ22 | FFCE _H | FFCF _H | L22 [1 : 0] | |
| Flash memory | IRQ23 | FFCC _H | FFCD _H | L23 [1 : 0] | |

■ ELECTRICAL CHARACTERISTICS

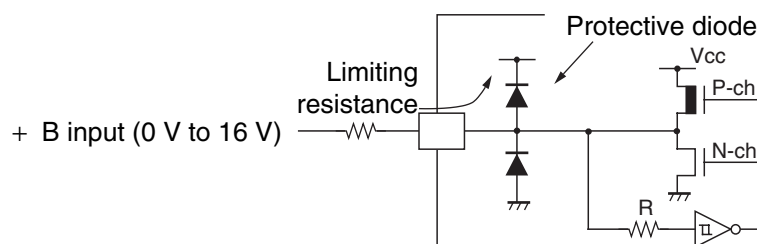
1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|-----------------------|----------------|----------------|------|---|
| | | Min | Max | | |
| Power supply voltage*1 | V_{CC} AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | *2 |
| Input voltage*1 | V_I | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | *3 |
| Output voltage*1 | V_O | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | *3 |
| Maximum clamp current | I_{CLAMP} | - 2.0 | + 2.0 | mA | Applicable to pins*4 |
| Total maximum clamp current | ΣI_{CLAMP} | — | 20 | mA | Applicable to pins*4 |
| “L” level maximum output current | I_{OL1} | — | 15 | mA | Other than PF0, PF1 |
| | I_{OL2} | | 15 | | PF0, PF1 |
| “L” level average current | I_{OLAV1} | — | 4 | mA | Other than PF0, PF1 Average output current = operating current × operating ratio (1 pin) |
| | I_{OLAV2} | | 12 | | PF0, PF1 Average output current = operating current × operating ratio (1 pin) |
| “L” level total maximum output current | ΣI_{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI_{OLAV} | — | 50 | mA | Total average output current = operating current × operating ratio (Total of pins) |
| “H” level maximum output current | I_{OH1} | — | - 15 | mA | Other than PF0, PF1 |
| | I_{OH2} | | - 15 | | PF0, PF1 |
| “H” level average current | I_{OHAV1} | — | - 4 | mA | Other than PF0, PF1 Average output current = operating current × operating ratio (1 pin) |
| | I_{OHAV2} | | - 8 | | PF0, PF1 Average output current = operating current × operating ratio (1 pin) |
| “H” level total maximum output current | ΣI_{OH} | — | - 100 | mA | |
| “H” level total average output current | ΣI_{OHAV} | — | - 50 | mA | Total average output current = operating current × operating ratio (Total number of pins) |
| Power consumption | P_d | — | 320 | mW | |
| Operating temperature | T_A | - 40 | + 85 | °C | |
| Storage temperature | T_{stg} | - 55 | + 150 | °C | |

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- *1: The parameter is based on $AV_{SS} = V_{SS} = 0.0\text{ V}$.
- *2: Apply equal potential to AV_{CC} and V_{CC} .
- *3: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.
- *4: Applicable pins: P10 to P15, PF0, PF1 (Inapplicable pins: PG1, PG2)
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
 - Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the + B input pin open.
 - Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.
 - Sample recommended circuits :

- Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

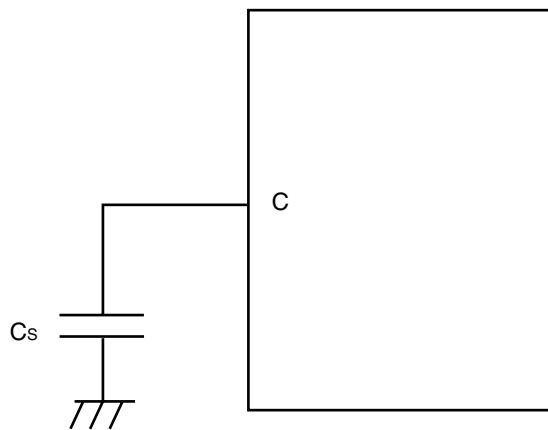
| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------|-------------------|--------------------|-------------------|--------------------|------------------------------|
| | | Min | Max | | |
| Power supply voltage | V_{CC}, AV_{CC} | 2.42* ² | 5.5* ¹ | V | At normal operation |
| | | 2.3 | 5.5 | | Holds condition in stop mode |
| Smoothing capacitor | C_S | 0.1 | 1.0 | μF | * ³ |
| Operating temperature | T_A | - 40 | + 85 | $^{\circ}\text{C}$ | |

*1: The value varies depending on the operating frequency.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S . For connection of smoothing capacitor C_S , refer to the diagram below.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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3. DC Characteristics

($V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--------------------------|------------|--|---------------------------|----------------|----------------|----------------|-------------------------------------|--|
| | | | | Min | Typ | Max | | |
| “H” level input voltage | V_{IHI} | P04 (selectable in SIN), P10 (selectable in UI0) | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHSI} | P00 to P07, P10 to P16, PF0, PF1, PG1, PG2 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHA} | P00 to P07, P10 to P16, PF0, PF1, PG1, PG2 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Pin input at selecting of Automotive input level |
| | V_{IHM} | \overline{RST} , MOD | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | CMOS input (Flash memory product) |
| — | | | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input (MASK ROM product) | |
| “L” level input voltage | V_{IL} | P04 (selectable in SIN), P10 (selectable in UI0) | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | Hysteresis input |
| | V_{ILS} | P00 to P07, P10 to P16, PF0, PF1, PG1, PG2 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILA} | P00 to P07, P10 to P16, PF0, PF1, PG1, PG2 | — | $V_{SS} - 0.3$ | — | $0.5 V_{CC}$ | V | Pin input at selecting of Automotive input level |
| | V_{ILM} | \overline{RST} , MOD | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | CMOS input (Flash memory product) |
| — | | | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input (MASK ROM product) | |
| “H” level output voltage | V_{OH1} | Output pins other than PF0, PF1 | $I_{OH} = -4.0\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| | V_{OH2} | PF0, PF1 | $I_{OH} = -8.0\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| “L” level output voltage | V_{OL1} | Output pins other than PF0 to PF7, \overline{RST}^*1 | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| | V_{OL2} | PF0, PF1 | $I_{OL} = 12\text{ mA}$ | — | — | 0.4 | V | |

(Continued)

MB95130MB Series

($V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|---|--|-------|------|------|------------------|--|
| | | | | Min | Typ | Max | | |
| Input leakage current (Hi-Z output leakage current) | I_{LI} | P00 to P07, P10 to P16, PF0, PF1, PG1, PG2 | $0.0\text{ V} < V_I < V_{CC}$ | -5 | — | +5 | μA | When the pull-up prohibition setting |
| Pull-up resistor | R_{PULL} | P00 to P07, P10 to P16, PG1, PG2 | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | $\text{k}\Omega$ | When the pull-up permission setting |
| Pull-down resistor | R_{MOD} | MOD | $V_I = V_{CC}$ | 50 | 100 | 200 | $\text{k}\Omega$ | MASK ROM product only |
| Input capacity | C_{IN} | Other than AV_{CC} , AV_{SS} , C, V_{CC} and V_{SS} | $f = 1\text{ MHz}$ | — | 5 | 15 | pF | |
| Power supply current*2 | I_{CC} | V_{CC} (External clock operation) | $V_{CC} = 5.5\text{ V}$ $F_{CH} = 20\text{ MHz}$ $F_{MP} = 10\text{ MHz}$ Main clock mode (divided by 2) | — | 9.5 | 12.5 | mA | Flash memory product (at other than Flash memory writing and erasing) |
| | | | | — | 30 | 35 | mA | Flash memory product (at Flash memory writing and erasing) |
| | | | | — | 7.2 | 9.5 | mA | MASK ROM product |
| | | | $F_{CH} = 32\text{ MHz}$ $F_{MP} = 16\text{ MHz}$ Main clock mode (divided by 2) | — | 15.2 | 20.0 | mA | Flash memory product (at other than Flash memory writing and erasing) |
| | | | | — | 35.7 | 42.5 | mA | Flash memory product (at Flash memory writing and erasing) |
| | | | | — | 11.6 | 15.2 | mA | MASK ROM product |

(Continued)

MB95130MB Series

($V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------|---------------------|---|--|-------|------|------|------|-------------------------|
| | | | | Min | Typ | Max | | |
| Power supply current*2 | I _{CCS} | V _{CC} (External clock operation) | V _{CC} = 5.5 V F _{CH} = 20 MHz F _{MP} = 10 MHz Main Sleep mode (divided by 2) | — | 4.5 | 7.5 | mA | |
| | | | F _{CH} = 32 MHz F _{MP} = 16 MHz Main Sleep mode (divided by 2) | — | 7.2 | 12.0 | mA | |
| | I _{CCCL} | | V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Sub clock mode (divided by 2), T _A = +25 °C | — | 45 | 100 | μA | Dual clock product only |
| | I _{CCLS} | | V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Sub sleep mode (divided by 2), T _A = +25 °C | — | 10 | 81 | μA | Dual clock product only |
| | I _{CCCT} | | V _{CC} = 5.5 V F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25 °C | — | 4.6 | 27 | μA | Dual clock product only |
| | I _{CCMPLL} | | V _{CC} = 5.5 V F _{CH} = 4 MHz F _{MP} = 10 MHz Main PLL mode (multiplied by 2.5) | — | 9.3 | 12.5 | mA | Flash memory product |
| | | | F _{CH} = 6.4 MHz F _{MP} = 16 MHz Main PLL mode (multiplied by 2.5) | — | 7 | 9.5 | mA | MASK ROM product |
| | | | F _{CH} = 6.4 MHz F _{MP} = 16 MHz Main PLL mode (multiplied by 2.5) | — | 14.9 | 20.0 | mA | Flash memory product |
| | | | F _{CH} = 6.4 MHz F _{MP} = 16 MHz Main PLL mode (multiplied by 2.5) | — | 11.2 | 15.2 | mA | MASK ROM product |
| | I _{CCSPLL} | | V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 128 kHz Sub PLL mode (multiplied by 4), T _A = +25 °C | — | 160 | 400 | μA | Dual clock product only |

(Continued)

MB95130MB Series

(Continued)

($V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------|------------------|---|--|-------|------|------|------|---|
| | | | | Min | Typ | Max | | |
| Power supply current*2 | I _{CTS} | V _{CC} (External clock operation) | V _{CC} = 5.5 V F _{CH} = 10 MHz Timebase timer mode T _A = +25 °C | — | 0.15 | 1.1 | mA | |
| | I _{CCH} | | V _{CC} = 5.5 V Sub stop mode T _A = +25 °C | — | 3.5 | 20.0 | μA | Main stop mode for single clock product |
| | I _A | AV _{CC} | V _{CC} = 5.5 V F _{CH} = 16 MHz When A/D conversion is in operation | — | 2.4 | 4.7 | mA | |
| | I _{AH} | | V _{CC} = 5.5 V F _{CH} = 16 MHz When A/D conversion is stopped T _A = +25 °C | — | 1 | 5 | μA | |

*1: Product without clock supervisor only

- *2:
- The power supply current is specified by the external clock. When the low-voltage detection and clock supervisor options are selected, the consumption current values of both the low-voltage detection circuit (I_{LVD}) and the built-in CR oscillator (I_{CSV}) must also be added to the power supply current value.
 - Refer to “4. AC Characteristics: (1) Clock Timing” for F_{CH} and F_{CL}.
 - Refer to “4. AC Characteristics: (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

MB95130MB Series

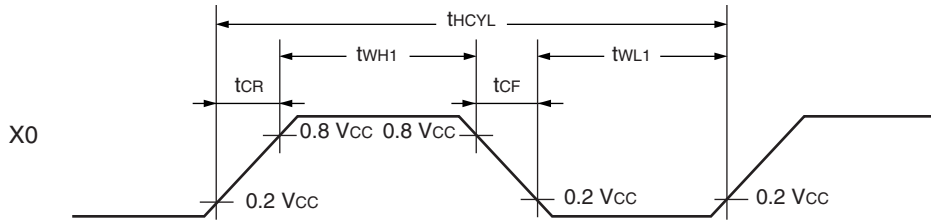
4. AC Characteristics

(1) Clock Timing

($V_{CC} = 2.42\text{ V to } 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$)

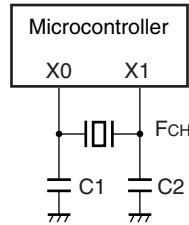
| Parameter | Sym- bol | Pin name | Condi- tion | Value | | | Unit | Remarks |
|----------------------------|--------------------------------------|----------|----------------|-------|--------|-------|---|--|
| | | | | Min | Typ | Max | | |
| Clock frequency | F _{CH} | X0, X1 | — | 1.00 | — | 16.25 | MHz | When using main oscillation circuit |
| | | | | 1.00 | — | 32.50 | MHz | When using external clock |
| | | | | 3.00 | — | 10.00 | MHz | Main PLL multiplied by 1 |
| | | | | 3.00 | — | 8.13 | MHz | Main PLL multiplied by 2 |
| | | | | 3.00 | — | 6.50 | MHz | Main PLL multiplied by 2.5 |
| | | | | 3.00 | — | 4.06 | MHz | Main PLL multiplied by 4 |
| | F _{CL} | X0A, X1A | | — | 32.768 | — | kHz | When using sub oscillation circuit |
| | — | — | | — | 32.768 | — | kHz | When using sub PLL $V_{CC} = 2.3\text{ V to } 3.6\text{ V}$ |
| Clock cycle time | t _{H CYL} | X0, X1 | 61.5 | — | 1000 | ns | When using main oscillation circuit | |
| | — | — | 30.8 | — | 1000 | ns | When using external clock | |
| | t _{L CYL} | X0A, X1A | — | 30.5 | — | μs | When using sub oscillation circuit | |
| Input clock pulse width | t _{WH1} t _{WL1} | X0 | 61.5 | — | — | ns | When using external clock duty ratio is about 30% to 70%. | |
| | t _{WH2} t _{WL2} | X0A | — | 15.2 | — | μs | | |
| Input clock rise/fall time | t _{CR} t _{CF} | X0, X0A | — | — | 5 | ns | When using external clock | |

- Input wave form for using external clock (main clock)

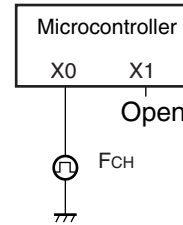


- Figure of Main Clock Input Port External Connection

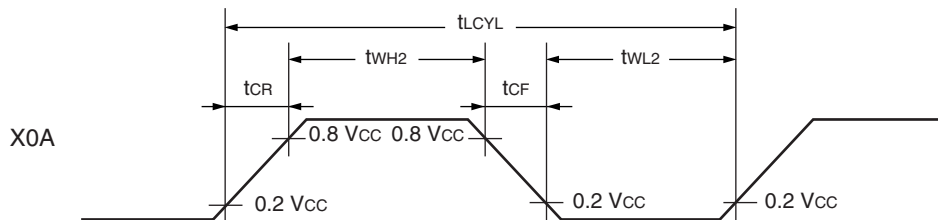
When using crystal or ceramic oscillator



When using external clock

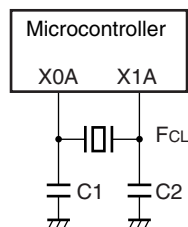


- Input wave form for using external clock (sub clock)

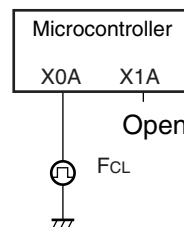


- Figure of Sub clock Input Port External Connection

When using crystal or ceramic oscillator



When using external clock



MB95130MB Series

(2) Source Clock/Machine Clock

($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

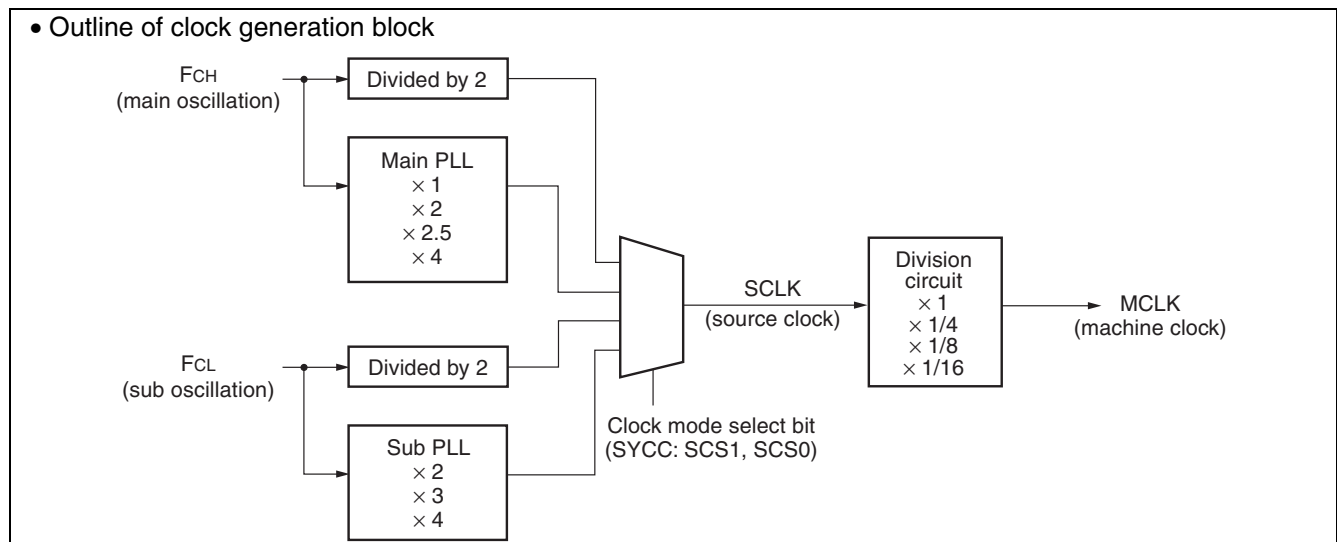
| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|--|------------|----------|--------|-----|---------|---------------|--|
| | | | Min | Typ | Max | | |
| Source clock cycle time* ¹ (Clock before setting division) | t_{SCLK} | — | 61.5 | — | 2000 | ns | When using main clock Min : $F_{CH} = 8.125\text{ MHz}$, PLL multiplied by 2 Max : $F_{CH} = 1\text{ MHz}$, divided by 2 |
| | | | 7.6 | — | 61.0 | μs | When using sub clock Min : $F_{CL} = 32\text{ kHz}$, PLL multiplied by 4 Max : $F_{CL} = 32\text{ kHz}$, divided by 2 |
| Source clock frequency | F_{SP} | — | 0.50 | — | 16.25 | MHz | When using main clock |
| | F_{SPL} | — | 16.384 | — | 131.072 | kHz | When using sub clock |
| Machine clock cycle time* ² (Minimum instruction execution time) | t_{MCLK} | — | 61.5 | — | 32000 | ns | When using main clock Min : $F_{SP} = 16.25\text{ MHz}$, no division Max : $F_{SP} = 0.5\text{ MHz}$, divided by 16 |
| | | | 7.6 | — | 976.5 | μs | When using sub clock Min : $F_{SPL} = 131\text{ kHz}$, no division Max : $F_{SPL} = 16\text{ kHz}$, divided by 16 |
| Machine clock frequency | F_{MP} | — | 0.031 | — | 16.250 | MHz | When using main clock |
| | F_{MPL} | — | 1.024 | — | 131.072 | kHz | When using sub clock |

*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

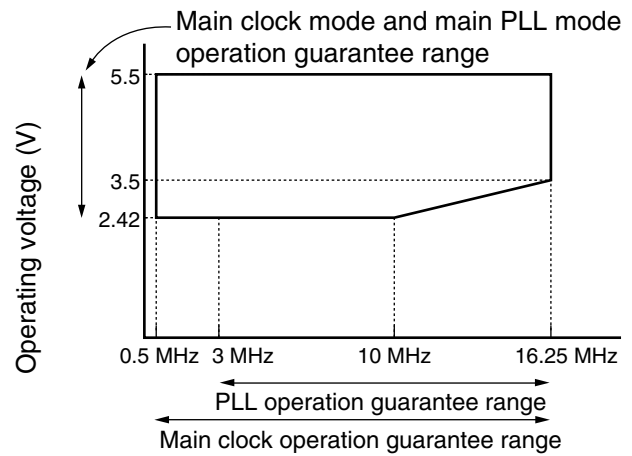
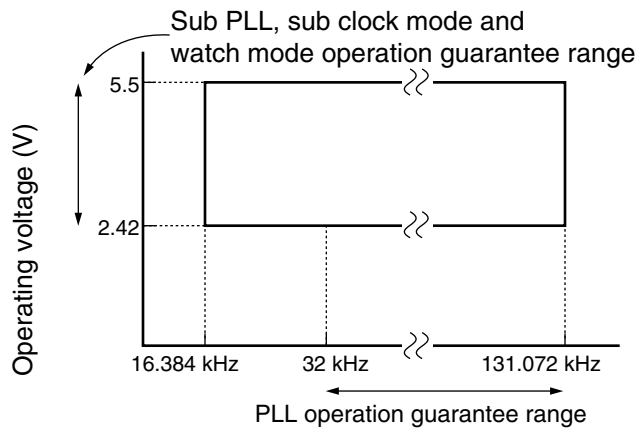
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

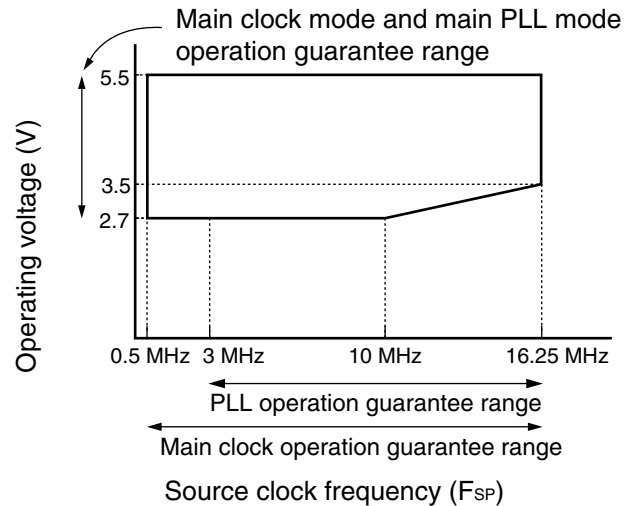
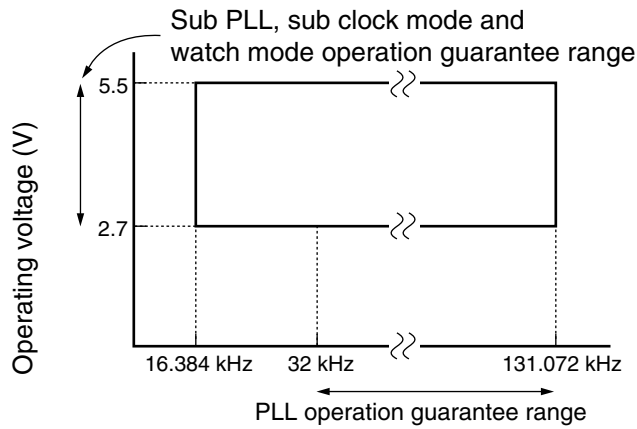


MB95130MB Series

- Operating voltage - Operating frequency (When $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)
 - MB95F133MBS/F133NBS/F133JBS/F134MBS/F134NBS/F134JBS/F136MBS/F136NBS/F136JBS/
MB95F133MBW/F133NBW/F133JBW/F134MBW/F134NBW/F134JBW/F136MBW/F136NBW/
MB95F136JBW

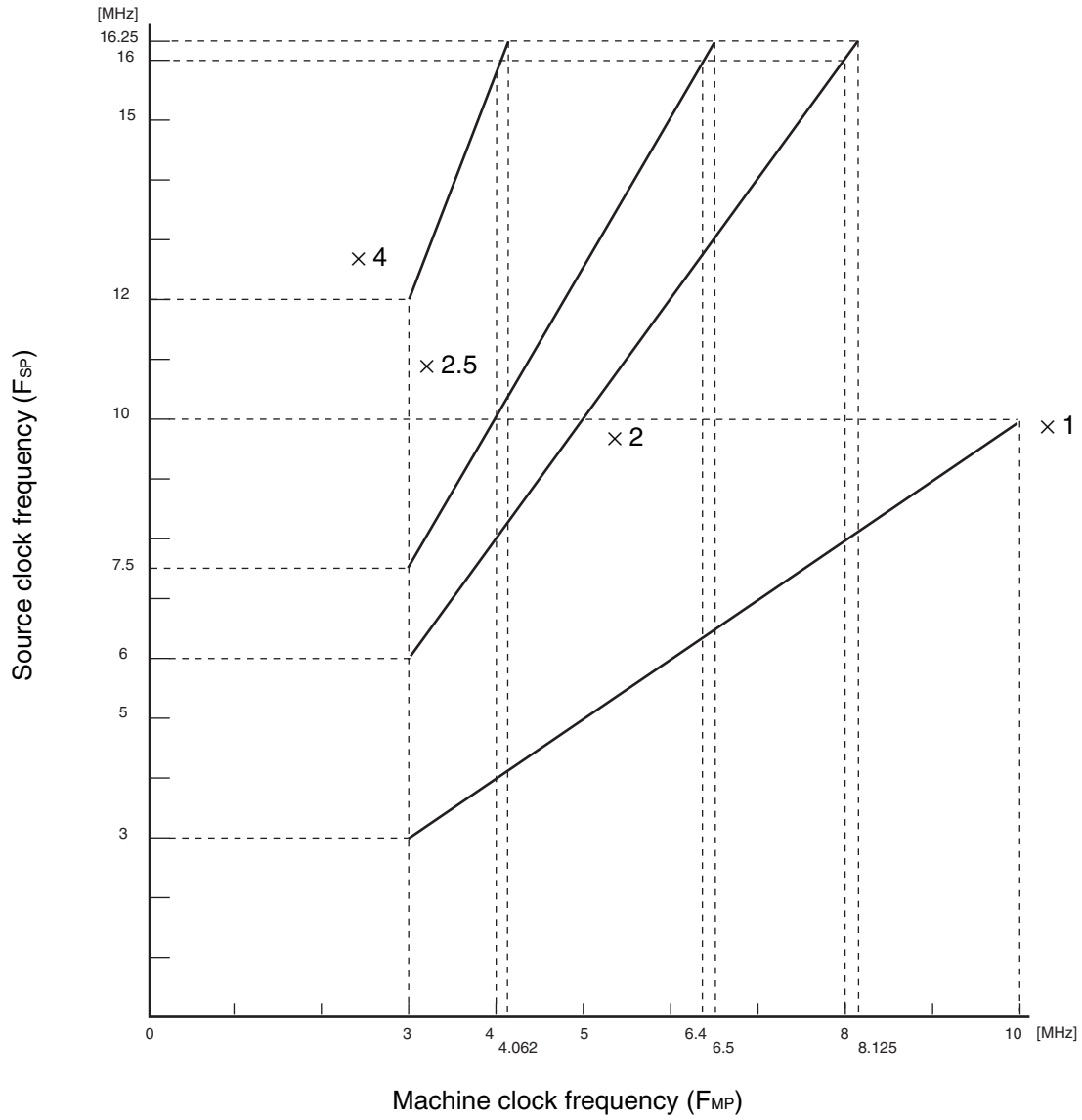


- Operating voltage - Operating frequency (When $T_A = +5\text{ }^\circ\text{C}$ to $+35\text{ }^\circ\text{C}$)
 - MB95FV100D-103



MB95130MB Series

- Main PLL operation frequency



(3) External Reset

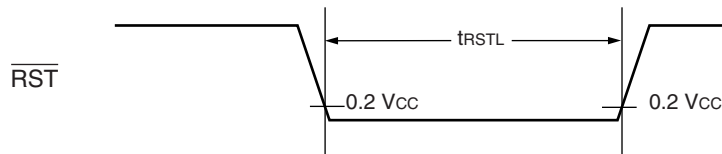
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|-------------------|-------------------------|--|-----|---------------|---|
| | | | Min | Max | | |
| $\overline{\text{RST}}$ "L" level pulse width | t_{RSTL} | $\overline{\text{RST}}$ | $2 t_{\text{MCLK}}^{*1}$ | — | ns | At normal operation |
| | | | Oscillation time of oscillator ^{*2} + 100 | — | μs | At stop mode, sub clock mode, sub sleep mode & watch mode |
| | | | 100 | — | μs | At timebase timer mode |

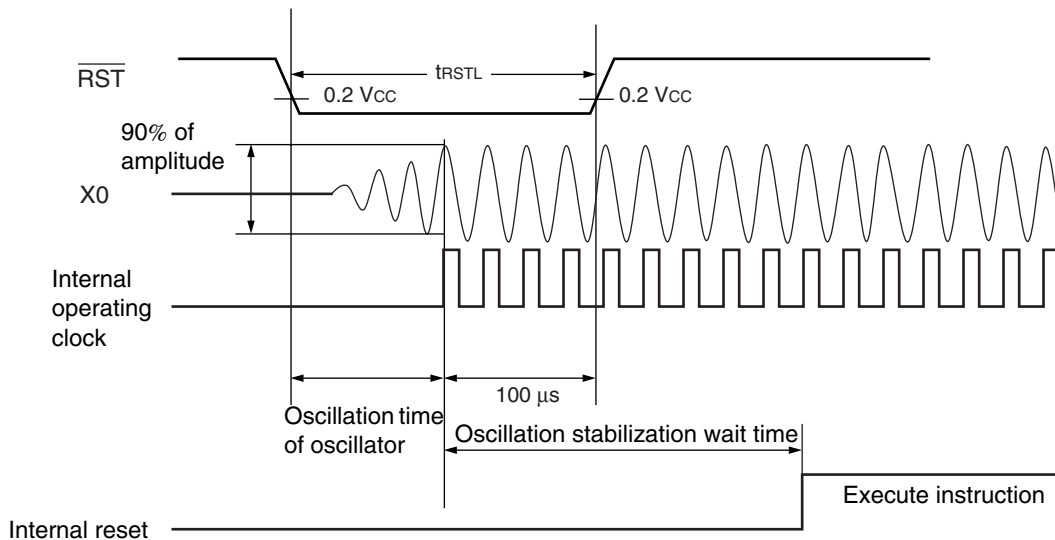
*1 : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .

*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs and several ms. In the external clock, the oscillation time is 0 ms.

- At normal operation



- At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



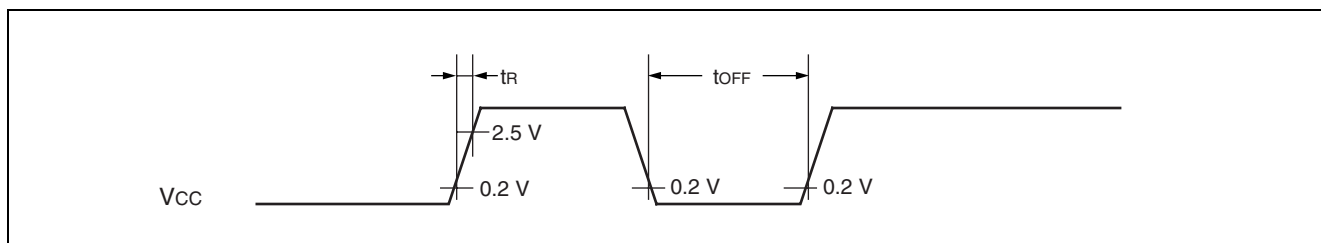
MB95130MB Series

(4) Power-on Reset

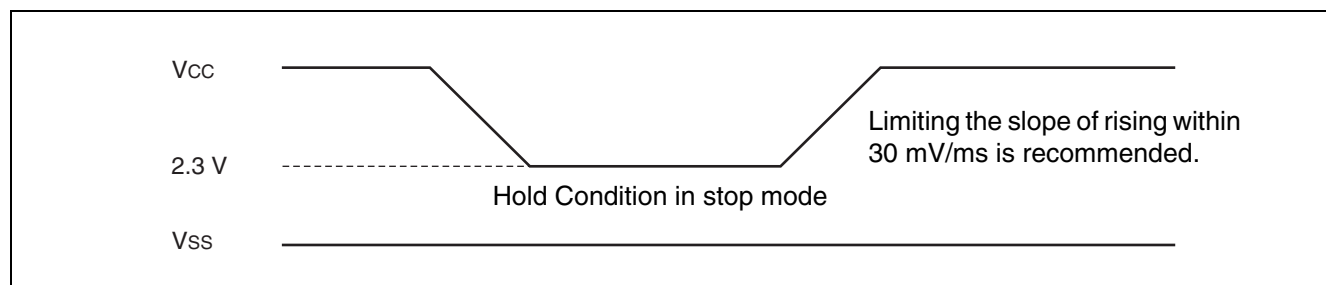
($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--------------------------|-----------|----------|-----------|-------|-----|------|-----------------------------|
| | | | | Min | Max | | |
| Power supply rising time | t_R | V_{CC} | — | — | 50 | ms | |
| Power supply cutoff time | t_{OFF} | | — | 1 | — | ms | Waiting time until power-on |

Note : Complete the power-on process within the selected oscillation stabilization wait time.



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

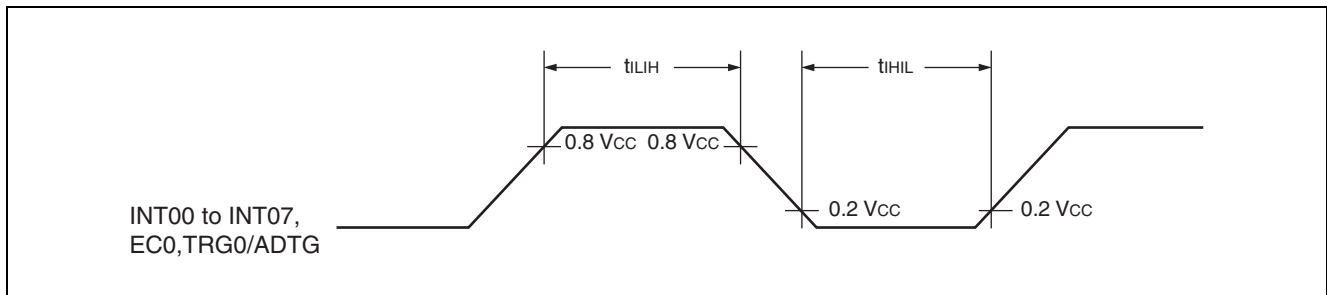


(5) Peripheral Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Value | | Unit |
|----------------------------|-----------|-----------------------------------|----------------|-----|------|
| | | | Min | Max | |
| Peripheral input "H" pulse | t_{LIH} | INT00 to INT07, EC0, TRG0/ADTG | $2 t_{MCLK}^*$ | — | ns |
| Peripheral input "L" pulse | t_{LIL} | | $2 t_{MCLK}^*$ | — | ns |

* : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .



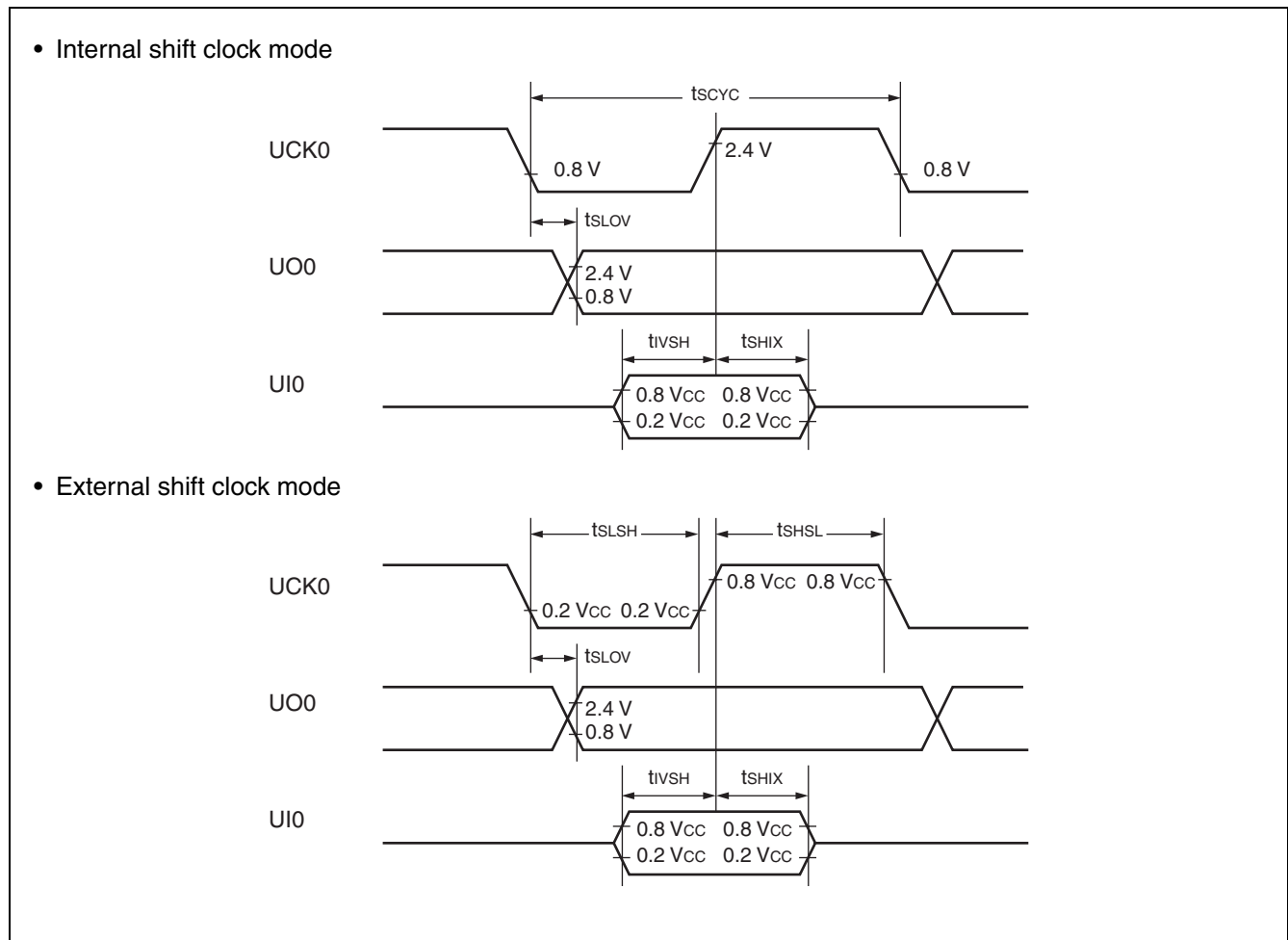
MB95130MB Series

(6) UART/SIO Serial I/O Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|------------------------------|------------|-----------|---|----------------|------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | UCK0 | Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $4 t_{MCLK}^*$ | — | ns |
| UCK ↓ → UO time | t_{SLOV} | UCK0, UO0 | | - 190 | +190 | ns |
| Valid UI → UCK ↑ | t_{IVSH} | UCK0, UI0 | | $2 t_{MCLK}^*$ | — | ns |
| UCK ↑ → valid UI hold time | t_{SHIX} | UCK0, UI0 | | $2 t_{MCLK}^*$ | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | UCK0 | External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $4 t_{MCLK}^*$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | UCK0 | | $4 t_{MCLK}^*$ | — | ns |
| UCK ↓ → UO time | t_{SLOV} | UCK0, UO0 | | — | 190 | ns |
| Valid UI → UCK ↑ | t_{IVSH} | UCK0, UI0 | | $2 t_{MCLK}^*$ | — | ns |
| UCK ↑ → valid UI hold time | t_{SHIX} | UCK0, UI0 | $2 t_{MCLK}^*$ | — | ns | |

* : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .



(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2

(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|---|-------------------------|------------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVI} | SCK, SOT | | -95 | +95 | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK | External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $3 t_{MCLK}^{*3} - t_R$ | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVE} | SCK, SOT | | — | $2 t_{MCLK}^{*3} + 95$ | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHE} | SCK, SIN | | 190 | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXE} | SCK, SIN | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK fall time | t_F | SCK | | — | 10 | ns |
| SCK rise time | t_R | SCK | | — | 10 | ns |

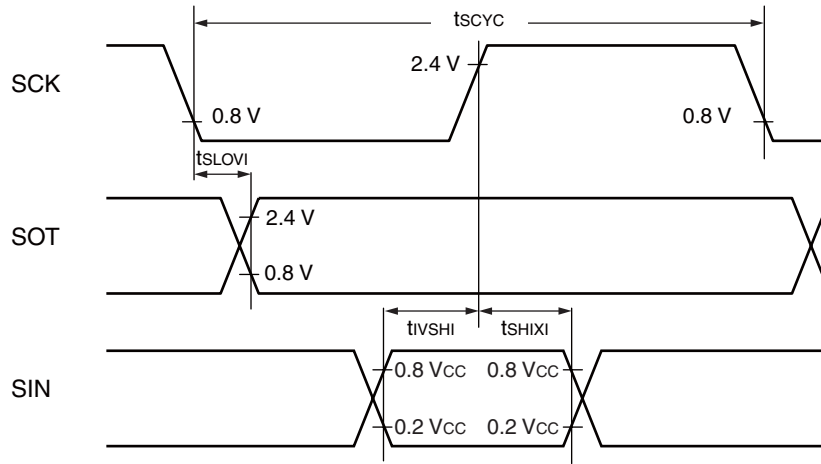
*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

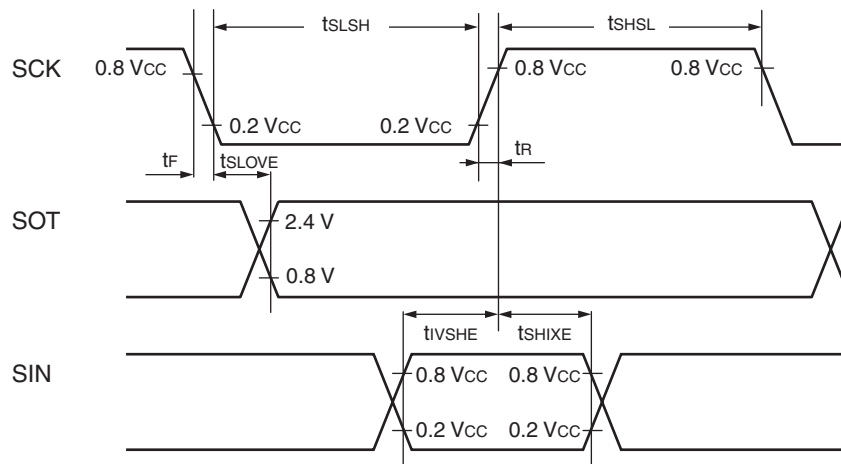
*3 : Refer to "(2) Source Clock/Machine Clock" for t_{MCLK} .

MB95130MB Series

- Internal shift clock mode



- External shift clock mode



MB95130MB Series

Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

($V_{CC} = 5.0 V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 V$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|---|-------------------------|------------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK \uparrow → SOT delay time | t_{SHOVI} | SCK, SOT | | -95 | +95 | ns |
| Valid SIN → SCK \downarrow | t_{IVSLI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK \downarrow → valid SIN hold time | t_{SLIXI} | SCK, SIN | | 0 | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL}$. | $3 t_{MCLK}^{*3} - t_R$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK \uparrow → SOT delay time | t_{SHOVE} | SCK, SOT | | — | $2 t_{MCLK}^{*3} + 95$ | ns |
| Valid SIN → SCK \downarrow | t_{IVSLE} | SCK, SIN | | 190 | — | ns |
| SCK \downarrow → valid SIN hold time | t_{SLIXE} | SCK, SIN | | $t_{MCLK}^{*3} + 95$ | — | ns |
| SCK fall time | t_F | SCK | | — | 10 | ns |
| SCK rise time | t_R | SCK | | — | 10 | ns |

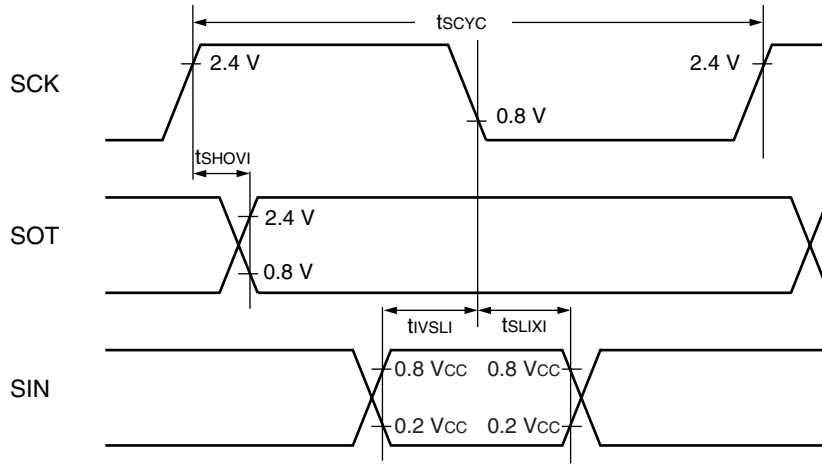
*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

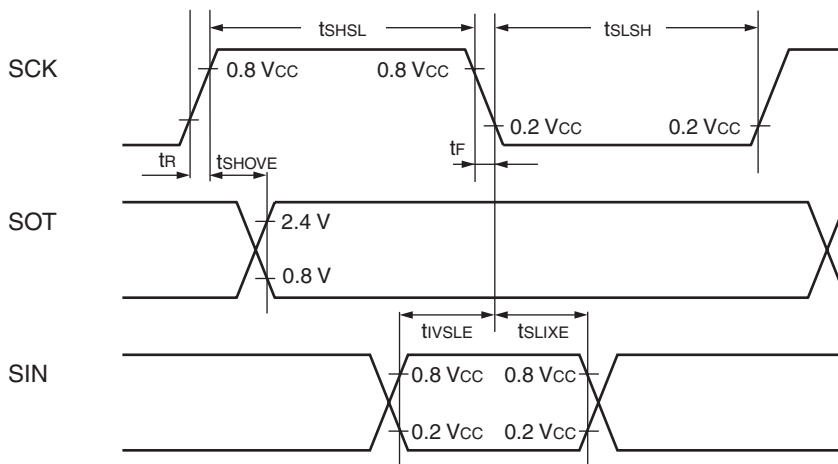
*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK} .

MB95130MB Series

- Internal shift clock mode



- External shift clock mode



MB95130MB Series

Sampling at the rising edge of sampling clock*¹ and enabled serial clock delay*²
 (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

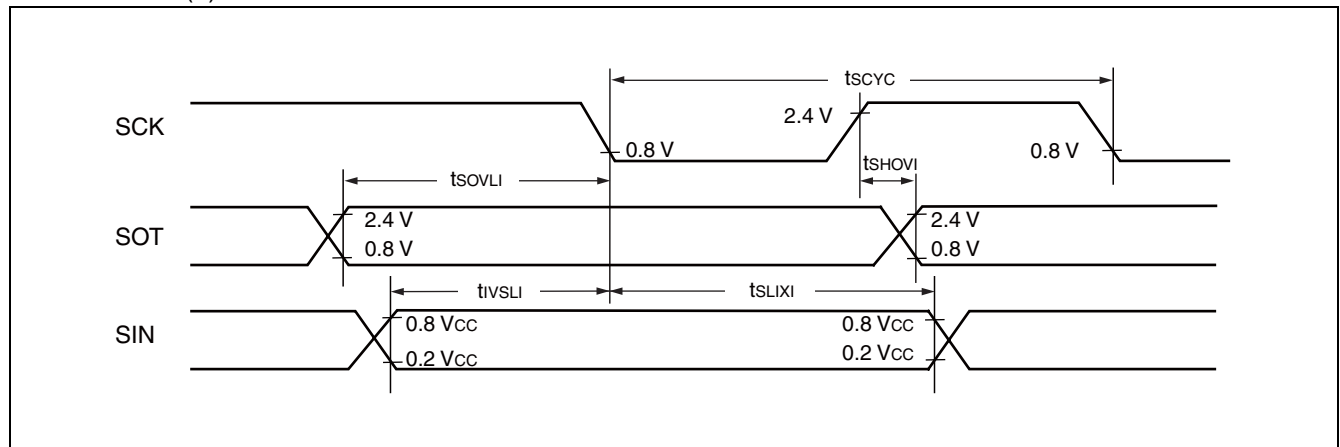
($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|--|-----------------------|-------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operation output pin : $C_L = 80\text{ pF} + 1\text{ TTL.}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK \uparrow → SOT delay time | t_{SHOVI} | SCK, SOT | | -95 | +95 | ns |
| Valid SIN → SCK \downarrow | t_{IVSLI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK \downarrow → valid SIN hold time | t_{SLIXI} | SCK, SIN | | 0 | — | ns |
| SOT → SCK \downarrow delay time | t_{SOVLI} | SCK, SOT | | — | $4 t_{MCLK}^{*3}$ | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK} .



MB95130MB Series

Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
 (ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

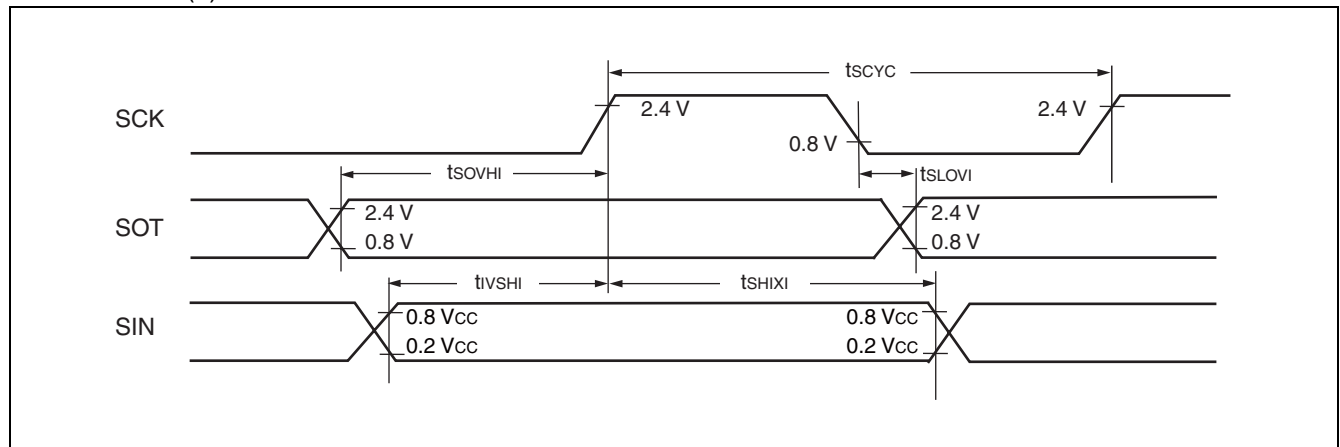
($V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|--|-------------|----------|--|-----------------------|-------------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal clock operating output pin : $C_L = 80\text{ pF} + 1\text{ TTL.}$ | $5 t_{MCLK}^{*3}$ | — | ns |
| SCK $\downarrow \rightarrow$ SOT delay time | t_{SLOVI} | SCK, SOT | | -95 | +95 | ns |
| Valid SIN \rightarrow SCK \uparrow | t_{IVSHI} | SCK, SIN | | $t_{MCLK}^{*3} + 190$ | — | ns |
| SCK $\uparrow \rightarrow$ valid SIN hold time | t_{SHIXI} | SCK, SIN | | 0 | — | ns |
| SOT \rightarrow SCK \uparrow delay time | t_{SOVHI} | SCK, SOT | | — | $4 t_{MCLK}^{*3}$ | ns |

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK} .

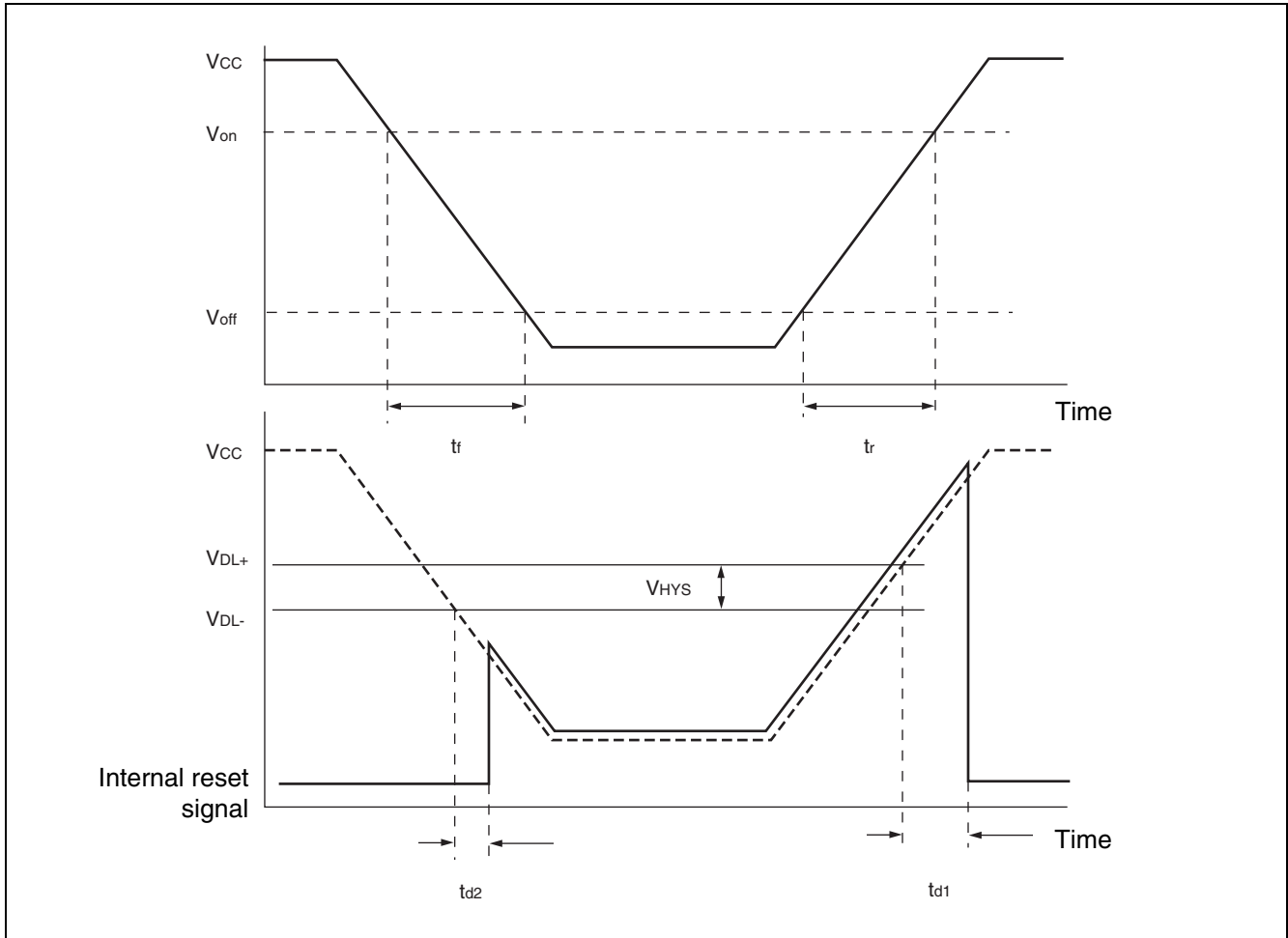


(8) Low voltage Detection

($A_{VSS} = V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|-----------|-------|------|------|---------------|---|
| | | Min | Typ | Max | | |
| Release voltage | V_{DL+} | 2.52 | 2.70 | 2.88 | V | At power-supply rise |
| Detection voltage | V_{DL-} | 2.42 | 2.60 | 2.78 | V | At power-supply fall |
| Hysteresis width | V_{HYS} | 70 | 100 | — | mV | |
| Power-supply start voltage | V_{off} | — | — | 2.3 | V | |
| Power-supply end voltage | V_{on} | 4.9 | — | — | V | |
| Power-supply voltage change time (at power supply rise) | t_r | 0.3 | — | — | μs | Slope of power supply that reset release signal generates |
| | | — | 3000 | — | μs | Slope of power supply that reset release signal generates within rating (V_{DL+}) |
| Power-supply voltage change time (at power supply fall) | t_f | 300 | — | — | μs | Slope of power supply that reset detection signal generates |
| | | — | 300 | — | μs | Slope of power supply that reset detection signal generates within rating (V_{DL-}) |
| Reset release delay time | t_{d1} | — | — | 400 | μs | |
| Reset detection delay time | t_{d2} | — | — | 30 | μs | |
| Consumption current | I_{LVD} | — | 38 | 50 | μA | Consumption current of low voltage detection circuit only |

MB95130MB Series



(9) Clock Supervisor Clock

($V_{CC} = AV_{CC} = 5\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|------------------------|-----------|-------|-----|-----|---------------|--|
| | | Min | Typ | Max | | |
| Oscillation frequency | f_{OUT} | 50 | 100 | 200 | kHz | |
| Oscillation start time | t_{wk} | — | — | 10 | μs | |
| Current consumption | I_{CSV} | — | 20 | 36 | μA | Current consumption of built-in CR oscillator at 100 kHz oscillation |

MB95130MB Series

5. A/D Converter

(1) A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

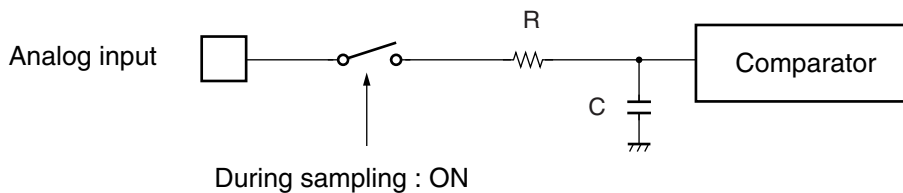
| Parameter | Symbol | Value | | | Unit | Remarks |
|-------------------------------|-----------|----------------------------|----------------------------|----------------------------|---------------|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | -3.0 | — | +3.0 | LSB | |
| Linearity error | | -2.5 | — | +2.5 | LSB | |
| Differential linear error | | -1.9 | — | +1.9 | LSB | |
| Zero transition voltage | V_{OT} | $AV_{SS} - 1.5\text{ LSB}$ | $AV_{SS} + 0.5\text{ LSB}$ | $AV_{SS} + 2.5\text{ LSB}$ | V | |
| Full-scale transition voltage | V_{FST} | $AV_{CC} - 4.5\text{ LSB}$ | $AV_{CC} - 1.5\text{ LSB}$ | $AV_{CC} + 0.5\text{ LSB}$ | V | |
| Compare time | — | 0.9 | — | 16500 | μs | $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$ |
| | | 1.8 | — | 16500 | μs | $4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$ |
| Sampling time | — | 0.6 | — | ∞ | μs | $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$, At external impedance < at 5.4 k Ω |
| | | 1.2 | — | ∞ | μs | $4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$, At external impedance < at 2.4 k Ω |
| Analog input current | I_{AIN} | -0.3 | — | +0.3 | μA | |
| Analog input voltage | V_{AIN} | AV_{SS} | — | AV_{CC} | V | |

(2) Notes on Using A/D Converter

• External impedance of analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• Analog input equivalent circuit

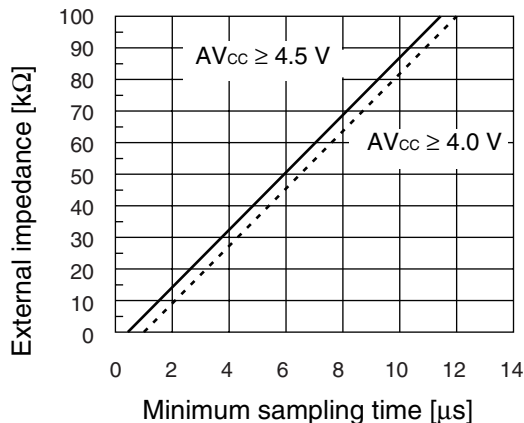


| | R | C |
|---|----------------------|-------------|
| $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$ | 2.0 k Ω (Max) | 16 pF (Max) |
| $4.0\text{ V} \leq AV_{CC} < 4.5\text{ V}$ | 8.2 k Ω (Max) | 16 pF (Max) |

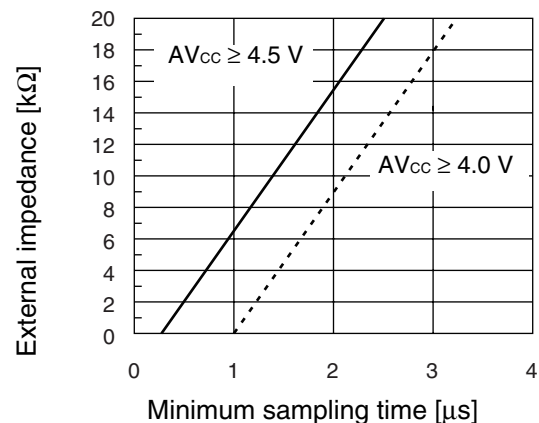
Note : The values are reference values.

• The relationship between external impedance and minimum sampling time

(External impedance = at 0 k Ω to 100 k Ω)



(External impedance = at 0 k Ω to 20 k Ω)



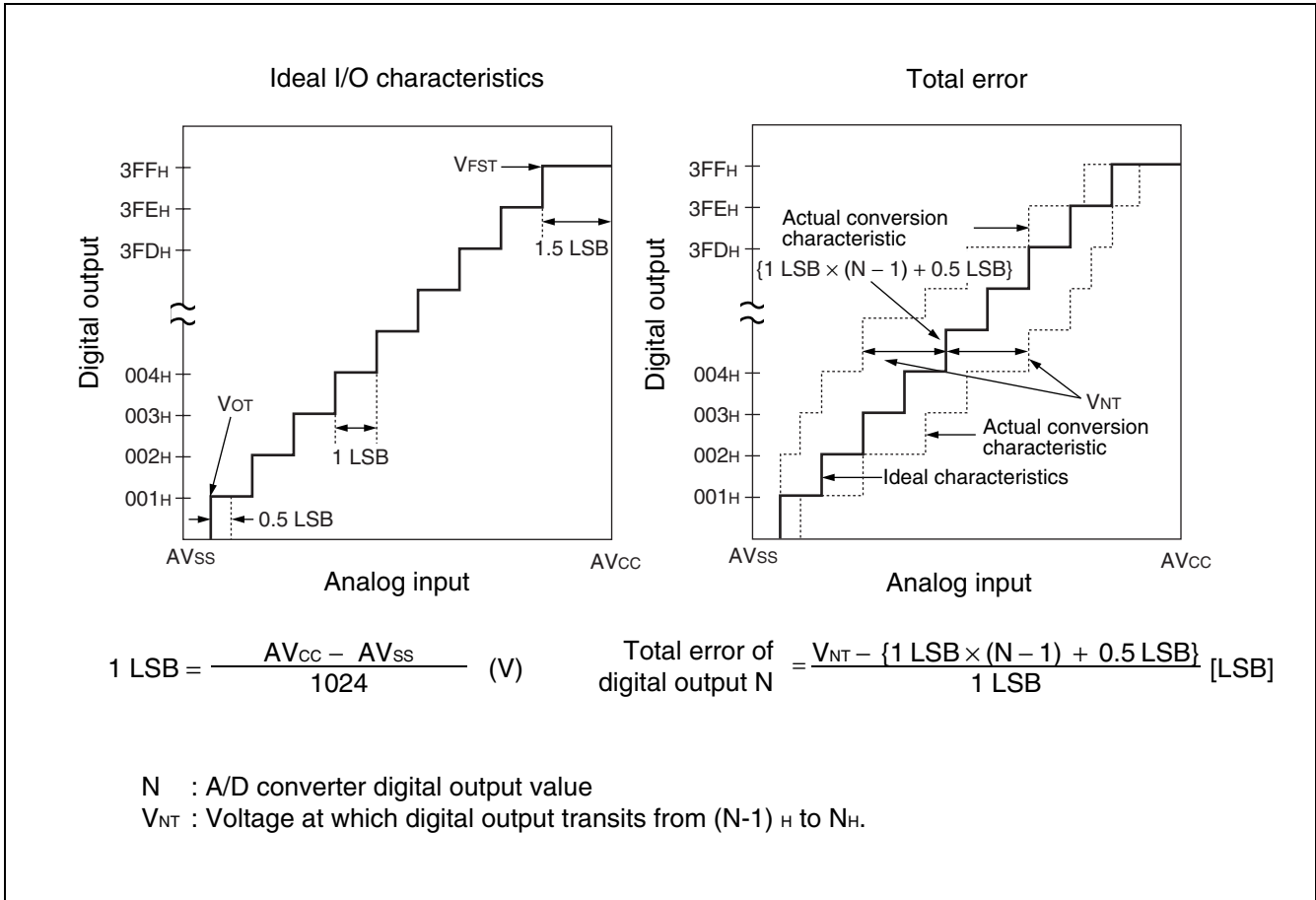
• Errors

As $AV_{CC} - AV_{SSL}$ becomes smaller, values of relative errors grow larger.

MB95130MB Series

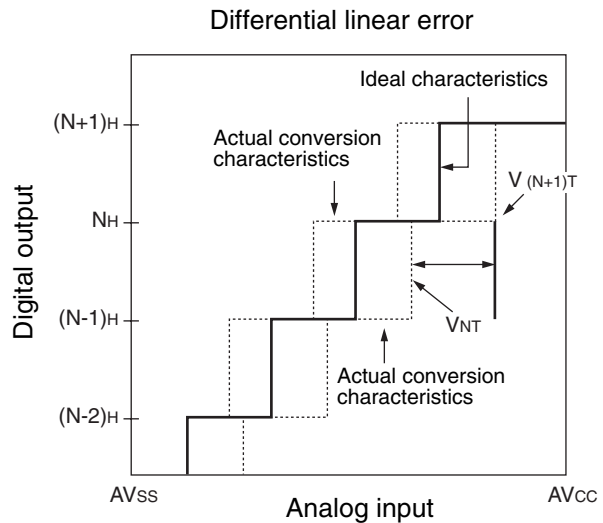
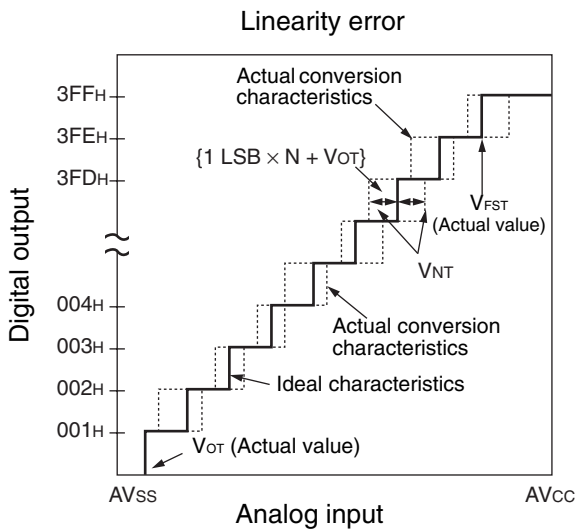
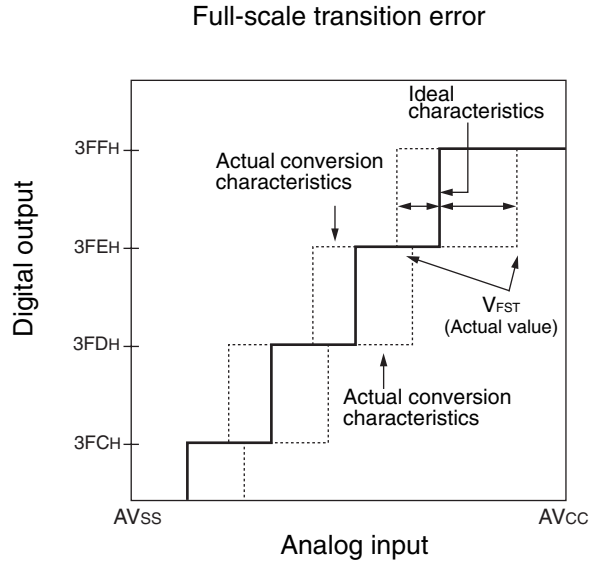
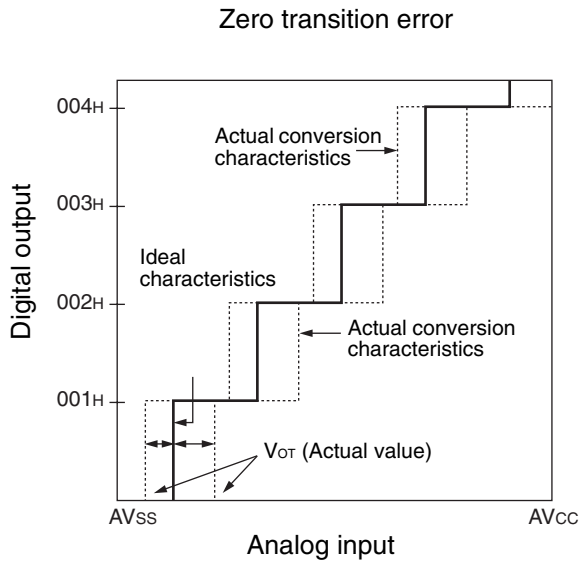
(3) Definition of A/D Converter Terms

- Resolution
The level of analog variation that can be distinguished by the A/D converter.
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
The deviation between the value along a straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device and the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.



(Continued)

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which digital output transits from $(N - 1)_H$ to N_H .

V_{OT} (Ideal value) = $AV_{SS} + 0.5 \text{ LSB [V]}$

V_{FST} (Ideal value) = $AV_{CC} - 1.5 \text{ LSB [V]}$

MB95130MB Series

6. Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|---|------------------|-------------------|--------------------|-------|---|
| | Min | Typ | Max | | |
| Chip erase time | — | 1.0* ¹ | 15.0* ² | s | Excludes 00 _H programming prior erasure. |
| Byte programming time | — | 32 | 3600 | μs | Excludes system-level overhead. |
| Erase/program cycle | 10000 | — | — | cycle | |
| Power supply voltage at erase/ program | 4.5 | — | 5.5 | V | |
| Flash memory data retention time | 20* ³ | — | — | year | Average T _A = +85 °C |

*1 : T_A = + 25 °C, V_{CC} = 5.0 V, 10000 cycles

*2 : T_A = + 85 °C, V_{CC} = 4.5 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTION

| No. | Part number | MB95136MB | MB95F133MBS MB95F133NBS MB95F133JBS MB95F134MBS MB95F134NBS MB95F134JBS MB95F136MBS MB95F136NBS MB95F136JBS | MB95F133MBW MB95F133NBW MB95F133JBW MB95F134MBW MB95F134NBW MB95F134JBW MB95F136MBW MB95F136NBW MB95F136JBW | MB95FV100D-103 |
|-----|---|---|---|---|---|
| | Specifying procedure | Specify when ordering MASK | Setting disabled | Setting disabled | Setting disabled |
| 1 | Clock mode select • Single-system clock mode • Dual-system clock mode | selectable | Single-system clock mode | Dual-system clock mode | Changing by the switch on MCU board |
| 2 | Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset | Specify when ordering MASK | Specified by part number | Specified by part number | Change by the switch on MCU board |
| 3 | Clock supervisor* • With clock supervisor • Without clock supervisor | Specify when ordering MASK | Specified by part number | Specified by part number | Change by the switch on MCU board |
| 4 | Reset output* • With reset output • Without reset output | Specify when ordering MASK | Specified by part number | Specified by part number | MCU board switch set as following ; • With supervisor : Without reset output • Without supervisor : With reset output |
| 5 | Oscillation stabilization wait time | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ | Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$ |

*: Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

MB95130MB Series

| Part number | Clock mode select | Low-voltage detection reset | Clock supervisor | Reset output |
|----------------|-------------------|-----------------------------|------------------|--------------|
| MB95136MB | Single - system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |
| | Dual - system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |
| MB95F133MBS | Single - system | No | No | Yes |
| MB95F133NBS | | Yes | No | Yes |
| MB95F133JBS | | Yes | Yes | No |
| MB95F134MBS | | No | No | Yes |
| MB95F134NBS | | Yes | No | Yes |
| MB95F134JBS | | Yes | Yes | No |
| MB95F136MBS | | No | No | Yes |
| MB95F136NBS | | Yes | No | Yes |
| MB95F136JBS | | Yes | Yes | No |
| MB95F133MBW | | Dual - system | No | No |
| MB95F133NBW | Yes | | No | Yes |
| MB95F133JBW | Yes | | Yes | No |
| MB95F134MBW | No | | No | Yes |
| MB95F134NBW | Yes | | No | Yes |
| MB95F134JBW | Yes | | Yes | No |
| MB95F136MBW | No | | No | Yes |
| MB95F136NBW | Yes | | No | Yes |
| MB95F136JBW | Yes | | Yes | No |
| MB95FV100D-103 | Single - system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |
| | Dual - system | No | No | Yes |
| | | Yes | No | Yes |
| | | Yes | Yes | No |

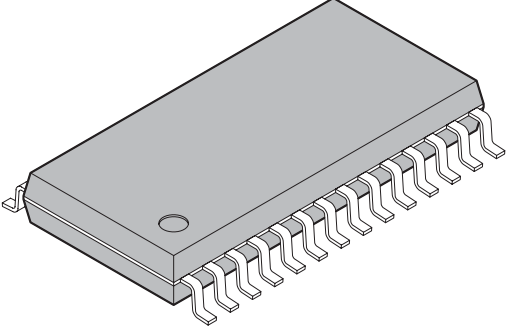
MB95130MB Series

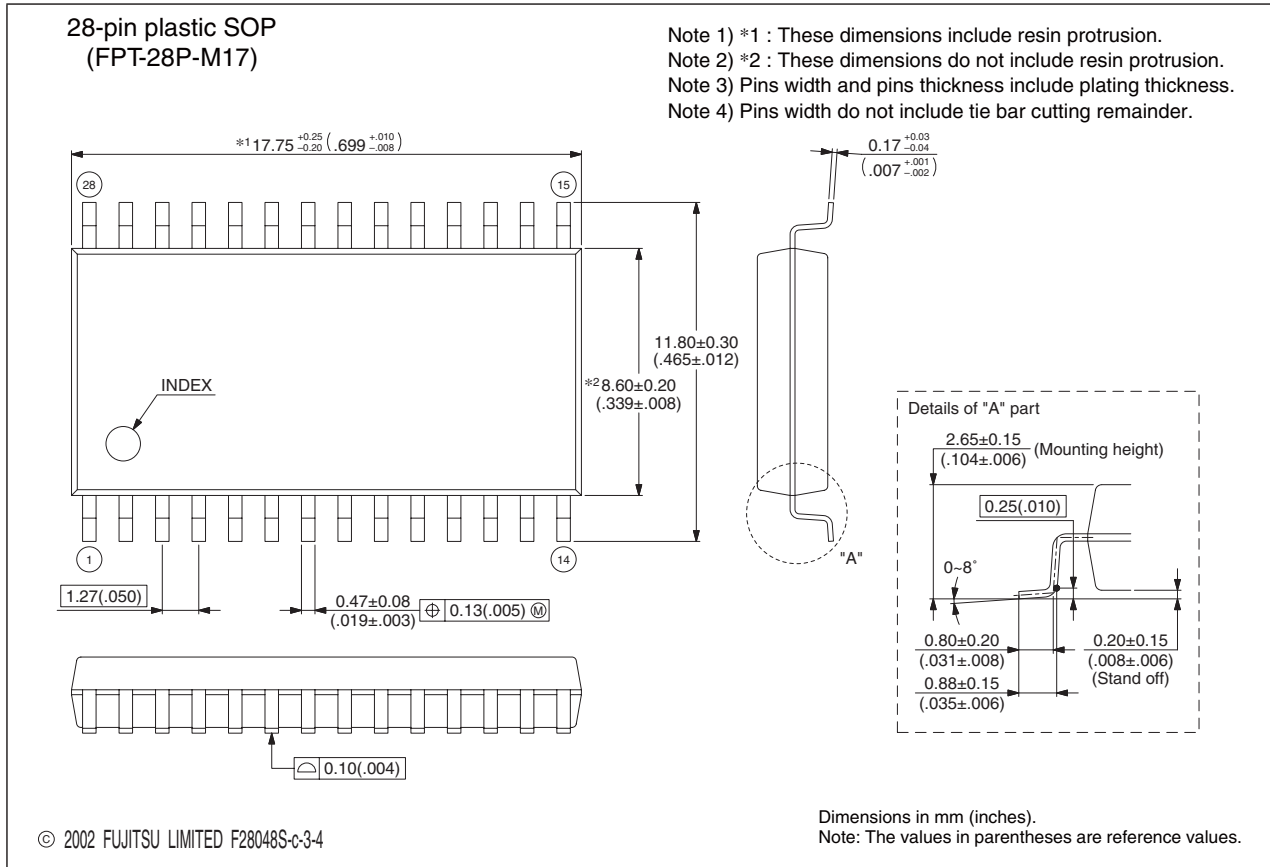
■ ORDERING INFORMATION

| Part number | Package |
|--|--|
| MB95136MBPF MB95F133MBSPF MB95F133NBSPF MB95F133JBSPF MB95F134MBSPF MB95F134NBSPF MB95F134JBSPF MB95F136MBSPF MB95F136NBSPF MB95F136JBSPF MB95F133MBWPF MB95F133NBWPF MB95F133JBWPF MB95F134MBWPF MB95F134NBWPF MB95F134JBWPF MB95F136MBWPF MB95F136NBWPF MB95F136JBWPF | 28-pin plastic SOP (FPT-28P-M17) |
| MB95136MBPFV MB95F133MBSPFV MB95F133NBSPFV MB95F133JBSPFV MB95F134MBSPFV MB95F134NBSPFV MB95F134JBSPFV MB95F136MBSPFV MB95F136NBSPFV MB95F136JBSPFV MB95F133MBWPFV MB95F133NBWPFV MB95F133JBWPFV MB95F134MBWPFV MB95F134NBWPFV MB95F134JBWPFV MB95F136MBWPFV MB95F136NBWPFV MB95F136JBWPFV | 30-pin plastic SSOP (FPT-30P-M02) |
| MB2146-303A (MB95FV100D-103PBT) | MCU board (224-pin plastic PFBGA) (BGA-224P-M08) |

MB95130MB Series

PACKAGE DIMENSION

| | | |
|--|--------------------------------|------------------------|
|  <p>28-pin plastic SOP</p> <p>(FPT-28P-M17)</p> | Lead pitch | 1.27 mm |
| | Package width × package length | 8.6 × 17.75 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 2.80 mm MAX |
| | Weight | 0.82 g |
| | Code (Reference) | P-SOP28-8.6×17.75-1.27 |

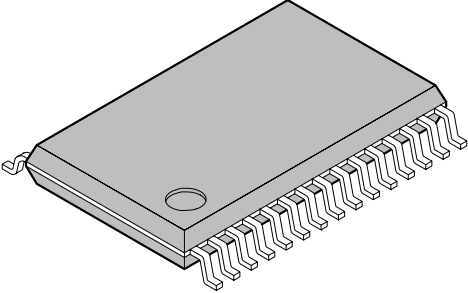


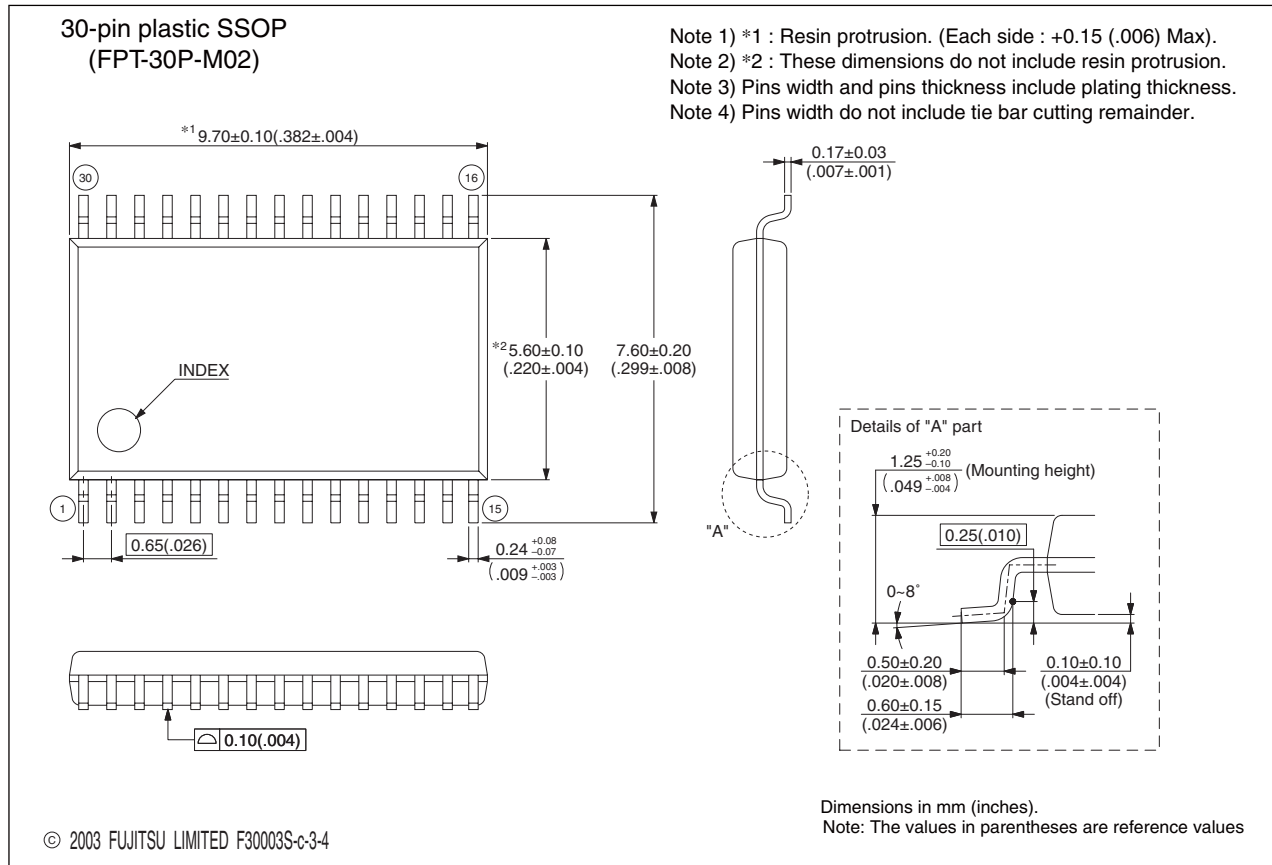
Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpklv.html>

(Continued)

MB95130MB Series

(Continued)

| | | |
|---|--------------------------------|-----------------------|
| <p style="text-align: center;">30-pin plastic SSOP</p>  <p style="text-align: center;">(FPT-30P-M02)</p> | Lead pitch | 0.65 mm |
| | Package width × package length | 5.60 × 9.70 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.45 mm MAX |
| | Code (Reference) | P-SSOP30-5.6×9.7-0.65 |
| | | |



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpkiv.html>

MB95130MB Series

The information for microcontroller supports is shown in the following homepage.
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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