# CY62158EV30 MoBL®

# 8-Mbit (1024K x 8) Static RAM

## Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62158DV30
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA
- Ultra low active power
  - Typical active current: 1.8 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball VFBGA, 44-pin TSOP II and 48-pin TSOP I packages[1]

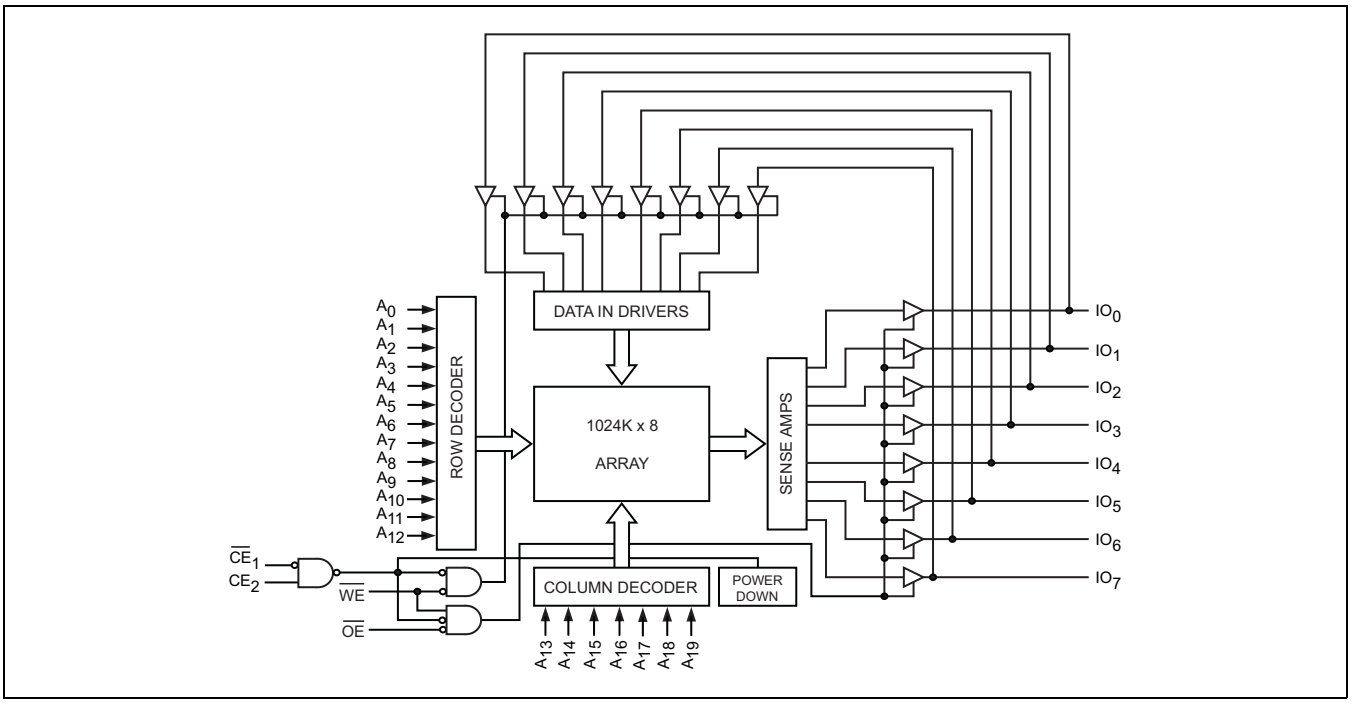
## Functional Description [2]

The CY62158EV30 is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW). The eight input and output pins ($IO_0$ through $IO_7$) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and $CE_2$ HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight IO pins ($IO_0$ through $IO_7$) is then written into the location specified on the address pins ($A_0$ through $A_{19}$).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and $\overline{OE}$ LOW while forcing the $\overline{WE}$ HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins. See the "Truth Table" on page 8 for a complete description of read and write modes.

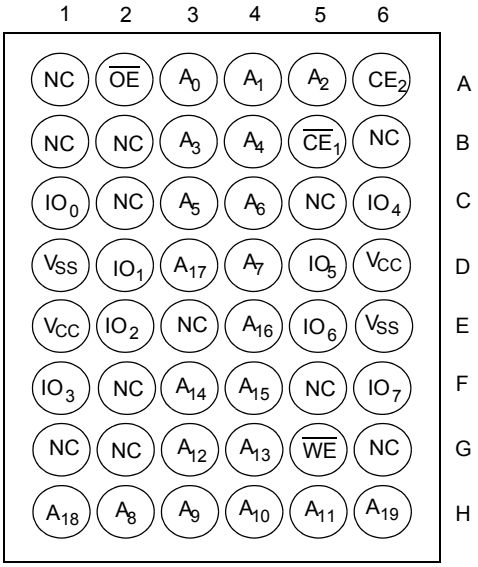
## Logic Block Diagram



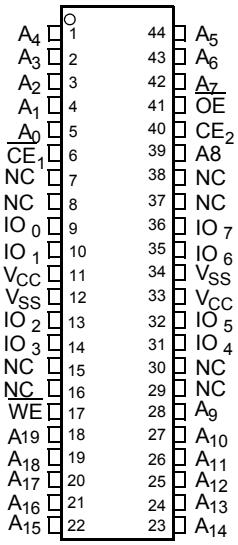

**Notes**
1. For 48 pin TSOP I pin configuration and ordering information, please refer to CY62157EV30 Data sheet.
2. For best practice recommendations, refer to the Cypress application note *"System Design Guidelines"* at http://www.cypress.com.

## Pin Configurations [3]

**48-Ball VFBGA**
**Top View**




**44-Pin TSOPII**
**Top View**




## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$ (mA) | | | | Standby, $I_{SB2}$ (µA) | |
| | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | Min | Typ[4] | Max | | Typ[4] | Max | Typ[4] | Max | Typ[4] | Max |
| CY62158EV30LL | 2.2 | 3.0 | 3.6 | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |

**Notes**
3. NC pins are not connected on the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State[5, 6] ..... –0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[5, 6] ..... –0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)

Latch up Current ..... >200 mA

## Operating Range

| Product | Range | Ambient Temperature ($T_A$) | $V_{CC}$[7] |
|---|---|---|---|
| CY62158EV30LL | Industrial | –40°C to +85°C | 2.2V – 3.6V |

## Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | | 45 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[4] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.1 mA | | 2.0 | | | V |
| | | $I_{OH}$ = –1.0 mA, $V_{CC} \geq$ 2.70V | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | | | | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA, $V_{CC} \geq$ 2.70V | | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = 2.2V to 2.7V | | 1.8 | | $V_{CC}$ + 0.3V | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2.2 | | $V_{CC}$ + 0.3V | V |
| $V_{IIL}$ | Input LOW Voltage | $V_{CC}$ = 2.2V to 2.7V | | –0.3 | | 0.6 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND $\leq V_I \leq V_{CC}$ | | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$, Output Disabled | | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CCmax}$, $I_{OUT}$ = 0 mA, CMOS levels | | 18 | 25 | mA |
| | | f = 1 MHz | | | 1.8 | 3 | mA |
| $I_{SB1}$ | Automatic CE Power down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$ – 0.2V, $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V), f = $f_{max}$ (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC}$ = 3.60V | | | 2 | 8 | µA |
| $I_{SB2}$[8] | Automatic CE Power down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$ – 0.2V or $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, $V_{CC}$ = 3.60V | | | 2 | 8 | µA |

## Capacitance[9]

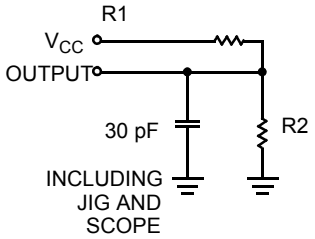
| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

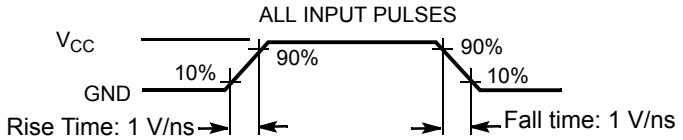
**Notes**
5. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$= $V_{CC}$ + 0.75V for pulse duration less than 20 ns.
7. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC}$(min) and 200 µs wait time after $V_{CC}$ stabilization.
8. Only chip enables ($\overline{CE}_1$ and $CE_2$) must be at CMOS level to meet the $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
9. Tested initially and after any design or process changes that may affect these parameters.

## Thermal Resistance[9]

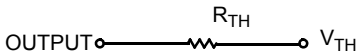
| Parameter | Description | Test Conditions | BGA | TSOP II | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board | 72 | 76.88 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 8.86 | 13.52 | °C/W |

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT

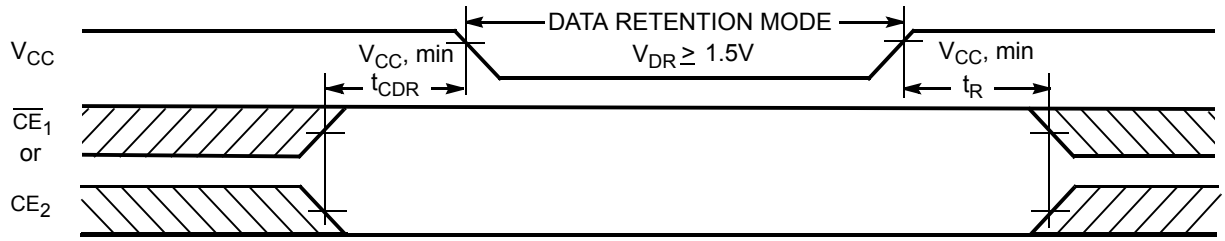



| Parameters | 2.5V | 3.0V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min | Typ[4] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 1.5 | | | V |
| $I_{CCDR}$[8] | Data Retention Current | $V_{CC}$ = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 2 | 5 | µA |
| $t_{CDR}$[9] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$[10] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform




**Note**
10. Full Device AC operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

## Switching Characteristics (Over the Operating Range) [11]

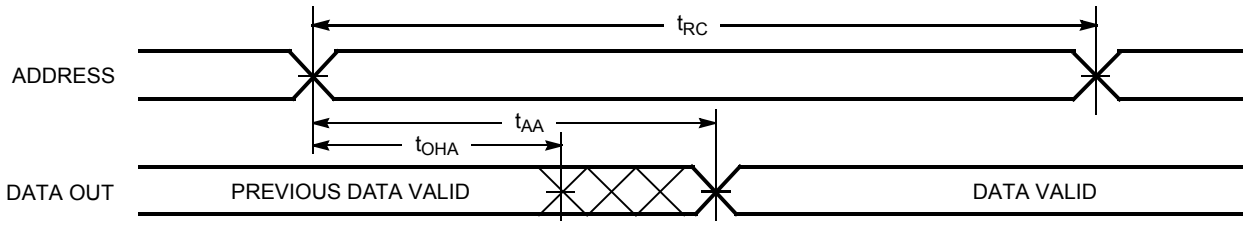
| Parameter | Description | 45 ns | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid | | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [12] | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [12, 13] | | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z [12] | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z [12, 13] | | 18 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH or $CE_2$ LOW to Power Down | | 45 | ns |
| **Write Cycle** [14] | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End | 35 | | ns |
| $t_{AW}$ | Address Setup to Write End | 35 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [12, 13] | | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [12] | 10 | | ns |

**Notes**

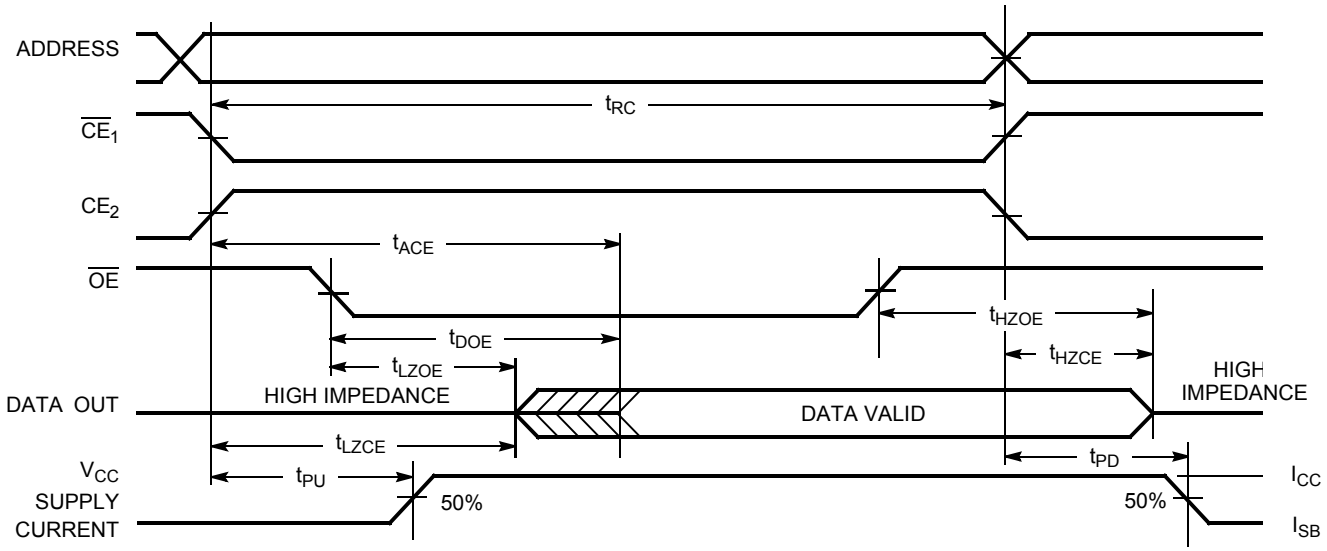
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in "AC Test Loads and Waveforms" on page 4.
12. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
13. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

**Read Cycle No. 1** (Address Transition Controlled)[15, 16]



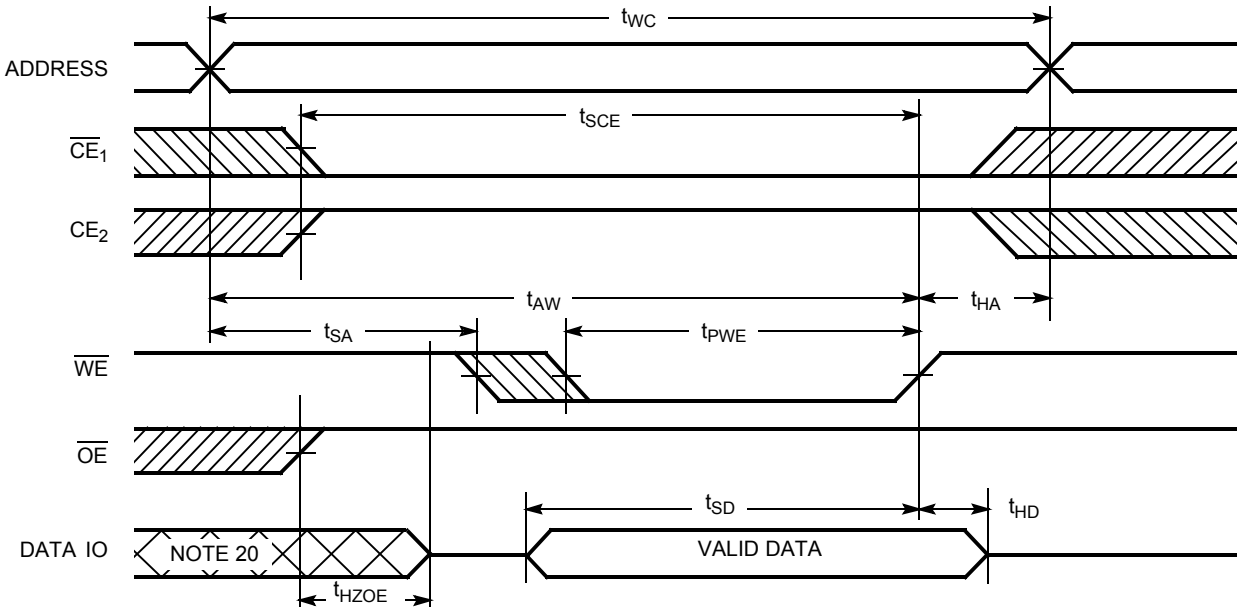

**Read Cycle No. 2** ($\overline{OE}$ Controlled)[16, 17]



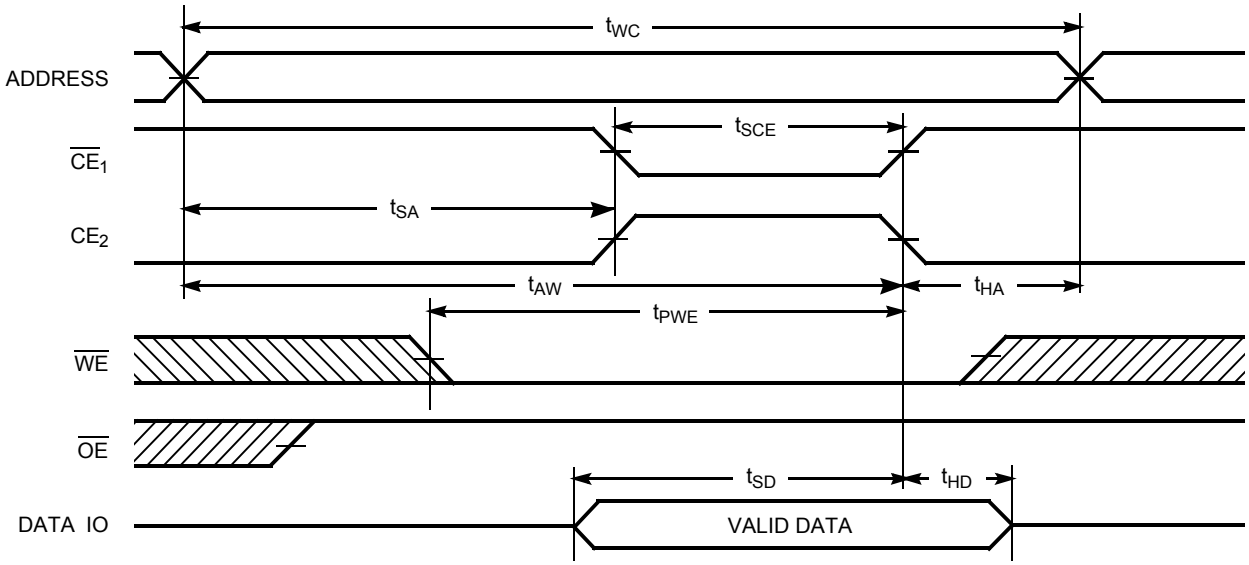

**Notes**
15. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = $V_{IL}$, $CE_2$ = $V_{IH}$.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid before or similar to $\overline{CE_1}$ transition LOW and $CE_2$ transition HIGH.

## Switching Waveforms (continued)

**Write Cycle No. 1** ($\overline{WE}$ Controlled)[14, 18, 19]



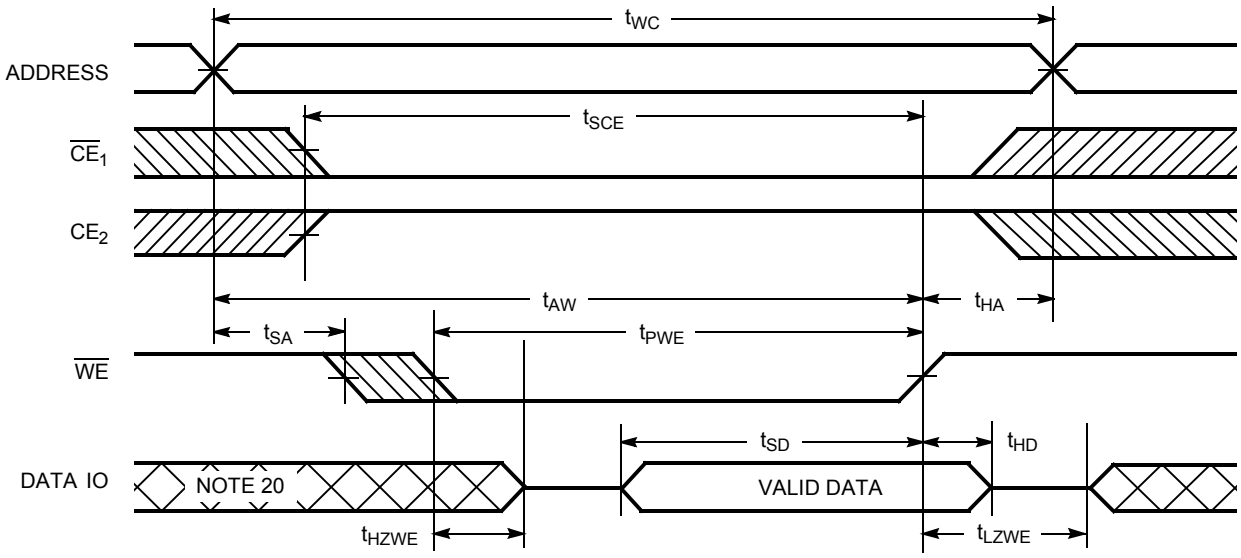

**Write Cycle No. 2** ($\overline{CE}_1$ or $CE_2$ Controlled)[14, 18, 19]




**Notes**
18. Data IO is high impedance if $\overline{OE} = V_{IH}$.
19. If $\overline{CE}_1$ goes HIGH or $CE_2$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
20. During this period, the IOs are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Write Cycle No. 3** ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[19]




## Truth Table

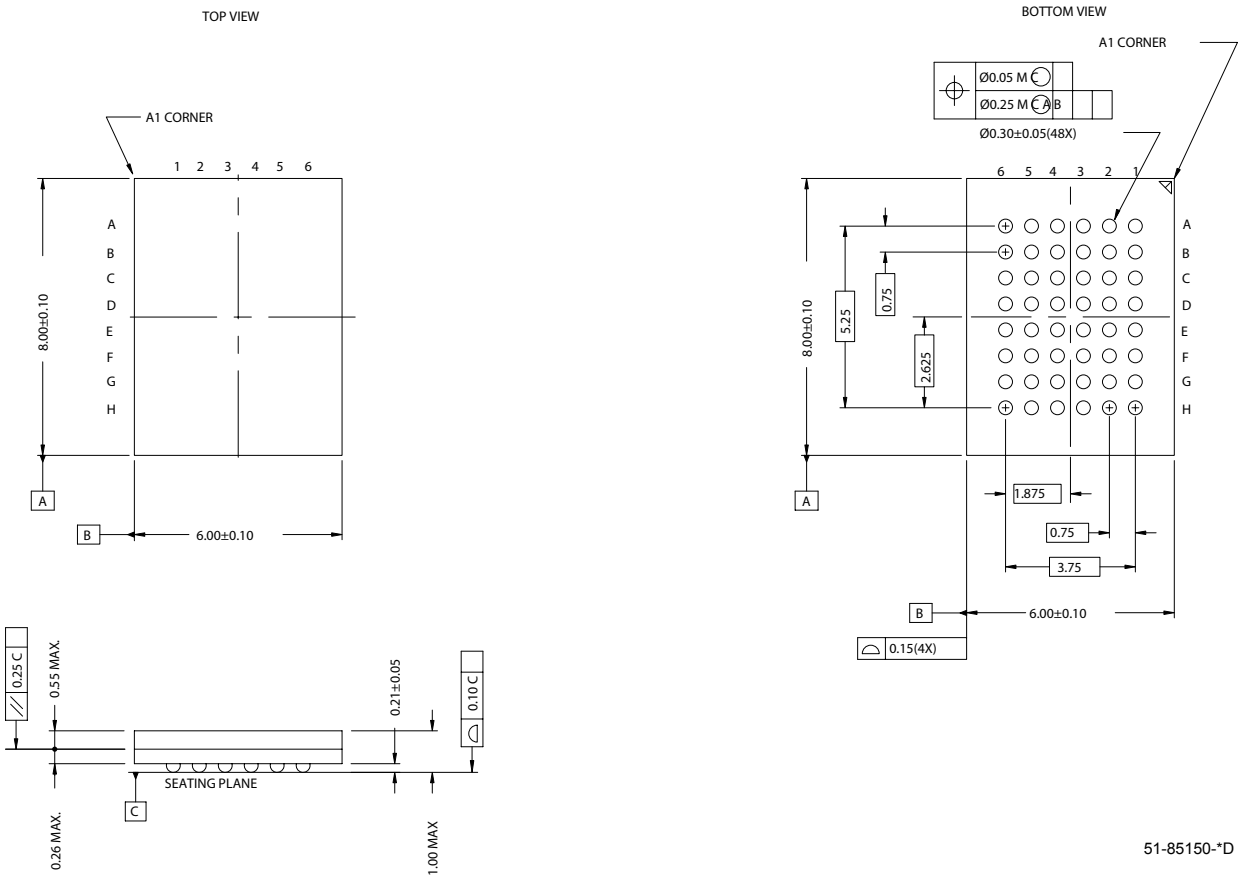
| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Deselect/Power Down | Standby ($I_{SB}$) |
| X | L | X | X | High Z | Deselect/Power Down | Standby ($I_{SB}$) |
| L | H | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | H | H | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | Data in | Write | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62158EV30LL-45BVXI | 51-85150 | 48-ball Very Fine Pitch Ball Grid Array (Pb-free) | Industrial |
| | CY62158EV30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | |

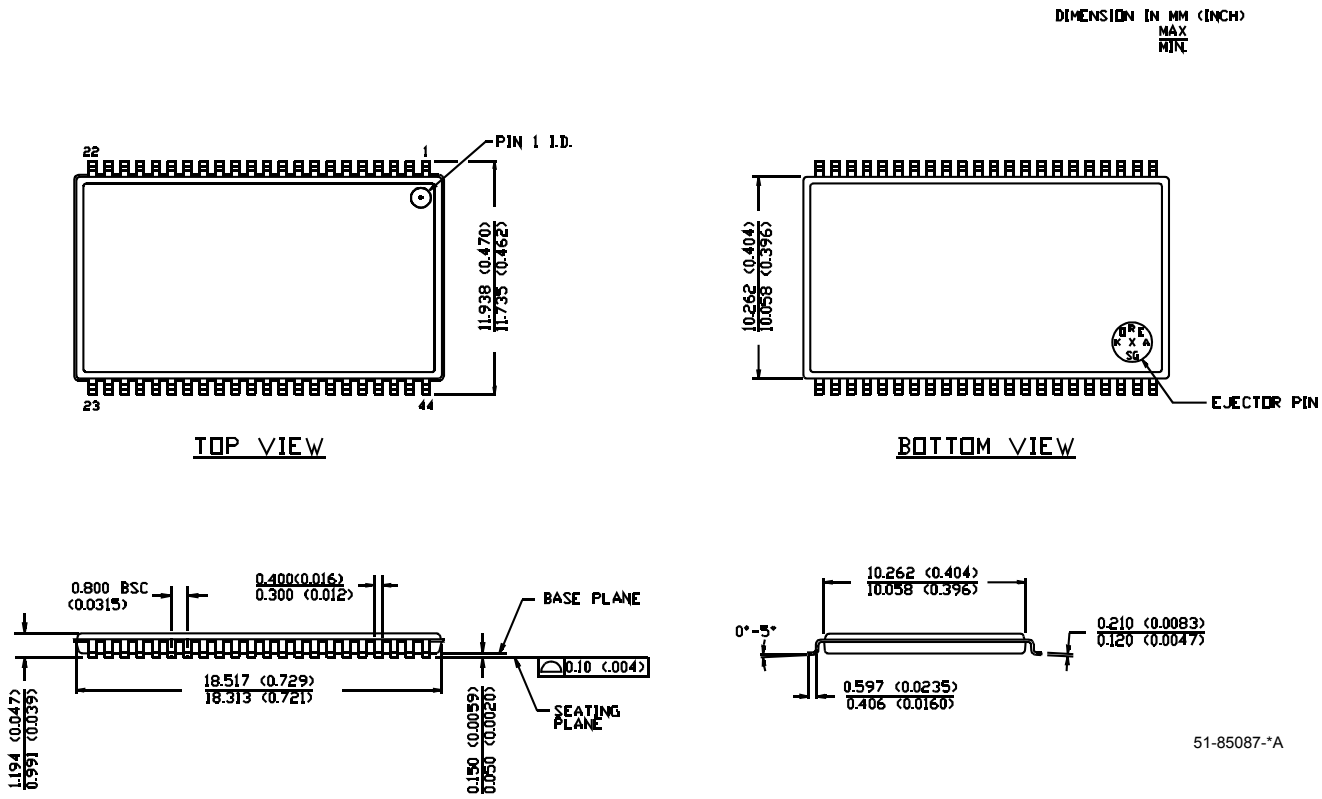
## Package Diagrams

**Figure 1. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150**



## Package Diagrams (continued)

**Figure 2. 44-Pin TSOP II, 51-85087**



## Document History Page

| Document Title: CY62158EV30 MoBL®, 8-Mbit (1024K x 8) Static RAM<br>Document Number: 38-05578 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 270329 | See ECN | PCI | New Data Sheet |
| *A | 291271 | See ECN | SYT | Converted from Advance Information to Preliminary<br>Changed $I_{CCDR}$ from 4 to 4.5 μA |
| *B | 444306 | See ECN | NXR | Converted from Preliminary to Final.<br>Removed 35 ns speed bin<br>Removed “L” bin.<br>Removed 44 pin TSOP II package<br>Included 48 pin TSOP I package<br>Changed the $I_{CC}$ Typ value from 16 mA to 18 mA and $I_{CC}$ max value from 28 mA to 25 mA for test condition f = fax = $1/t_{RC}$.<br>Changed the $I_{CC}$ max value from 2.3 mA to 3 mA for test condition f = 1MHz.<br>Changed the $I_{SB1}$ and $I_{SB2}$ max value from 4.5 μA to 8 μA and Typ value from 0.9 μA to 2 μA respectively.<br>Updated Thermal Resistance table<br>Changed Test Load Capacitance from 50 pF to 30 pF.<br>Added Typ value for $I_{CCDR}$ .<br>Changed the $I_{CCDR}$ max value from 4.5 μA to 5 μA<br>Corrected $t_R$ in Data Retention Characteristics from 100 μs to $t_{RC}$ ns<br>Changed $t_{LZOE}$ from 3 to 5<br>Changed $t_{LZCE}$ from 6 to 10<br>Changed $t_{HZCE}$ from 22 to 18<br>Changed $t_{PWE}$ from 30 to 35<br>Changed $t_{SD}$ from 22 to 25<br>Changed $t_{LZWE}$ from 6 to 10<br>Updated the ordering Information and replaced the Package Name column with Package Diagram. |
| *C | 467052 | See ECN | NXR | Included 44 pin TSOP II package in Product Offering.<br>Removed TSOP I package; Added reference to CY62157EV30 TSOP I<br>Updated the ordering Information table |
| *D | 1015643 | See ECN | VKN | Added footnote #8 related to $I_{SB2}$ and $I_{CCDR}$ |