Factory Programmable Quad PLL Clock Generator with VCXO

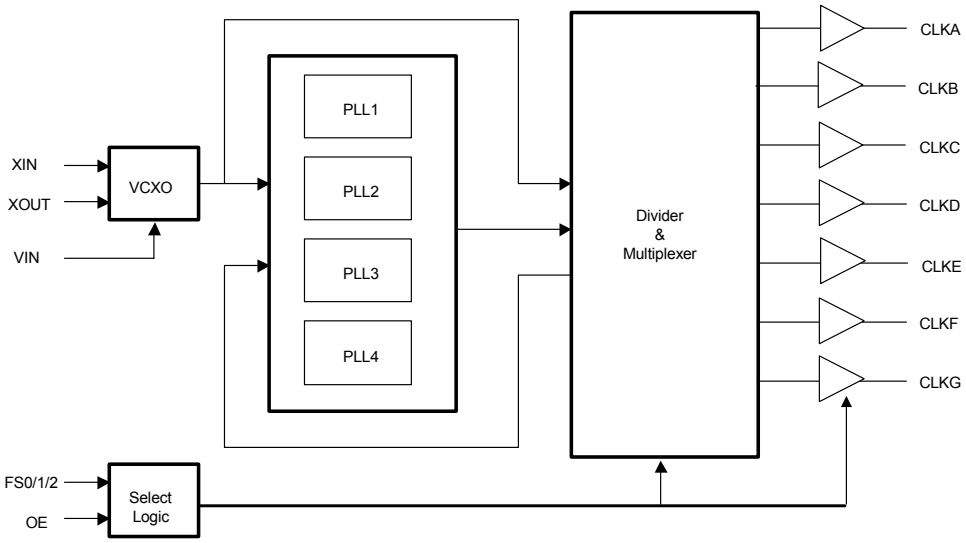
Features

- Fully integrated phase-locked loops (PLLs)
- Selectable Output Frequency
- Programmable Output Frequencies
- Output Frequency Range of 5–166 MHz
- Input Frequency Range
  - — Crystal: 10–30 MHz
  - — External Reference: 1–100 MHz
- Analog VCXO
- 16-/20-pin TSSOP packages
- 3.3V operation

Benefits

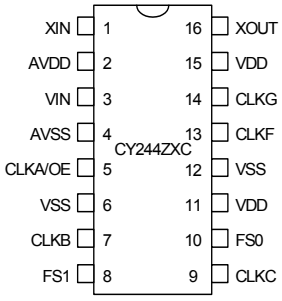
- Meets most Digital Set Top Box, DVD Recorder and DTV application requirements
- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Integration eliminates the need for external loop filter components
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Complete VCXO solution with ±120 ppm (minimum pull range)

Block Diagram

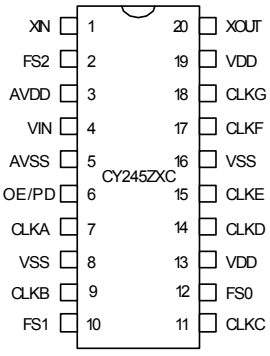


Pin Configuration

16-Pin TSSOP



20-Pin TSSOP



Pin Description

Pin Name	Pin Number		Pin Description
	16-pin TSSOP	20-pin TSSOP	
XIN	1	1	Crystal Input or Reference Clock Input
XOUT	16	20	Crystal Output (No connect if external clock is used)
CLKA	5[1]	7	Clock Output
CLKB	7	9	Clock Output
CLKC	9	11	Clock Output
CLKD	N/A	14	Clock Output
CLKE	N/A	15	Clock Output
CLKF	13	17	Clock Output
CLKG	14	18	Clock Output
FS0	10	12	Frequency Select 0
FS1	8	10	Frequency Select 1
FS2	N/A	2	Frequency Select 2
OE/PD	5[1]	6	Output Enable Control/Power Down
VIN	3	4	Analog Control Input for VCXO
VDD	11,15	13,19	Voltage Supply
VSS	6,12	8,16	Ground
AVDD	2	3	Analog Voltage Supply
AVSS	4	5	Analog Ground

General Description

The CY24xZXC family of devices has an Analog VCXO (Voltage Controlled Crystal Oscillator), 4 PLLs, up to 7 clock outputs, and frequency selection capabilities. The frequency selects do not modify any PLL frequency. Instead, they allow the user to choose between up to 8 different output divider selections depending on the clock and package configuration. This is illustrated in Frequency Selection tables 1 and 2.

There is one programmable OE/PDWN. The OE/PDWN pin can be programmed as either an output enable pin or a power down pin. The OE function can be programmed to disable a selected set of outputs when low, leaving the remaining outputs running. Full chip power-down will disable all outputs as well as the PLLs and most of the active circuitry when low.

Factory-Programmable CY24xZXC

Factory programming is available for high or low volume manufacturing by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number will be used for additional sample requests and production orders. Please refer to the CY223388/89/91 data sheet for up to 8 clock outputs and compatibility with most SMD type crystals.

PLLs

The advantage of having 4 PLLs is that a single device can generate up to 4 independent frequencies from a single crystal. Generally a design may require up to 4 oscillators to accomplish what could be done with a single CY24xZXC.

Each PLL is independent and can be configured to generate a VCO (Voltage Controlled Oscillator) frequency between 62.5 MHz and 250 MHz. Each PLL can then in turn be divided down with post dividers to generate the clock output frequency of the user's choice. The output divider allows each clock output to be divided by 1,2,3,4,6,8,9,10,12,15. The PLL maximum is reduced to 166 MHz in divide by 1 mode due to output buffer limitations.

Outputs that allow frequency switching perform the transition free of glitches. A glitch is defined as a high or low time shorter than half the smaller of the two periods being switched between. Extended low time (even many cycles in duration) is acceptable. Please refer to *Figure 5*.

In order to minimize PPM (Parts Per Million) error on the clock outputs, a user should try and choose a crystal reference frequency that is a common multiple of the desired PLL frequencies. While this would be the ideal situation, this is not always the case and the PLLs have high resolution counters internally to help minimize frequency deviation from the desired frequency.

PLL VCO frequencies are generated by the following equation: $F_{VCO} = F_{REF} * (P / Q)$

Where F_{REF} is the reference input frequency, P is the PLL feedback divider and Q is the reference input divider. A PLL is a feedback system where the VCO frequency divided by P and reference frequency divided by Q are constantly being compared and the VCO frequency is adjusted to achieve a locked state. *Figure 1* is a simplified drawing of a PLL.

Note:
1. Pin 5 16-pin TSSOP (choice between clock output or OE/PD)

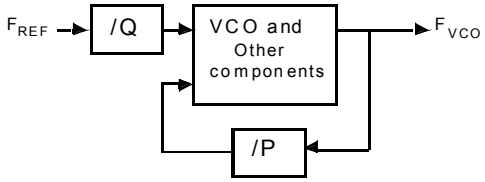


Figure 1. Simplified PLL

Frequency Select Pin Operation

Table 1. CY244ZXC 16-pin TSSOP

Output Signal	Frequency Selection Lines
CLOCK B & CLOCK C	FS1 FS0
CLOCK A & CLOCK F	FS0
CLOCK G	FIXED

Table 2. CY245ZXC 20-pin TSSOP

Output Signal	Frequency Selection Lines
CLOCK C	FS2 FS1 FS0
CLOCK B & CLOCK D	FS1 FS0
CLOCK A, CLOCK E, & CLOCK F	FS0
CLOCK G	FIXED

Analog VCXO

There are three programmable reference operating modes for the CY24xZXC family of devices. The first mode utilizes an external pullable crystal and incorporates an internal Analog VCXO.

The second mode configures the internal crystal oscillator to accept an external driven reference source from 1 to 100 MHz. The input capacitance on the XIN pin when driven in this mode is typically 15pF.

The third mode disables the VCXO input control and sets the internal oscillator to a fixed frequency operation. The load capacitance seen by the external crystal when connected to pins XIN and XOUT is typically equal to 10pF.

One of the key components to the CY24xZXC family of devices is the analog VCXO. The VCXO is used to “pull” the reference crystal higher or lower in order to lock the system frequency to an external source. This is ideal for applications where the output frequency needs to track along with an external reference frequency that is constantly shifting.

The VCXO is completely analog, so there is infinite resolution on the VCXO pull curve. The Analog to Digital Converter steps that are normally associated with a digital VCXO input are not present in this device. A special pullable crystal must be used in order to have adequate VCXO pull range. Pullable Crystal specifications are included in this data sheet.

Please contact the local Cypress Field Application Engineer (FAE) or sales representative for pullable crystal recommendations outside of the standard industry frequencies given in the Pullable Crystal Specifications.

VCXO Profile

Figure 2 shows an example of what a VCXO profile looks like. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This has the effect of moving the PPM from a negative to positive offset.

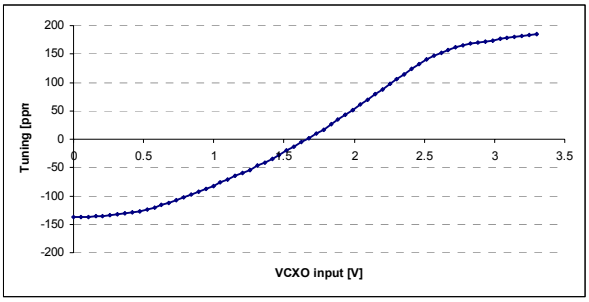


Figure 2. VCXO Profile

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD}/AV_{DD}/V_{DDL}$	Core Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-Functional	–65	+125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	Volts
UL-94	Flammability Rating	V-0 @1/8 in.	–	10	ppm
MSL	Moisture Sensitivity Level				
		16 and 20 pin TSSOP	1		

Pullable Crystal Specifications[2, 4]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	10 to 30 MHz Crystal AT-Cut	Parallel resonance, Fundamental mode	See Note 4			
C_{LNOM}	Nominal load capacitance	C_{LNOM} =14 pF (0 ppm)	13.5	14	14.5	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode (CL = Series)	–	–	25	Ω
DL	Crystal drive level	No external series resistor assumed	–	–	500	µW
C_0[3]	Crystal shunt capacitance		–	–	7	pF
C_1[3]	Crystal motional capacitance		14.4	18	21.6	fF
F_{3SEPHI}[4]	Third overtone separation from 3*F_{NOM}	Mechanical Third (High side of 3*F_{NOM})	380	–	–	ppm
F_{3SEPLO}[4]	Third overtone separation from 3*F_{NOM}	Mechanical Third (Low side of 3*F_{NOM})	–	–	–170	ppm
C_0/C_1	Ratio of shunt to motional capacitance		–	–	250	

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD}/AV_{DD}/V_{DDL}$	Operating Voltage	3.0	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD}s reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Parameters

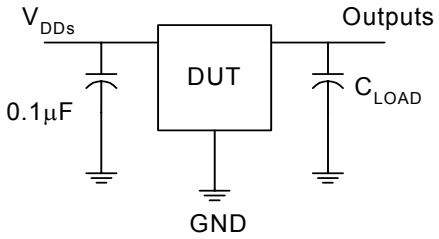
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}[5]	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V	–	12	–	mA
I_{OL}[5]	Output Low Current	V_{OL} = 0.5, V_{DD} = 3.3V	–	12	–	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$, excluding Vin, Xin	–	5	10	µA
I_{IL}	Input Low Current	V_{IL} = 0V, excluding Vin, Xin	–	5	10	µA
V_{IH}	Input High Voltage	FS0/1/2 OE input CMOS levels	0.7xA_{VDD}	–	–	V
V_{IL}	Input Low Voltage	FS0/1/2 OE input CMOS levels	–	–	0.3xA_{VDD}	V
V_{VCXO}	VIN Input Range		0	–	A_{VDD}	V
C_{IN}	Input Capacitance	FS0/1/2 and OE Pins only	–	–	7	pF
I_{VDD}	Supply Current	$V_{DD}/AV_{DD}/V_{DDL}$ Current	–	85	–	mA
C_{INXIN}	Input Capacitance at XIN	VCXO Disabled External Reference	–	15	–	pF
Crystal Load	Crystal Load Capacitance	VCXO Disabled Fixed Freq. Crystal	–	10	–	pF

Notes:
2. Device operates to the following specs, which are guaranteed by design.
3. Increased tolerance available from pull range less than ±120 ppm.
4. ECX-5953 Series crystal orderable from Ecliptek Corporation. Please refer to the CY22388/89/91 data sheet for compatibility with most SMD type crystals.
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

AC Parameters

Parameter[4]	Description	Conditions	Min.	Typ.	Max.	Units
1/t1	Output Frequency	PLL $_{minmax}$/Divider$_{maximum}$	4.2	–	166	MHz
DC1[6]	Output Duty Cycle	Duty Cycle is defined in *Figure 3*; t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is ≤ 125MHz)	45	50	55	%
DC2	Output Duty Cycle	Duty Cycle is defined in *Figure 3*; t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is > 125MHz)	40	50	60	%
DC_{REFOUT}	Reference Output Duty Cycle	Duty Cycle is defined in *Figure 3*; t_2/t_1, 50% of V_{DD} (XIN Duty Cycle = 45/55%)	40	50	60	%
ER	Rising Edge Rate	Output Clock Edge Rate. Measured from 20% to 80% of V_{DD}. C_{LOAD} = 15 pF. See *Figure 4*.	0.8	1.2	–	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate. Measured from 80% to 20% of V_{DD}. C_{LOAD} = 15pF See *Figure 4*.	0.8	1.2	–	V/ns
T_9[7]	Clock Jitter	Period Jitter	–	±250	–	ps
T_{10}	PLL Lock Time		–	1	5	ms
$f_{\Delta XO}$	VCXO Crystal Pull Range	*Using Crystal specified in "Pullable Crystal Specifications" table. Nominal Crystal Frequency Input assumed (0ppm)@25°C and 3.3V*	±120	–	–	ppm

Test and Measurement Set-up



Voltage and Timing Definitions

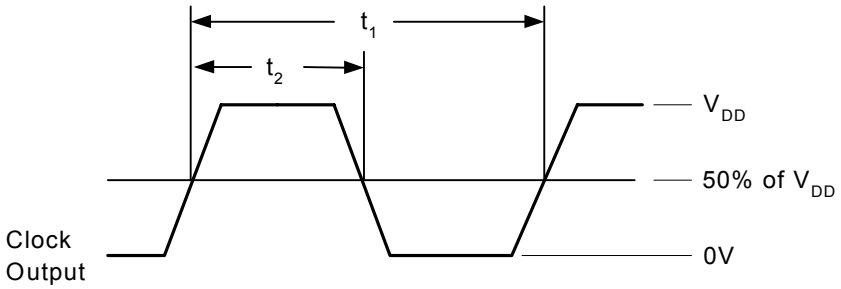


Figure 3. Duty Cycle Definition

Note:
6. Excluding any output configured as a reference.
7. Jitter measurement will vary. Actually jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, and device programming.

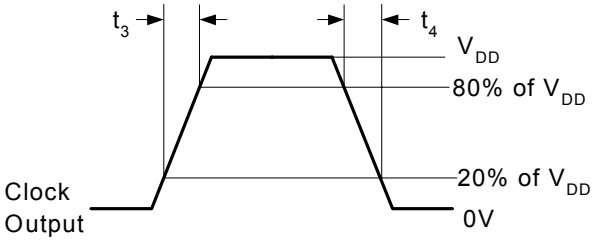


Figure 4. ER = (0.6 × V_{DD})/t3, EF = (0.6 × V_{DD})/t4

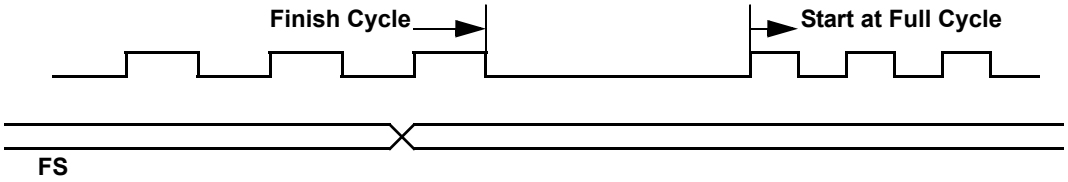


Figure 5. FS Controlled Clock Output

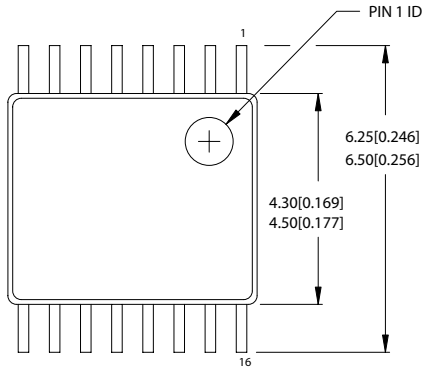
Ordering Information

Part Number[8]	Type	Production Flow
Lead-free		
CY244ZXC-XXX	16-pin TSSOP	Commercial, 0°C to +70°C
CY244ZXC-XXXT	16-pin TSSOP - Tape and Reel	Commercial, 0°C to +70°C
CY245ZXC-XXX	20-pin TSSOP	Commercial, 0°C to +70°C
CY245ZXC-XXXT	20-pin TSSOP - Tape and Reel	Commercial, 0°C to +70°C

Note:
8. The CY244ZXC-xxx, CY245ZXC-xxx are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Drawing and Dimensions

16-lead TSSOP 4.40 mm Body Z16.173

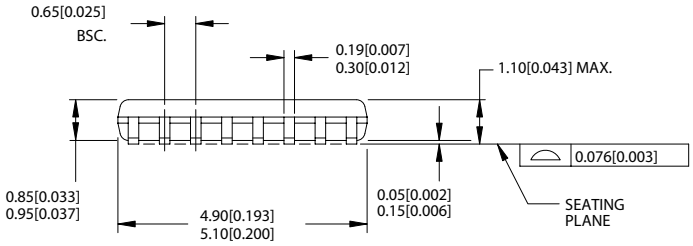


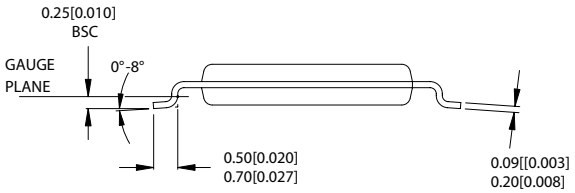
DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.





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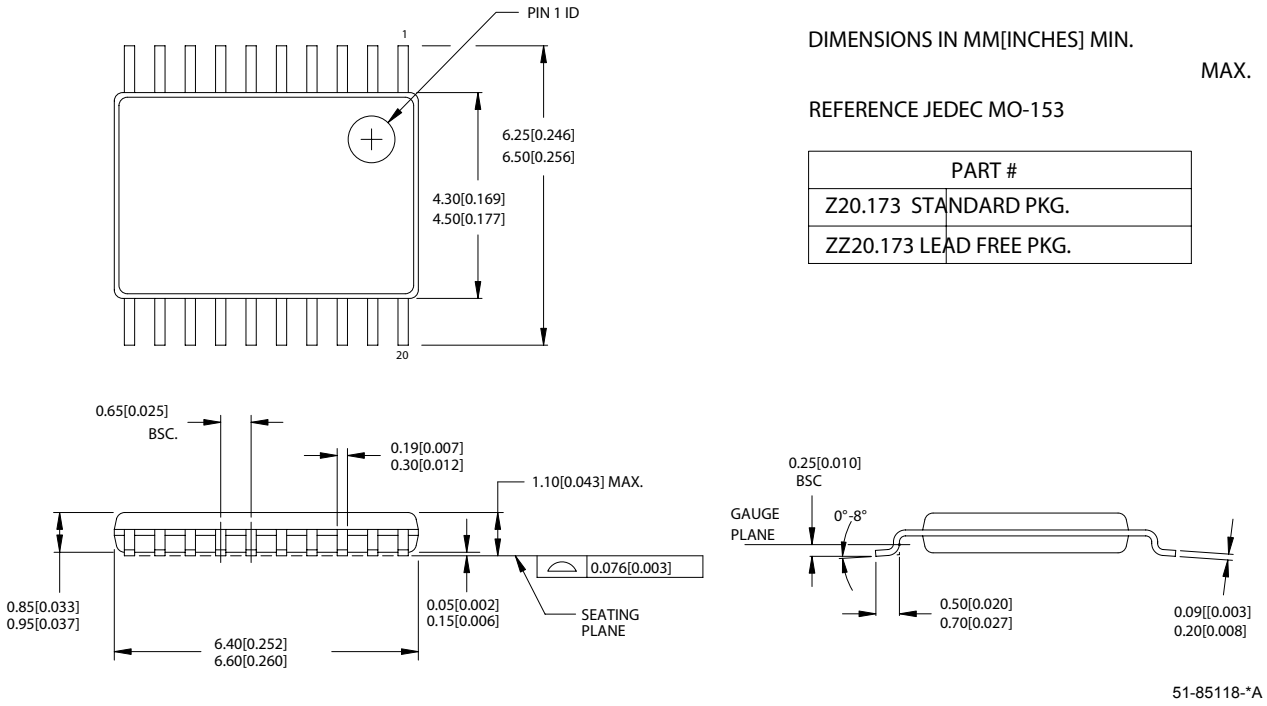
Package Drawing and Dimensions (continued)

20-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z20



DIMENSIONS IN MM[INCHES] MIN.

MAX.

REFERENCE JEDEC MO-153

PART #
Z20.173 STANDARD PKG.
ZZ20.173 LEAD FREE PKG.

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Document History Page

Document Title: CY244/45ZXC Factory Programmable Quad PLL Clock Generator with VCXO Document Number: 38-07748				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	330814	See ECN	RGL	New data sheet