

### FEATURES

- AD5544 16-bit resolution
- AD5554 14-bit resolution
- 2 mA full-scale current  $\pm 20\%$ , with  $V_{REF} = \pm 10\text{ V}$
- 2  $\mu\text{s}$  settling time
- $V_{SS}$  BIAS for zero-scale error reduction @ temp
- midscale or zero-scale reset
- Four separate, 4-Q multiplying reference inputs
- SPI<sup>®</sup>-compatible 3-wire interface
- Double buffered registers enable
- Simultaneous multichannel change
- Internal power ON reset
- Compact SSOP-28 package

### APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration

### GENERAL DESCRIPTION

The AD5544/AD5554 quad, 16-/14-bit, current-output, digital to-analog converters are designed to operate from a single 5 V supply.

The applied external reference input voltage ( $V_{REF}$ ) determines the full-scale output current. Integrated feedback resistors ( $R_{FB}$ ) provide temperature-tracking, full-scale voltage outputs when combined with an external I-to-V precision amplifier.

A double-buffered serial-data interface offers high speed, 3-wire, SPI- and microcontroller-compatible inputs using serial-data-in (SDI), a chip-select ( $\overline{CS}$ ), and clock (CLK) signals. In addition, a serial-data-out pin (SDO) allows for daisy-chaining when multiple packages are used. A common, level-sensitive, load-DAC strobe (LDAC) input allows the simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power ON reset forces the output voltage to zero at system turn ON. An MSB pin allows system reset assertion (RS) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

The AD5544/AD5554 are packaged in the compact SSOP-28.

#### Rev. A

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### FUNCTIONAL BLOCK DIAGRAM

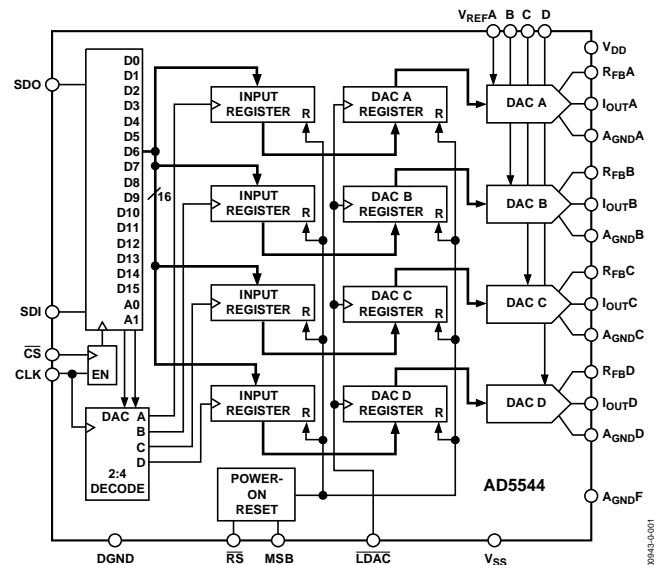


Figure 1.

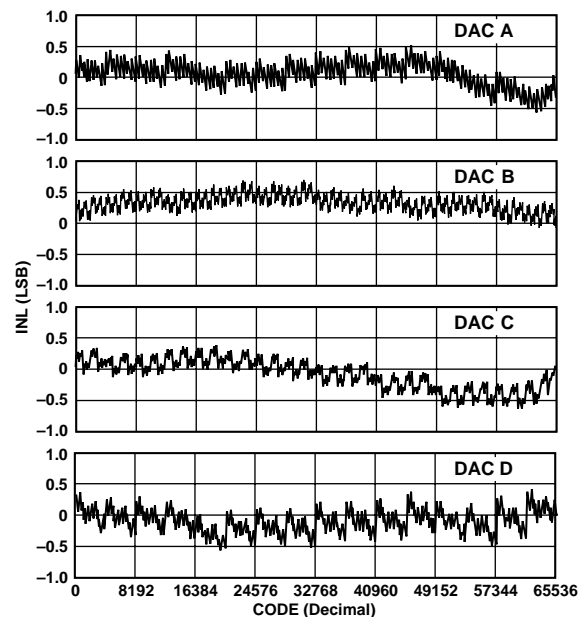


Figure 2. AD5544 INL vs. Code Plot ( $T_A = 25^\circ\text{C}$ )

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## REVISION HISTORY

### 12/04—Rev. 0 to Rev. A

Updated Format .....	Universal
Change to Electrical Characteristics Tables .....	4
Change to Pin Description Table.....	10
Addition of Power Supply Sequence Section .....	19
Addition of Layout and Power Supply Bypassing Section .....	19
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### 4/00—Revision 0: Initial Version

# SPECIFICATIONS

## AD5544 ELECTRICAL CHARACTERISTICS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $I_{OUTX}$  = virtual GND,  $A_{GNDX} = 0\text{ V}$ ,  $V_{REFA, B, C, D} = 10\text{ V}$ ,  $T_A$  = full operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>STATIC PERFORMANCE<sup>1</sup></b>						
Resolution	N	1 LSB = $V_{REF}/2^{16} = 153\text{ }\mu\text{V}$ when $V_{REF} = 10\text{ V}$			16	Bits
Relative Accuracy	INL				$\pm 4$	LSB
Differential Nonlinearity	DNL				$\pm 1.5$	LSB
Output Leakage Current	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = 25^\circ\text{C}$			10	nA
	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = T_A\text{ max}$			20	nA
Full-Scale Gain Error	$G_{FSE}$	Data = FFFF <sub>H</sub>		$\pm 0.75$	$\pm 3$	mV
Full-Scale Tempco <sup>2</sup>	$TCV_{FS}$			1		ppm/ $^\circ\text{C}$
Feedback Resistor	$R_{FBX}$	$V_{DD} = 5\text{ V}$	4	6	8	k $\Omega$
<b>REFERENCE INPUT</b>						
$V_{REFX}$ Range	$V_{REFX}$		-15		+15	V
Input Resistance	$R_{REFX}$		4	6	8	k $\Omega$
Input Resistance Match	$R_{REFX}$	Channel-to-channel		1		%
Input Capacitance <sup>2</sup>	$C_{REFX}$			5		pF
<b>ANALOG OUTPUT</b>						
Output Current	$I_{OUTX}$	Data = FFFF <sub>H</sub>	1.25		2.5	mA
Output Capacitance <sup>2</sup>	$C_{OUTX}$	Code-dependent		80		pF
<b>LOGIC INPUT AND OUTPUT</b>						
Logic Input Low Voltage	$V_{IL}$				0.8	V
Logic Input High Voltage	$V_{IH}$		2.4			V
Input Leakage Current	$I_{IL}$				1	$\mu\text{A}$
Input Capacitance <sup>2</sup>	$C_{IL}$				10	pF
Logic Output Low Voltage	$V_{OL}$	$I_{OL} = 1.6\text{ mA}$			0.4	V
Logic Output High Voltage	$V_{OH}$	$I_{OH} = 100\text{ }\mu\text{A}$	4			V
<b>INTERFACE TIMING<sup>2, 3</sup></b>						
Clock Width High	$t_{CH}$		25			ns
Clock Width Low	$t_{CL}$		25			ns
$\overline{CS}$ to Clock Setup	$t_{CSS}$		0			ns
Clock to $\overline{CS}$ Hold	$t_{CSH}$		25			ns
Clock to SDO Prop Delay	$t_{PD}$		2		20	ns
Load DAC Pulse Width	$t_{LDAC}$		25			ns
Data Setup	$t_{DS}$		20			ns
Data Hold	$t_{DH}$		20			ns
Load Setup	$t_{LDS}$		5			ns
Load Hold	$t_{LDH}$		25			ns
<b>SUPPLY CHARACTERISTICS</b>						
Power Supply Range	$V_{DD\text{ RANGE}}$		4.5		5.5	V
Positive Supply Current	$I_{DD}$	Logic inputs = 0 V		50	250	$\mu\text{A}$
Negative Supply Current	$I_{SS}$	Logic inputs = 0 V, $V_{SS} = -5\text{ V}$		0.001	1	$\mu\text{A}$
Power Dissipation	$P_{DISS}$	Logic inputs = 0 V			1.25	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = \pm 5\%$			0.006	%/%

# AD5554/AD5554

Parameter	Symbol	Condition	Min	Typ	Max	Unit
AC CHARACTERISTICS <sup>4</sup>						
Output Voltage Settling Time	$t_s$	To $\pm 0.1\%$ of full scale, data = 0000 <sub>H</sub> to FFFF <sub>H</sub> to 0x0000		1		$\mu$ s
Output Voltage Settling Time	$t_s$	To $\pm 0.0015\%$ of full scale, data = 0000 <sub>H</sub> to FFFF <sub>H</sub> to 0000 <sub>H</sub>		2		$\mu$ s
Reference Multiplying BW	BW – 3 dB	$V_{REFX} = 100$ mV rms, data = FFFF <sub>H</sub> , $C_{FB} = 15$ pF		2		MHz
DAC Glitch Impulse	Q	$V_{REFX} = 10$ V, data 0000 <sub>H</sub> to 8000 <sub>H</sub> to 0000 <sub>H</sub>		12		nV-s
Feedthrough Error	$V_{OUTX}/V_{REFX}$	Data = 0000 <sub>H</sub> , $V_{REFX} = 100$ mV rms, $f = 100$ kHz		–65		dB
Crosstalk Error	$V_{OUTA}/V_{REFB}$	Data = 0000 <sub>H</sub> , $V_{REFB} = 100$ mV rms, adjacent channel, $f = 100$ kHz		–90		dB
Digital Feedthrough	Q	$\overline{CS} = 1$ , and $f_{CLK} = 1$ MHz		5		nV-s
Total Harmonic Distortion	THD	$V_{REF} = 5$ V p-p, data = FFFF <sub>H</sub> , $f = 1$ kHz		–90		dB
Output Spot Noise Voltage	$e_n$	$f = 1$ kHz, BW = 1 Hz		7		nV/Hz

<sup>1</sup> All static performance tests (except  $I_{OUT}$ ) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5544  $R_{FB}$  terminal is tied to the amplifier output. Typical values represent average readings measured at 25 °C.

<sup>2</sup> These parameters are guaranteed by design and not subject to production testing.

<sup>3</sup> All input control signals are specified with  $t_r = t_f = 2.5$  ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

<sup>4</sup> All ac characteristic tests are performed in a closed-loop system using an OP42 I-to-V converter amplifier.

## AD5554 ELECTRICAL CHARACTERISTICS

$V_{DD} = 5$  V  $\pm 10\%$ ,  $V_{SS} = 0$  V,  $I_{OUTX}$  = virtual GND,  $A_{GNDX} = 0$  V,  $V_{REFA}$ , B, C, D = 10 V,  $T_A$  = full operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
STATIC PERFORMANCE <sup>1</sup>						
Resolution	N	1 LSB = $V_{REF}/2^{14} = 610$ $\mu$ V when $V_{REF} = 10$ V			14	Bits
Relative Accuracy	INL				$\pm 1$	LSB
Differential Nonlinearity	DNL				$\pm 1$	LSB
Output Leakage Current	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = 25^\circ$ C			10	nA
	$I_{OUTX}$	Data = 0000 <sub>H</sub> , $T_A = T_A$ Max			20	nA
Full-Scale Gain Error	$G_{FSE}$	Data = 3FFF <sub>H</sub>		$\pm 2$	$\pm 10$	mV
Full-Scale Tempco <sup>2</sup>	TCV <sub>FS</sub>			1		ppm/°C
Feedback Resistor	$R_{FBX}$	$V_{DD} = 5$ V	4	6	8	k $\Omega$
REFERENCE INPUT						
$V_{REFX}$ Range	$V_{REFX}$		–15		+15	V
Input Resistance	$R_{REFX}$		4	6	8	k $\Omega$
Input Resistance Match	$R_{REFX}$	Channel-to-channel		1		%
Input Capacitance <sup>2</sup>	$C_{REFX}$			5		pF
ANALOG OUTPUT						
Output Current	$I_{OUTX}$	Data = 3FFF <sub>H</sub>	1.25		2.5	mA
Output Capacitance <sup>2</sup>	$C_{OUTX}$	Code-dependent		80		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	$V_{IL}$				0.8	V
Logic Input High Voltage	$V_{IH}$		2.4			V
Input Leakage Current	$I_{IL}$				1	$\mu$ A
Input Capacitance <sup>2</sup>	$C_{IL}$				10	pF
Logic Output Low Voltage	$V_{OL}$	$I_{OL} = 1.6$ mA			0.4	V
Logic Output High Voltage	$V_{OH}$	$I_{OH} = 100$ $\mu$ A	4			V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>INTERFACE TIMING<sup>2,3</sup></b>						
Clock Width High	$t_{CH}$		25			ns
Clock Width Low	$t_{CL}$		25			ns
$\overline{CS}$ to Clock Setup	$t_{CSS}$		0			ns
Clock to $\overline{CS}$ Hold	$t_{CSH}$		25			ns
Clock to SDO Prop Delay	$t_{PD}$		2		20	ns
Load DAC Pulse Width	$t_{LDAC}$		25			ns
Data Setup	$t_{DS}$		20			ns
Data Hold	$t_{DH}$		20			ns
Load Setup	$t_{LDS}$		5			ns
Load Hold	$t_{LDH}$		25			ns
<b>SUPPLY CHARACTERISTICS</b>						
Power Supply Range	$V_{DD\ RANGE}$		4.5		5.5	V
Positive Supply Current	$I_{DD}$	Logic inputs = 0 V		50	250	$\mu A$
Negative Supply Current	$I_{SS}$	Logic inputs = 0 V, $V_{SS} = -5$ V		0.001	1	$\mu A$
Power Dissipation	$P_{DISS}$	Logic inputs = 0 V			1.25	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = \pm 5\%$			0.006	%/%
<b>AC CHARACTERISTICS<sup>4</sup></b>						
Output Voltage Settling Time	$t_s$	To $\pm 0.1\%$ of full scale, data = 0000 <sub>H</sub> to 3FFF <sub>H</sub> to 0000 <sub>H</sub>		1		$\mu s$
Output Voltage Settling Time	$t_s$	To $\pm 0.0015\%$ of full scale, data = 0000 <sub>H</sub> to 3FFF <sub>H</sub> to 0000 <sub>H</sub>		2		$\mu s$
Reference Multiplying BW	BW – 3 dB	$V_{REFX} = 100$ mV rms, data = 3FFF <sub>H</sub> , $C_{FB} = 15$ pF		2		MHz
DAC Glitch Impulse	Q	$V_{REFX} = 10$ V, data 0000 <sub>H</sub> to 2000 <sub>H</sub> to 0000 <sub>H</sub>		12		nV-s
Feedthrough Error	$V_{OUTX}/V_{REFX}$	Data = 0000 <sub>H</sub> , $V_{REFX} = 100$ mV rms, $f = 100$ kHz		-65		dB
Crosstalk Error	$V_{OUTA}/V_{REFB}$	Data = 0000 <sub>H</sub> , $V_{REFB} = 100$ mV rms, adjacent channel, $f = 100$ kHz		-90		dB
Digital Feedthrough	Q	$\overline{CS} = 1$ , and $f_{CLK} = 1$ MHz		5		nV-s
Total Harmonic Distortion	THD	$V_{REF} = 5$ V p-p, data = 3FFF <sub>H</sub> , $f = 1$ kHz		-90		dB
Output Spot Noise Voltage	$e_N$	$f = 1$ kHz, BW = 1 Hz		7		nV/Hz

<sup>1</sup> All static performance tests (except  $I_{OUT}$ ) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5554  $R_{FB}$  terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.

<sup>2</sup> These parameters are guaranteed by design and not subject to production testing.

<sup>3</sup> All input control signals are specified with  $t_r = t_f = 2.5$  ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

<sup>4</sup> All ac characteristic tests are performed in a closed-loop system using an OP42 I-to-V converter amplifier.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V <sub>DD</sub> to GND	−0.3 V, +8 V
V <sub>SS</sub> to GND	+0.3 V, −7 V
V <sub>REF</sub> to GND	−18 V, +18 V
Logic Input and Output to GND	−0.3 V, +8 V
V(I <sub>OUT</sub> ) to GND	−0.3 V, V <sub>DD</sub> + 0.3 V
A <sub>GNDX</sub> to DGND	−0.3 V, + 0.3 V
Input Current to Any Pin Except Supplies	±50 mA
Package Power Dissipation	(T <sub>J</sub> Max − T <sub>A</sub> )/θ <sub>JA</sub>
Thermal Resistance	θ <sub>JA</sub>
28-Lead Shrink Surface-Mount (RS-28)	100°C/W
Maximum Junction Temperature (T <sub>J</sub> Max)	150°C
Operating Temperature Range: Model A	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature:	
RS-28 (Vapor Phase, 60 secs)	215°C
RS-28 (Infrared, 15 secs)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

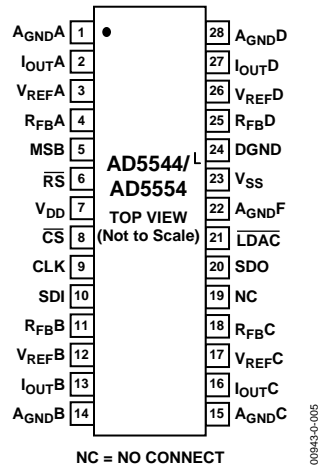


Figure 3. AD5544/AD5554 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Name	Function
1	AGND A	DAC A Analog Ground.
2	IOUT A	DAC A Current Output.
3	VREF A	DAC A Reference Voltage Input Terminal. Establishes DAC A full-scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
4	RFB A	Establish voltage output for DAC A by connecting to external amplifier output.
5	MSB	MSB Bit. Set pin during a reset pulse ( $\overline{RS}$ ) or at system power ON if tied to ground or V <sub>DD</sub> .
6	$\overline{RS}$	Reset Pin, Active Low Input. Input registers and DAC registers are set to all zeros or half-scale code (8000 <sub>H</sub> for AD5544 and 2000 <sub>H</sub> for AD5554) determined by the voltage on the MSB pin. Register Data = 0000 <sub>H</sub> when MSB = 0. Register Data = 8000 <sub>H</sub> for AD5544 and 2000 <sub>H</sub> .
7	V <sub>DD</sub>	Positive Power Supply Input. Specified range of operation 5 V $\pm$ 10%.
8	$\overline{CS}$	Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial register data to the input register when $\overline{CS}/\overline{LDAC}$ returns high. Does not effect LDAC operation.
9	CLK	Clock Input. Positive edge clocks data into shift register.
10	SDI	Serial Data Input. Input data loads directly into the shift register.
11	RFB B	Establish voltage output for DAC B by connecting to external amplifier output.
12	VREF B	DAC B Reference Voltage Input Terminal. Establishes DAC B full-scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
13	IOUT B	DAC B Current Output.
14	AGND B	DAC B Analog Ground.
15	AGND C	DAC C Analog Ground.
16	IOUT C	DAC C Current Output.
17	VREF C	DAC C Reference Voltage Input Terminal. Establishes DAC C full-scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
18	RFB C	Establish voltage output for DAC C by connecting to external amplifier output.
19	NC	No Connect. Leave pin unconnected.
20	SDO	Serial Data Output. Input data loads directly into the shift register. Data appears at SDO, 19 clock pulses for AD5544 and 17 clock pulses for AD5554 after input at the SDI pin.
21	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. Transfers all input register data to DAC registers. Asynchronous active low input. See Table 5 and Table 6 for operation.
22	AGNDF	High Current Analog Force Ground.
23	VSS	Negative Bias Power Supply Input. Specified range of operation: -5.5 V to +0.3 V.
24	DGND	Digital Ground Pin.
25	RFB D	Establish Voltage Output for DAC D by Connecting to External Amplifier Output.
26	VREF D	DAC D Reference Voltage Input Terminal. Establishes DAC D full-scale output voltage. Pin can be tied to V <sub>DD</sub> pin.
27	IOUT D	DAC D Current Output.
28	AGND D	DAC D Analog Ground.

# AD5554/AD5554

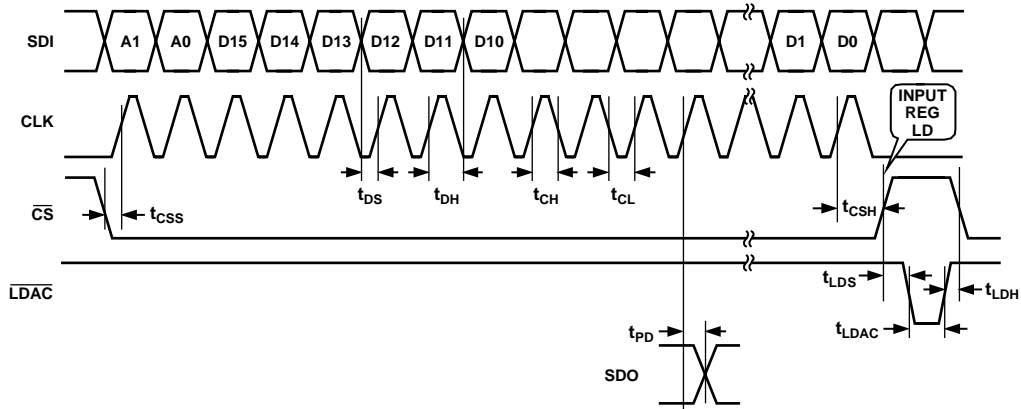


Figure 4. AD5544 Timing Diagram

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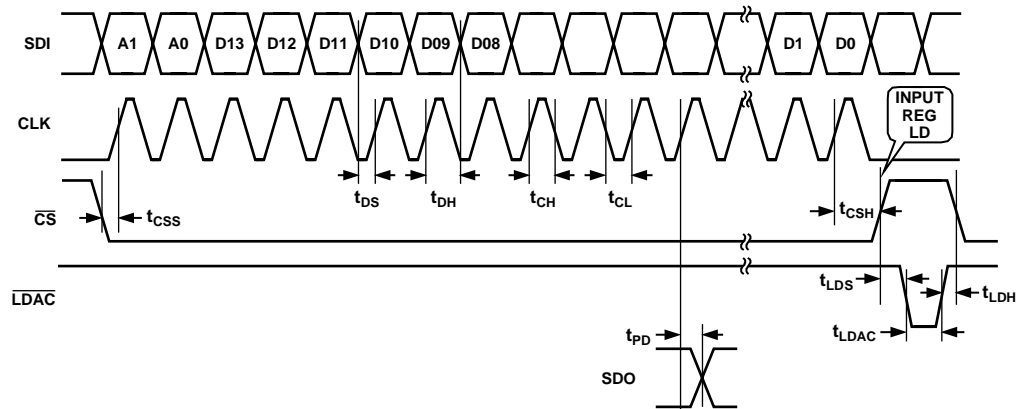


Figure 5. AD5554 Timing Diagram

00943-0-004

Table 5. AD5544<sup>1</sup> Control-Logic Truth Table

CS	CLK	LDAC	RS	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift-Register-Data Advanced One Bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with Current SR Contents	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0000 <sub>H</sub>	Latched Data = 0000 <sub>H</sub>
H	X	H	L	H	No Effect	Latched Data = 8000 <sub>H</sub>	Latched Data = 8000 <sub>H</sub>

<sup>1</sup> For the AD5544, data appears at the SDO Pin 19 clock pulses after input at the SDI pin.



Table 6. AD5554<sup>1</sup> Control-Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	RS	MSB	Serial Shift Register <sup>2</sup> Function	Input Register <sup>2</sup> Function	DAC Register
H	X	H	H	X <sup>3</sup>	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	$\uparrow_{+2}$	H	H	X	Shift-Register-Data Advanced One Bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
$\uparrow_{+2}$	L	H	H	X	No Effect	Selected DAC Updated with Current Shift-Register Contents <sup>4</sup>	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	$\uparrow_{+}$	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0000 <sub>H</sub>	Latched Data = 0000 <sub>H</sub>
H	X	H	L	H	No Effect	Latched Data = 2000 <sub>H</sub>	Latched Data = 2000 <sub>H</sub>

<sup>1</sup> For the AD5554, data appears at the SDO Pin 17 clock pulses after input at the SDI pin.

<sup>2</sup>  $\uparrow_{+}$  positive logic transition.

<sup>3</sup> X = don't care.

<sup>4</sup> At power on both the input register and the DAC register are loaded with all zeros.

Table 7. AD5544 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format<sup>1</sup>

	MSB																	LSB
Bit Position	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

<sup>1</sup> Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the  $\overline{CS}$  line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (Bits D15 to D0) to the decoded DAC-input-register address determined by Bits A1 and A0. Any extra bits clocked into the AD5544 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the  $\overline{LDAC}$  pin can be tied logic low to disable the DAC registers.

Table 8. AD5554 Serial Input Register Data Format, Data Is Loaded in the MSB-First Format<sup>1</sup>

	MSB																	LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		B0
Data Word	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		D0

<sup>1</sup> Only the last 16 bits of data clocked into the serial register (address + data) are inspected when the  $\overline{CS}$  line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (Bits D13 to D0) to the decoded DAC-input-register address determined by Bits A1 and A0. Any extra bits clocked into the AD5554 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the  $\overline{LDAC}$  pin can be tied logic low to disable the DAC registers.

Table 9. Address Decode

A1	A0	DAC Decoded
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

## TYPICAL PERFORMANCE CHARACTERISTICS

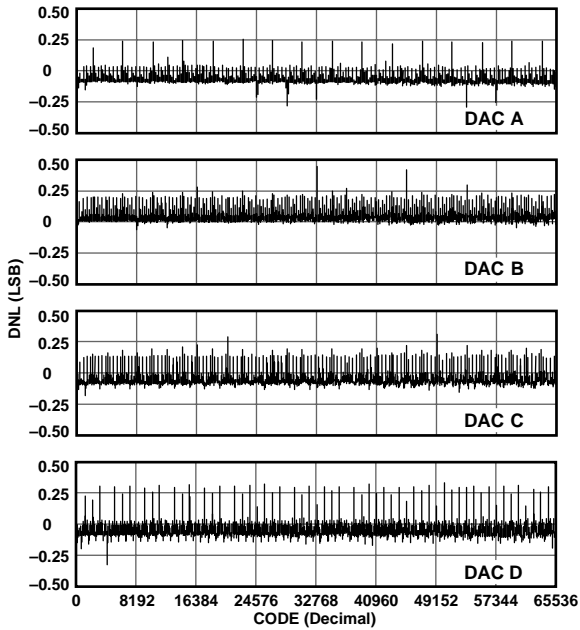


Figure 6. AD5544 DNL vs. Code,  $T_A = 25^\circ\text{C}$

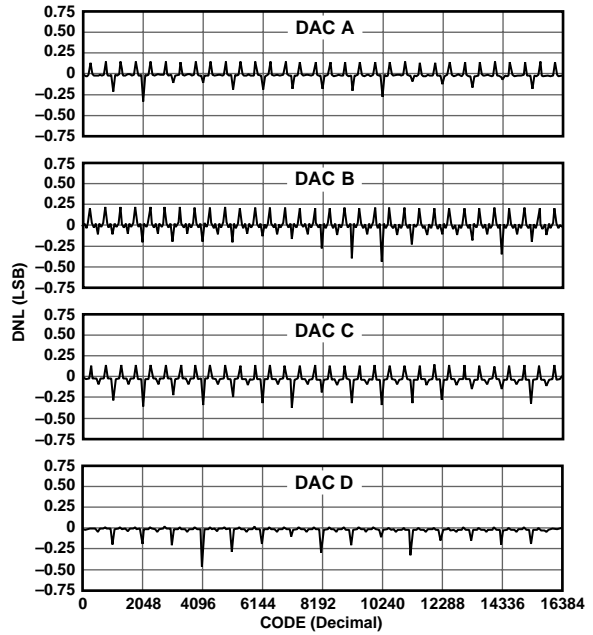


Figure 8. AD5554 DNL vs. Code,  $T_A = 25^\circ\text{C}$

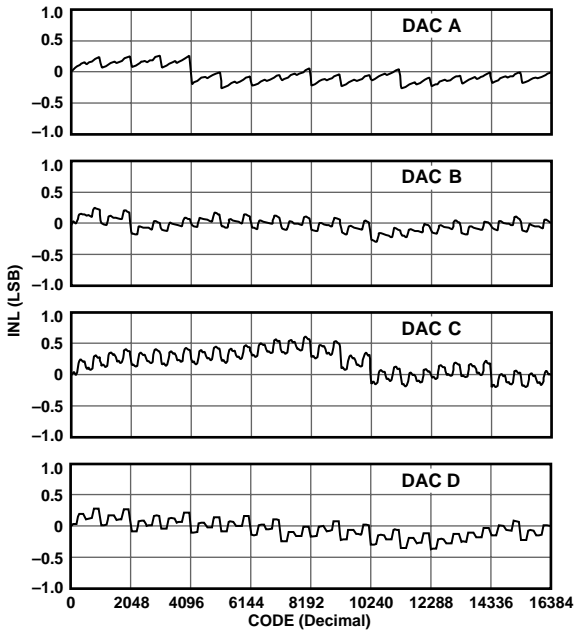


Figure 7. AD5554 INL vs. Code,  $T_A = 25^\circ\text{C}$

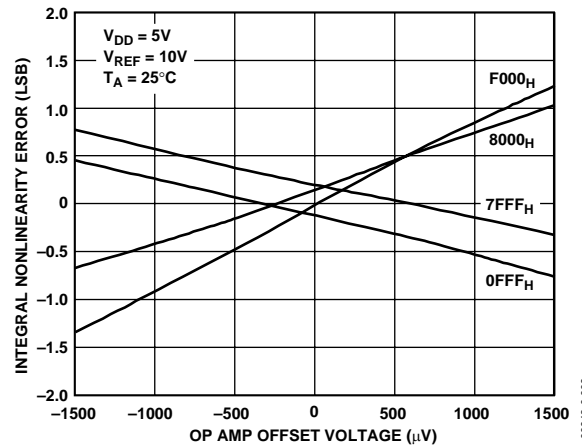


Figure 9. AD5544 Integral Nonlinearity Error vs. Op Amp Offset

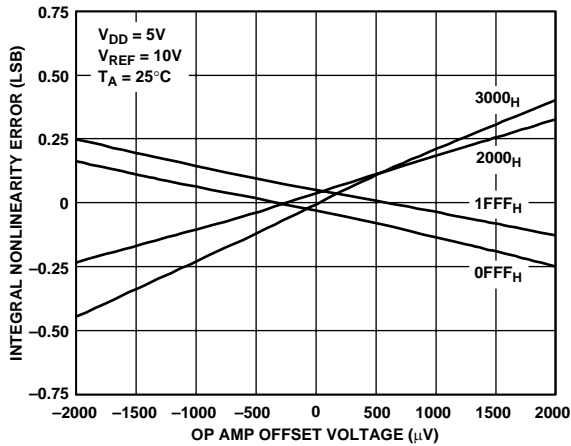


Figure 10. AD5544 Integral Nonlinearity Error vs. Op Amp Offset

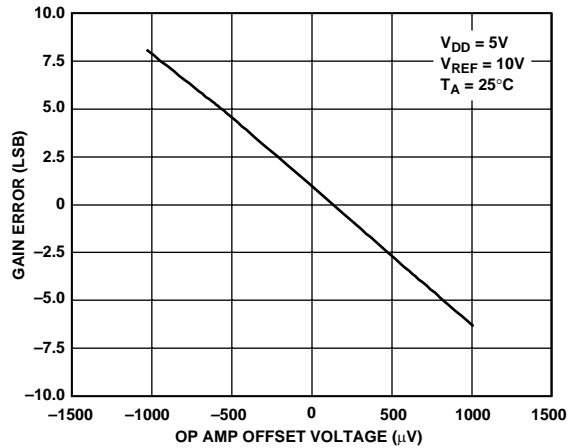


Figure 13. AD5544 Gain Error vs. Op Amp Offset

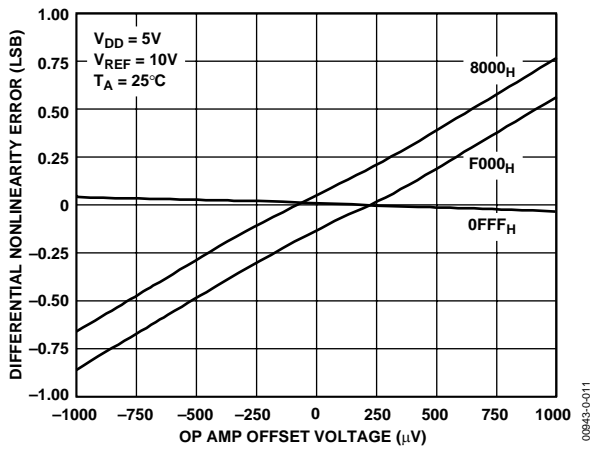


Figure 11. AD5544 Differential Nonlinearity Error vs. Op Amp Offset

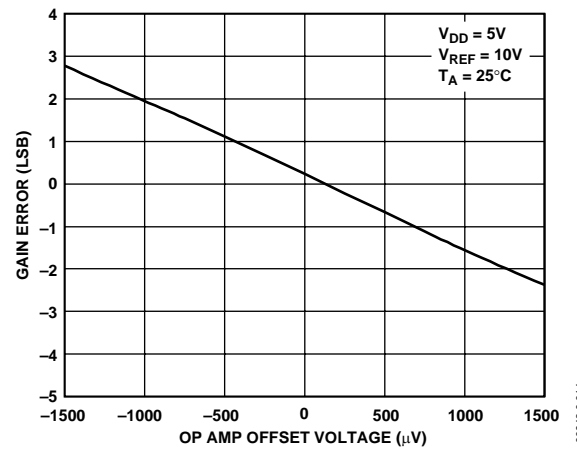


Figure 14. AD5554 Gain Error vs. Op Amp Offset

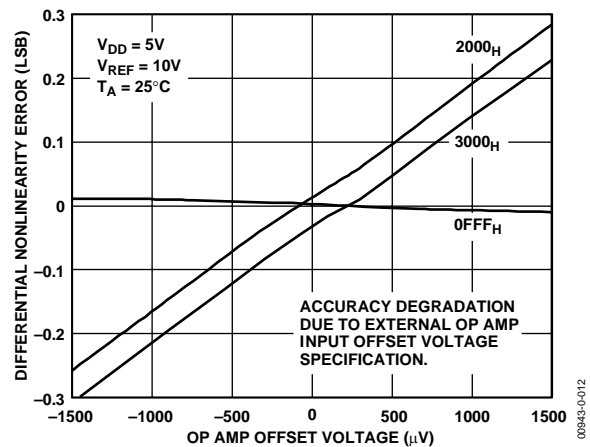


Figure 12. AD5554 Differential Nonlinearity Error vs. Op Amp Offset

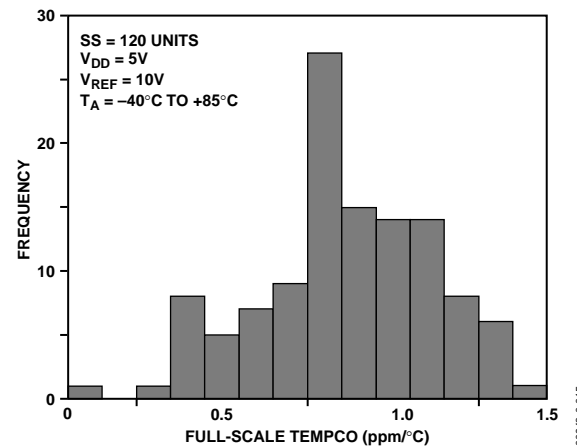


Figure 15. AD5544 Full-Scale Tempco (ppm/°C)

# AD5554/AD5554

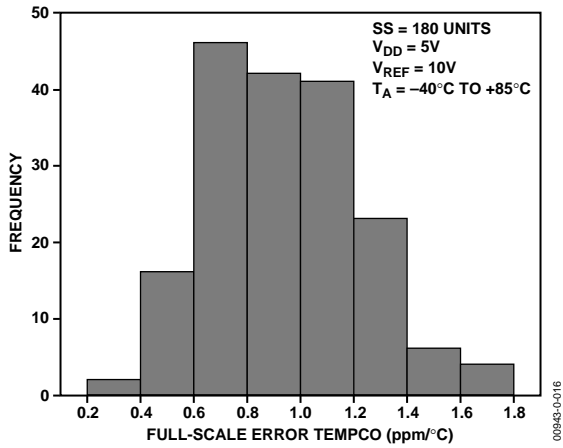


Figure 16. AD5554 Full-Scale Tempco (ppm/°C)

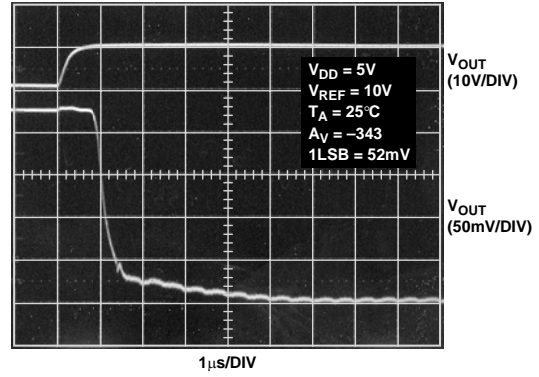


Figure 19. AD5554 Small Signal Settling Time

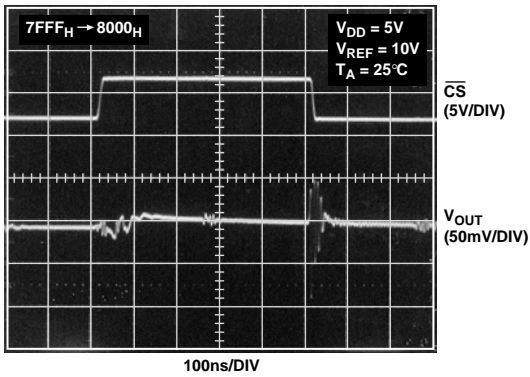


Figure 17. AD5554 Midscale Transition

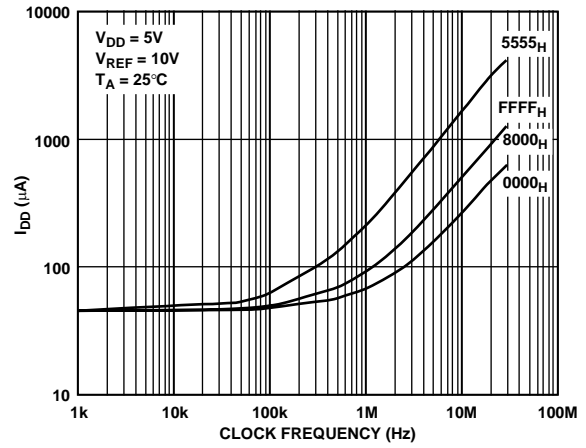


Figure 20. AD5554 Power Supply Current vs. Clock Frequency

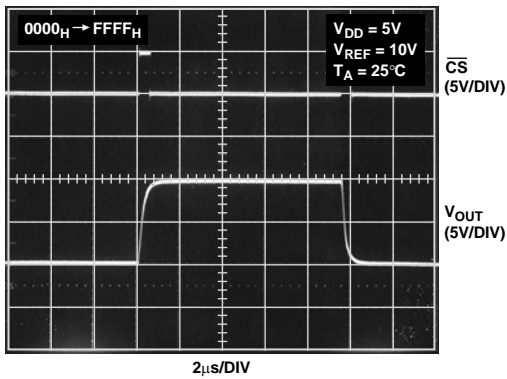


Figure 18. AD5554 Large Signal Settling Time

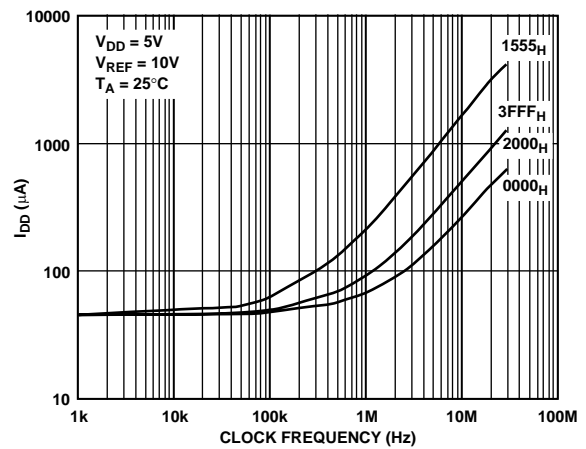


Figure 21. AD5554 Power Supply Current vs. Clock Frequency

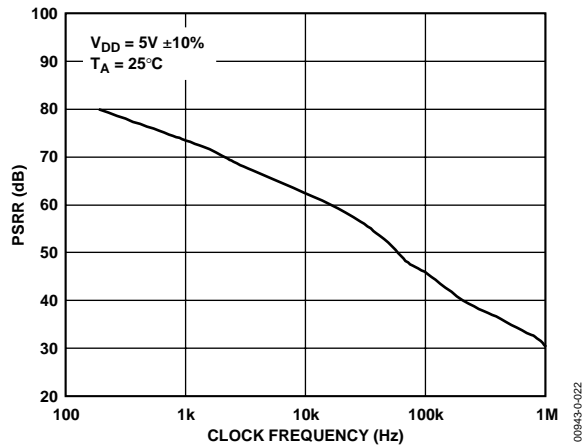


Figure 22. AD5544/AD5554 Power Supply Rejection vs. Frequency

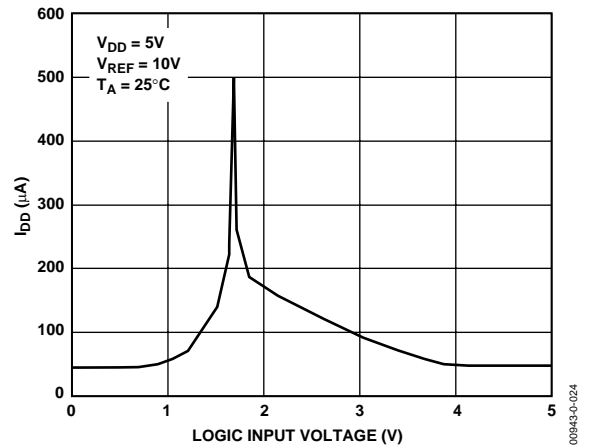


Figure 24. AD5544/AD5554 Power Supply Current vs. Logic Input Voltage

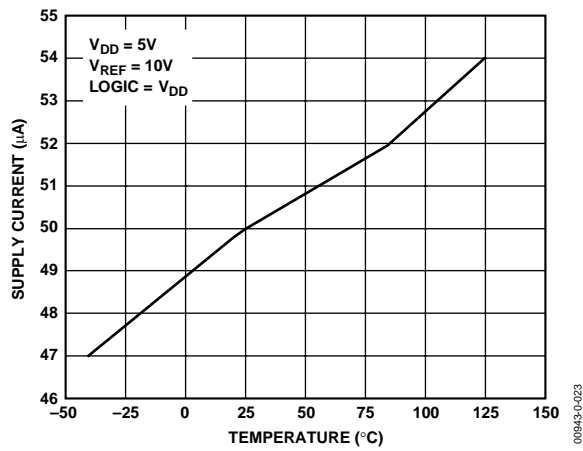


Figure 23. AD5544/AD5554 Power Supply Current vs. Temperature

## CIRCUIT OPERATION

The AD5544 and AD5554 contain four, 16-bit and 14-bit, current-output, digital-to-analog converters, respectively. Each DAC has its own independent multiplying reference input. Both the AD5544 and the AD5554 use a 3-wire, SPI compatible, serial data interface, with a configurable asynchronous  $\overline{RS}$  pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an  $\overline{LDAC}$  strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

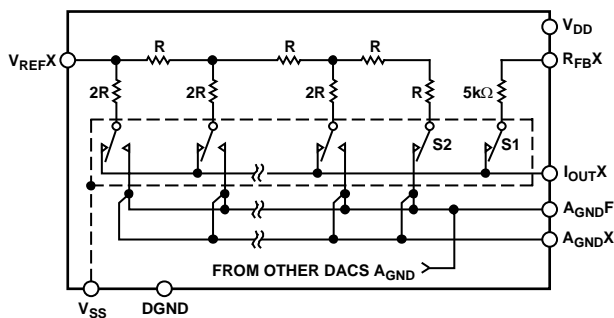
### D/A CONVERTER

Each part contains four current-steering R-2R ladder DACs. Figure 25 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The  $R_{FBX}$  pin connects to the output of the external amplifier. The  $I_{OUTX}$  terminal connects to the inverting input of the external amplifier. The  $A_{GNDX}$  pin should be Kelvin-connected to the load point requiring full 16-bit accuracy. These DACs are designed to operate with both negative or positive reference voltage. The  $V_{DD}$  power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 k $\Omega$  feedback resistor. If users attempt to measure the value of  $R_{FB}$ , power must be applied to  $V_{DD}$  in order to achieve continuity. An additional VSS bias pin is used to guard the substrate during high temperature applications, minimizing zero-scale leakage currents that double every 10°C. The DAC output voltage is determined by  $V_{REF}$  and the digital data (D) in the following equations:

$$V_{OUT} = -V_{REF} \times \frac{D}{65536} \quad (\text{For AD5544}) \quad (1)$$

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \quad (\text{For AD5554}) \quad (2)$$

Note that the output polarity is opposite to the  $V_{REF}$  polarity for dc reference voltages.



DIGITAL INTERFACE CONNECTIONS OMITTED FOR CLARITY. SWITCHES S1 AND S2 ARE CLOSED,  $V_{DD}$  MUST BE POWERED.

Figure 25. Typical Equivalent DAC Channel

These DACs are also designed to accommodate ac reference input signals. Both the AD5544 and the AD5554 accommodate input reference voltages in the range of -12 V to +12 V. The reference voltage inputs exhibit a constant nominal input

resistance of 5 k $\Omega$ ,  $\pm 30\%$ . On the other hand, the DAC outputs  $I_{OUTA}$ , B, C, D are code-dependent and produce various output resistances and capacitances. The choice of external amplifier should take into account the variation in impedance generated by the AD5544/AD5554 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor ( $C_{FB}$ ) may be needed to provide a critically damped output response for step changes in reference input voltages. Figure 26 and Figure 27 show the gain vs. frequency performance at various attenuation settings using a 23 pF external feedback capacitor connected across the  $I_{OUTX}$  and  $R_{FBX}$  terminals for AD5544 and AD5554, respectively. In order to maintain good analog performance, power supply bypassing of 0.01  $\mu$ F, in parallel with 1  $\mu$ F, is recommended. Under these conditions, a clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and PSS frequency-dependent characteristics. It is best to derive the AD5544/AD5554's 5 V supply from the system's analog supply voltages. Do not use the digital 5 V supply (see Figure 28).

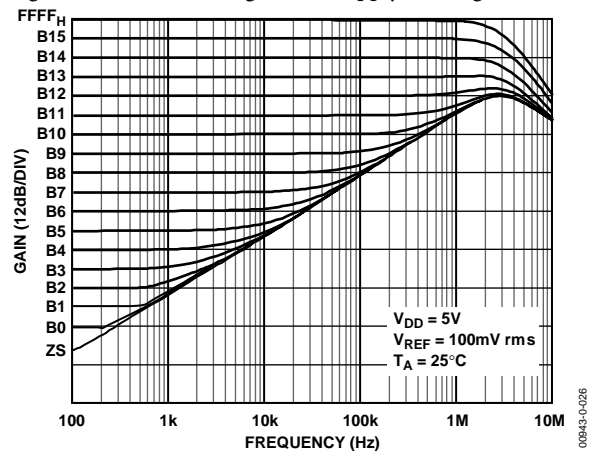


Figure 26. AD5544 Reference Multiplying Bandwidth vs. Code

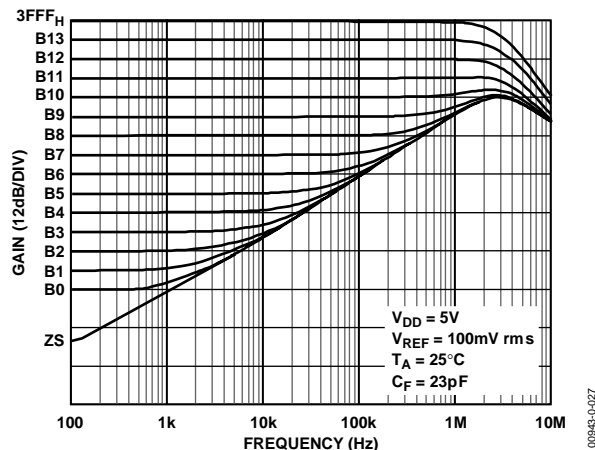
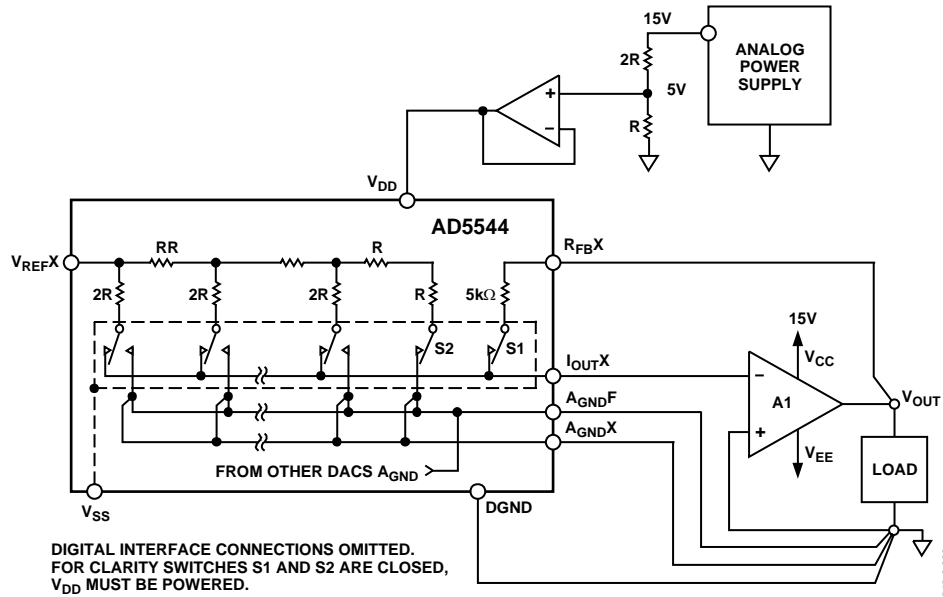


Figure 27. AD5554 Reference Multiplying Bandwidth vs. Code



00543-0-028

Figure 28. Recommended Kelvin-Sensed Hookup





If these functions are not needed, the  $\overline{RS}$  pin can be tied to logic high. The asynchronous input  $\overline{RS}$  pin forces all input and DAC registers to either the zero-code state (MSB = 0) or the half-scale state (MSB = 1).

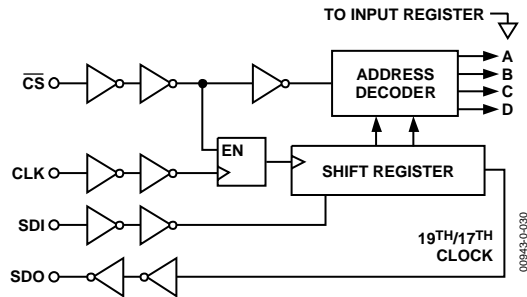


Figure 30. AD5544/AD5554 Equivalent Logic Interface

## POWER ON RESET

When the  $V_{DD}$  power supply is turned on, an internal reset strobe forces all the input and DAC registers to the zero-code state or half-scale state, depending on the MSB pin voltage. The  $V_{DD}$  power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of  $V_{DD} = 1.5\text{ V}$  to  $2.3\text{ V}$ . The  $V_{SS}$  supply has no effect on the power-on reset performance. The DAC register data will stay at a zero or half-scale setting until a valid serial register data load takes place.

## ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground ( $D_{GND}$ ) and  $V_{DD}$ , as shown in Figure 31.

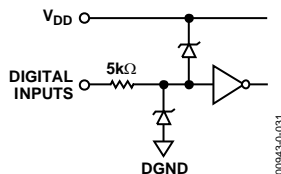


Figure 31. Equivalent ESD Protection Circuits

## Power Supply Sequence

As standard practice, it is recommended to power  $V_{DD}$ ,  $V_{SS}$ , and ground prior to any reference. The ideal power up sequence is  $A_{GNDX}$ ,  $D_{GND}$ ,  $V_{DD}$ ,  $V_{SS}$ ,  $V_{REFX}$ , and digital inputs. A noncompliance power up sequence may elevate the reference current, but the devices resume normal operation once  $V_{DD}$  and  $V_{SS}$  are powered-up.

## Layout and Power Supply Bypassing

It is good practice to employ a compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with  $0.01\ \mu\text{F}$  to  $0.1\ \mu\text{F}$  disc or chip ceramic capacitors. Low-ESR  $1\ \mu\text{F}$  to  $10\ \mu\text{F}$  tantalum or

electrolytic capacitors should also be applied at  $V_{DD}$  to minimize any transient disturbance and filter any low frequency ripple (see Figure 32). Users should not apply switching regulators for  $V_{DD}$  due to the power supply rejection ratio degradation over frequency.

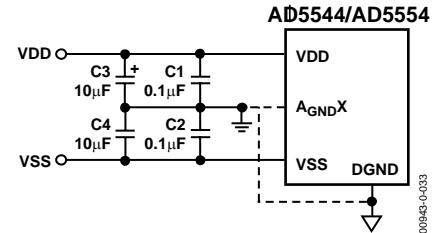


Figure 32. Power Supply Bypassing and Grounding Connection

## Grounding

The  $D_{GND}$  and  $A_{GNDX}$  pins of the AD5544/AD5554 refer to digital and analog ground references. To minimize the digital ground bounce, the  $D_{GND}$  terminal should be joined remotely at a single point to the analog ground plane (see Figure 32).

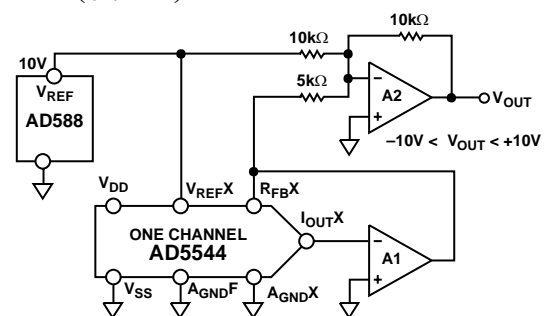
## APPLICATIONS

The AD5544/AD5554 are inherently 2-quadrant multiplying D/A converters. That is, they can be easily set up for unipolar output operation. The full-scale output polarity is the inverse of the reference-input voltage.

In some applications it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an additional external amplifier (A2) configured as a summing amplifier (see Figure 33). In this circuit the first and second amplifiers (A1 and A2) provide a total gain of 2 which increases the output voltage span to 20 V. Biasing the external amplifier with a 10 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ( $V_{OUT} = -10\text{ V}$ ) to midscale ( $V_{OUT} = 0\text{ V}$ ) to full-scale ( $V_{OUT} = 10\text{ V}$ ).

$$V_{OUT} \left( \frac{D}{32768} - 1 \right) \times -V_{REF} \quad (\text{For AD5544}) \quad (3)$$

$$V_{OUT} \left( \frac{D}{8192} - 1 \right) \times -V_{REF} \quad (\text{For AD5554}) \quad (4)$$

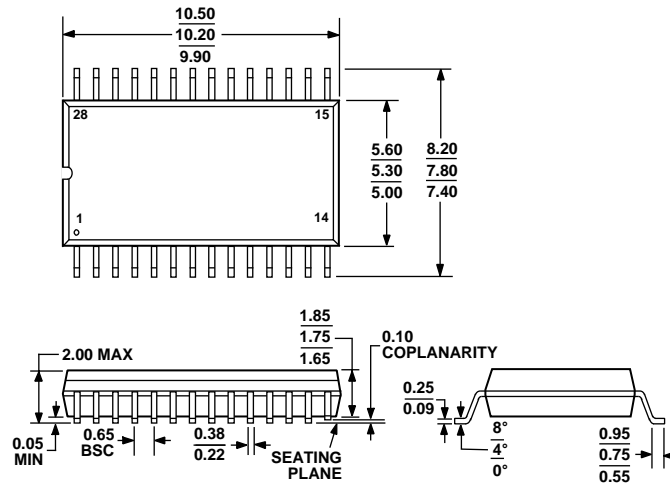


DIGITAL INTERFACE CONNECTIONS OMITTED FOR CLARITY.

Figure 33. Four-Quadrant Multiplying Application Circuit

# AD5544/AD5554

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150AH

Figure 34. 28-Lead SSOP  
(RS-28)

Dimensions Shown in Inches and (Millimeters)

## ORDERING GUIDE

Model	RES Bit	INL LSB	DNL LSB	Temperature Range	Package Description	Package Option
AD5544ARS	16	±4	±1.5	-40°C to +85°C	SSOP-28	RS-28
AD5554BRS	14	±1	±1	-40°C to +85°C	SSOP-28	RS-28
AD5544EVAL					Evaluation Board	

**NOTES**

**AD5544/AD5554**

**NOTES**