Intel® Entry Server Board SE7230CA1-E

Technical Product Specification

Revision 1.0

April 2006

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
April 2006	0.5	Release subject to change.
May 2006	1.0	Update bios.

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1.   Introduction

This *Intel® Entry Server Board SE7230CA1-E Technical Product Specification* (TPS) provides a high-level technical description for the Intel® Entry Server Board SE7230CA1-E. It details the architecture and feature set for all functional sub-systems that make up the server board.

1.1   Section Outline

This document is divided into the following chapters:

- Section 1 – Introduction
- Section 2 – Server Board Overview
- Section 3 – Functional Architecture
- Section 4 – System BIOS
- Section 5 – Platform Management Architecture
- Section 6 – Error Reporting and Handling
- Section 7 – Connectors and Jumper Blocks
- Section 8 – Absolute Maximum Ratings
- Section 9 – Design and Environmental Specifications
- Section 10 – Hardware Monitoring
- Appendix A – Integration and Usage Tips
- Glossary
- Reference Documents

1.2   Server Board Use Disclaimer

Intel® server boards contain a number of high-density VLSI* and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

2.   Server Board Overview

The Intel® Entry Server Board SE7230CA1-E is a monolithic printed circuit board with features that support the UP server high-density (1U) market.

2.1   Intel® Entry Server Board SE7230CA1-E Feature Set

The Intel® Entry Server Board SE7230CA1-E supports the following feature set:

- Processor and Front Side Bus (FSB) support
  - Supports Pentium® 4 processor Extreme Edition, Pentium® processor Extreme Edition, Pentium® D, Pentium® 4 and Celeron® D processors in the Intel® 775-pin PLGA package
  - Supports Intel® Dual Core Architecture
  - Supports Hyper-Threading Technology
  - Supports Intel® Extended Memory System 64 Technology (Intel® EM64T)
- Intel® E7230 Chipset components
  - Intel® E7230 MCH Memory Controller Hub
  - Intel® ICH7R I/O Controller
  - 12-deep In-order Queue
- Memory System
  - Four DIMM sockets supporting 533/667MHz DDR2 DIMMs
  - Data bandwidth per channel of 4.2GB/s or 8.4GB/s in dual channel when using DDR2 667MHz
  - Support for up to two DDR2 channels for a total of four DIMMs (two DIMMs / channel) providing up to 8 MB max memory capacity.
  - Support for 512-MB, 1-GB and 2-GB DDR2 DIMMs
- I/O Subsystem
- Board I/O Subsystem (Two independent PCI buses):
  - Segment A: One embedded Intel® Gigabit Ethernet Controller 10/100/1000 82541PI (Supports *PCI Specification, Rev 2.3*)
  - Segment B: One x1 PCI Express* resource implemented as an embedded Intel® 10/100/1000 82573E Gigabit Ethernet Controller
- Serial ATA host controller
- Two independent SATA ports support data transfer rates up to 1.5 Gb/s (150MB/s) per port
- Universal Serial Bus 2.0 (USB)
- Two external USB ports with an additional internal header providing two optional USB ports for front panel support.
  - Supports wake-up from sleeping states S1-S4 (S3 not supported)
  - Supports Legacy Keyboard/Mouse connections when using PS2-USB dongle
- LPC (Low Pin Count) bus segment with one embedded device

- Super I/O controller chips providing all PC-compatible I/O (floppy, serial, keyboard, mouse, two serial com port) and integrated hardware monitoring
- LC Super I/O = SMsC* LP47M182NR
- Standard Intel® 14-pin SSI front panel 2x9 power connectors
- Fan Support
  - Two general purpose 4-pin fans
- Intel® Light-guided Diagnostic LEDs to display POST code indicators during boot

The following figure shows the board layout of the Intel® Entry Server Board SE7230CA1-E. Each connector and major component is identified by letter and is identified in Table 1.
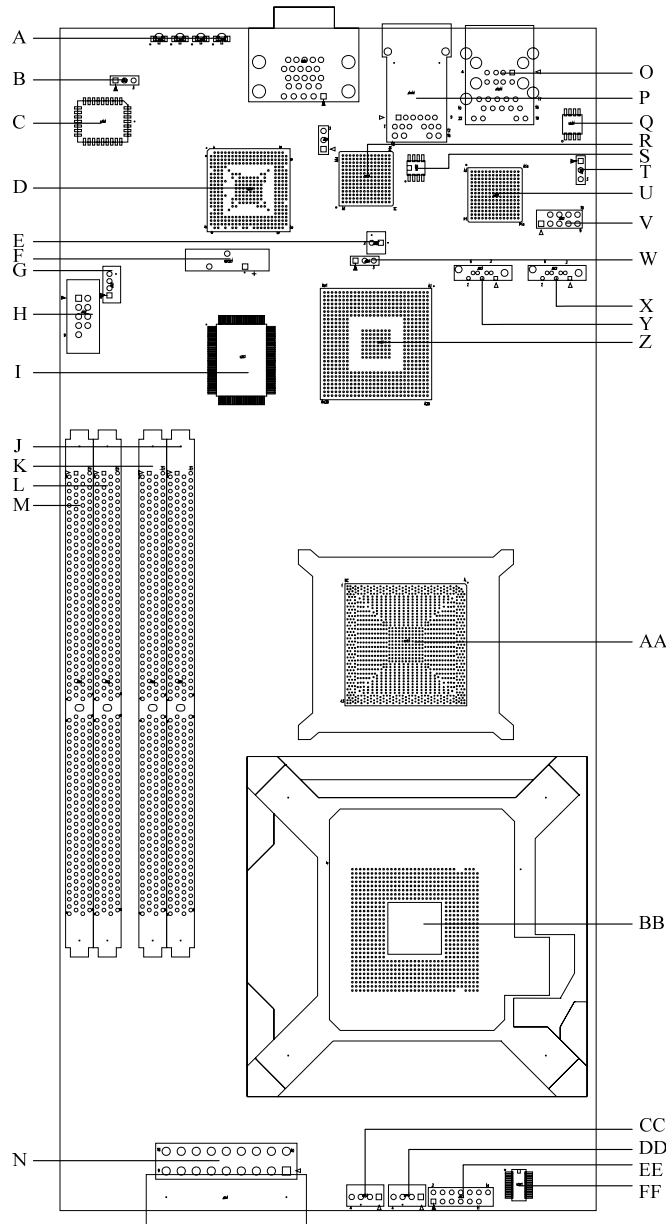
Figure 1. Intel® Entry Server Board SE7230CA1-E Layout

Table 1. Server Board Layout Reference

Ref	Description	Ref	Description
A	Post LEDs	Q	NIC1 SPI Flash
B	BIOS recovery jumper	R	Intel® 82541PI LAN Controller
C	BIOS Flash(FWH)	S	NIC2 SPI EEPROM
D	ATI* ES1000 video controller	T	Intel® AMT firmware update jumper
E	Chassis intrusion header	U	Intel® 82573E LAN Controller
F	Battery	V	USB 3 and 4 header
G	I^{2}C Connector	W	Clear CMOS jumper
H	Serial B header	X	SATA port 2
I	SMSC* LPC47M182 SIO	Y	SATA port 1
J	Memory Slot DIMM 1A	Z	Intel® 82802 ICH7R
K	Memory Slot DIMM 2A	AA	Intel® E7230 MCH
L	Memory Slot DIMM 1B	BB	775-Land (LGA) CPU Socket
M	Memory Slot DIMM 2B	CC	System Fan 1 (4-pin)
N	2 x 9 Power connector	DD	System Fan 2 (4-pin)
O	NIC1 RJ-45 and USB 1 and 2 connector	EE	2 x 7 Front Panel header
P	NIC2 RJ-45 connector	FF	Hardware Management Controller

3.   Functional Architecture

This section provides a high-level description of the functionality associated with the architectural blocks that make up the Intel® Entry Server Board SE7230CA1-E.
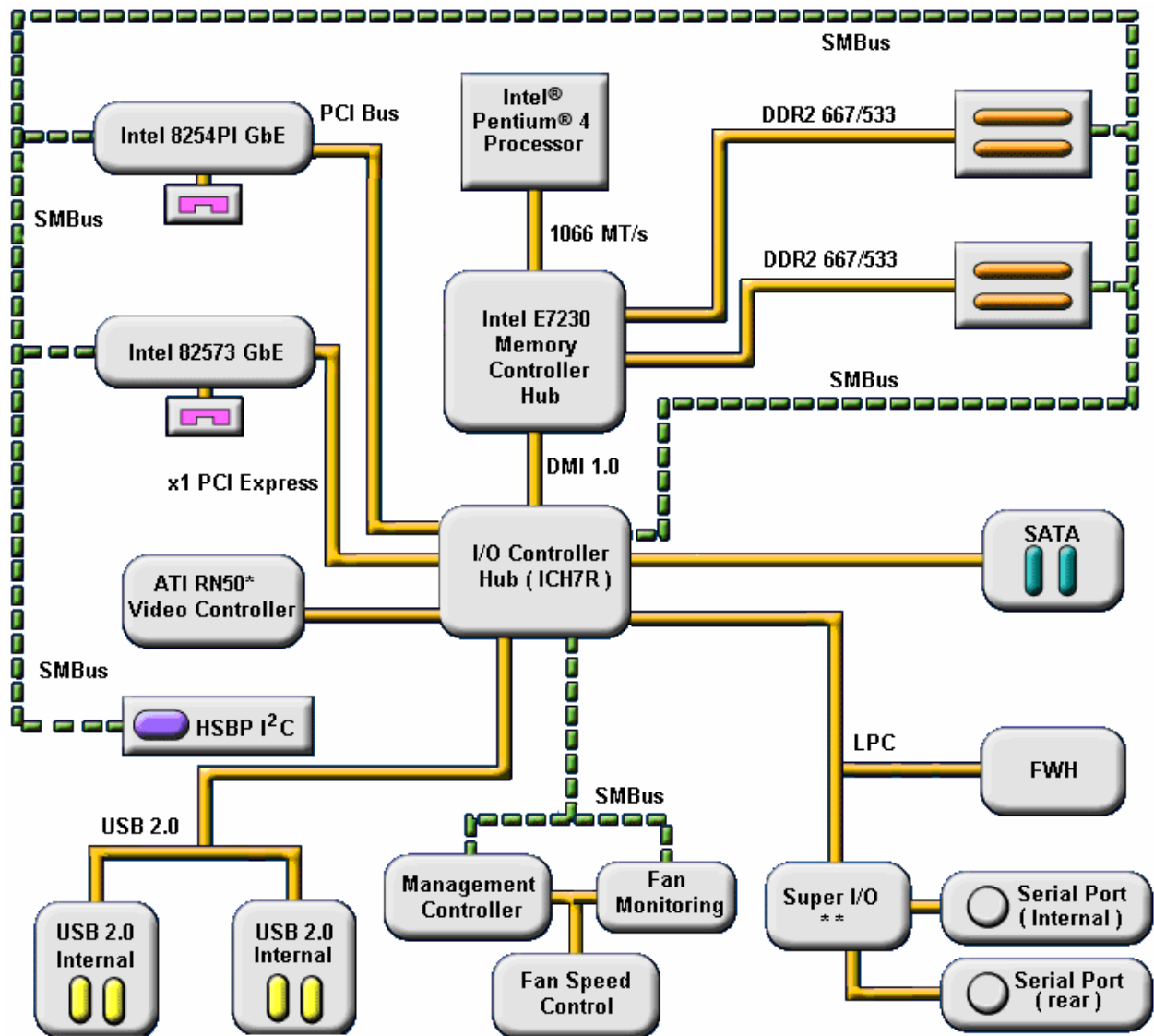
Figure 2. Intel® Entry Server Board SE7230CA1-E Block Diagram

3.1   Processor Sub-System

The Intel® Entry Server Board SE7230CA1-E supports the following:

- Pentium® 4 processor Extreme Edition in the 775-land package
- Pentium® processor Extreme Edition in the 775-land package
- Pentium® D processors in the 775-land package
- Pentium® 4 processors in the 775-land package
- Celeron® D processors in the 775-land package

The 775-land package is a follow-on to Pentium® 4 and Celeron® processors in the 478-pin package with enhancements to the Intel NetBurst® micro-architecture, including but not limited to the following:

- Dual Core Architecture
- Hyper-Threading Technology
- Intel® EM64T
- Pentium® 4 processor Extreme Edition
- Pentium® processor Extreme Edition
- Pentium® D processor
- Pentium® 4 processor
- Celeron® D processor

The processors built on 90-nm and 65-nm process technology in the 775-land package utilize Flip-Chip Land Grid Array (FC-LGA4) package technology, and plug into a 775-land LGA socket, referred to as the Intel® LGA775 socket. The processors are as follows:

- Pentium® 4 processor Extreme Edition, Pentium® processor Extreme Edition
- Pentium® D processor
- Pentium® 4 Processor
- Celeron® D Processor

The above processors in the 775-land package, like their predecessors in the 478-pin package, are based on the same Pentium® 4 micro-architecture. They maintain compatibility with 32-bit software written for the IA-32 instruction set, while supporting 64-bit native mode operation when coupled with supported 64-bit operating systems and applications.

The Celeron® processor does not come in a dual-core configuration, or support Hyper-Threading Technology or Intel® EM64T.

3.1.1   Processor Voltage Regulator Down (VRD)

The Intel® Entry Server Board SE7230CA1-E has a VRD (Voltage Regulator Down) to support one processor. It is compliant with the *VRM 10.1 DC-DC Converter Design Guide Line* and provides a maximum of 120A, which is capable of supporting the requirements for the following processors:

- Pentium® 4 processor Extreme Edition
- Pentium® processor Extreme Edition
- Pentium® D Processor
- Pentium® 4 Processor
- Celeron® D Processor

The board hardware monitors the processor VTTEN (Output enable for VTT) pin before turning on the VRD. If the VTTEN pin of the processors is not identical, the Power On Logic will not turn on the VRD.

3.1.2   Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc., through the CPUID instruction. The requirement is:

- Processor run at a fixed speed, but BIOS can program it to operate at a lower or higher speed.

The processor information is read at every system power-on.

Note: The processor speed is the processor power-on reset default value. No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers.

3.1.3   Processor Support

The Intel® Entry Server Board SE7230CA1-E supports one processor in the Intel® LGA775 package. The support circuitry on the server board consists of the following:

- Intel® LGA775 processor socket supporting:
  - Pentium® D Processor with 800MHz system bus
  - Pentium® 4 Processor with 800MHz system bus
  - Pentium® 4 processor Extreme Edition with 1066 MHz system bus
- Processor host bus AGTL+ support circuitry

Table 2. Processor Support Matrix

Processor Family	Package Type	Frequency	Cache Size	Front Side Bus
Pentium® 4 processor Extreme Edition	Intel® LGA775	3.73GHz	2MB L2	1066MHz
Pentium® D processor	Intel® LGA775	2.8 – 3.6GHz	2 x 1MB or 2x 2MB L2	800MHz
Pentium® 4 processor	Intel® LGA775	3.2 – 3.8 GHz	1MB or 2MB L2	800MHz
Celeron® D processor	Intel® LGA775	2.26 – 3.2 GHz	256K L2	533MHz

Note: For a complete list of all supported processors, please visit the Intel® Entry Server Board SE7230CA1-E support site located at the following URL:
http://support.intel.com/support/motherboards/server/

In addition to the circuitry described above, the processor subsystem contains the following:

- Reset configuration logic
- Server management registers and sensors

3.2   Intel® E7230 Chipset

The Intel® Entry Server Board SE7230CA1-E is designed around the Intel® E7230 Chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI Express*).

3.2.1   Intel® E7230 Chipset MCH: Memory Control Hub

The MCH accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to the following:

- A memory request queue for subsequent forwarding to the memory sub-system
- An outbound request queue for subsequent forwarding to one of the PCI buses

The MCH also accepts inbound requests from the Intel® ICH7R. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.

The MCH is a 1210-ball FC-BGA device and uses the proven components of the following previous generations:

- Pentium® 4 processor Extreme Edition
- Pentium® processor Extreme Edition
- Pentium® D Processor
- Pentium® 4 Processor bus interface unit
- Hub interface unit
- DDR2 memory interface unit

The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 72-bit wide memory interface.

The MCH integrates the following main functions:

- An integrated high performance main memory subsystem
- A DMI which provides an interface to the Intel® ICH7R

Other features provided by the MCH include the following:

- Full support of ECC on the processor bus
- Full support of Intel® x4 Single Device Data Correction on the memory interface with x4 DIMMs
- Twelve deep in-order queue, two deep defer queue
- Full support of un-buffered DDR2 ECC DIMMs
- Support for 1 GB and 2 GB DDR2 memory modules
- Memory scrubbing

3.2.1.1 MCH Memory Sub-System Overview

The MCH supports a 72-bit wide memory sub-system that can support a maximum of 8 GB of DDR2 memory using 2 GB DIMMs. This configuration needs external registers for buffering the memory address and control signals. The four chip selects are registered inside the MCH and need no external registers for chip selects.

The memory interface runs at 533/667MT/s. The memory interface supports a 72-bit wide memory array. It uses seventeen address lines (BA [2:0] and MA [13:0]) and supports 512-MB, 1-GB, and 2-GB DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, and multiple-bit error detection and Intel® x4 Single Device Data Correction with x4 DIMMs.

The DDR2 interface supports up to 8 GB of main memory and supports single- and double-density DIMMs. The DDR2 can be any industry-standard DDR2. The following table shows the DDR2 DIMM technology supported.

Table 3. Supported DDR2 Modules

DDR2-533/667 Un-buffered SDRAM Module Matrix					
DIMM Capacity	**DIMM Organization**	**SDRAM Density**	**SDRAM Organization**	**# SDRAM Devices/rows/Banks**	**# Address bits rows/Banks/column**
512 MB	64M x 72	256Mbit	32M x 8	18 / 2 / 4	13 / 2 / 10
512 MB	64M x 72	512Mbit	64M x 8	9 / 1 / 4	14 / 2 / 10
1 GB	128M x 72	512Mbit	64M x 8	18 / 2 / 4	14 / 2 / 10
1 GB	128M x 72	1Gbit	128M x 8	9 / 1 / 8	14 / 4 / 10
2 GB	256M x 72	2GB	128M x 8	18 / 2 / 8	14 / 8 / 10

3.2.1.2   PCI Express*

3.2.1.2.1   x1 PCI Express* Subsystem

The Intel® ICH7R supports two x 1 PCI Express* buses. Only one is used to support the Intel® 82573-Gigabit Ethernet Controller.

One 32-bit PCI bus segment is directed through the Intel® ICH7R Interface A. This PCI Segment B has an embedded device, the Intel® 82541PI LAN (NIC2).

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-B devices and the corresponding device description:

Table 4. Segment B Configuration

IDSEL Value	Device
21	Intel® 82541PI LAN (NIC2)

PCI Segment B supports one PCI master. All PCI masters must arbitrate for PCI access using resources supplied by the Intel® ICH7R. The host bridge PCI interface arbitration lines REQx* and GNTx* are internal to the Intel® ICH7R. The following table defines the arbitration connections:

Table 5. Segment B Arbitration Connections

Server board Signals	Device
PCIX REQ_N5/GNT_N5	Intel® 82541PI LAN (NIC2)

3.2.2   I/O Controller Hub

3.2.2.1   Intel® ICH7R: I/O Controller Hub 7R

The Intel® ICH7R controller has several components. It provides the interface for a 32-bit/33-MHz PCI bus. The Intel® ICH7R can be both a master and a target on that PCI bus and includes a USB 2.0 controller and an IDE controller. The ICH7R controller is also responsible for much of the power management functions, with ACPI control registers built in. It also provides a number of GPIO pins and has the LPC bus to support low-speed Legacy I/O.

The MCH and Intel® ICH7R chips provide the pathway between the processor and the I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or Legacy I/O locations. If the cycle is directed to one of the PCI Express* segments, the MCH communicates with the PCI Express* devices (add-in card, on board devices) through the PCI Express* interface. If the cycle is directed to the Intel® ICH7R, the cycle is output on the MCH's DMI bus. All I/O for the board, including PCI and PC-compatible I/O, is directed through the MCH and then through the Intel® ICH7R provided PCI buses.

The Intel® ICH7R is a multi-function device, housed in a 609-pin mBGA device. It provides the following:

- A DMI bus
- A PCI 32-bit/33-MHz interface
- An IDE interface
- An integrated Serial ATA Host controller
- A USB controller
- A PCI Express* x4 interface
- A power management controller

Each function within the Intel® ICH7R has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The primary role of the ICH7R controller is providing the gateway to all PC-compatible I/O devices and features. The board uses the following the Intel® ICH7R features:

- PCI 32-bit/33MHz interface for Intel® 82541PI Gigabit Ethernet Controller
- PCI 32-bit/33MHz interface to dedicated ATI* ES1000 video subsystem
- LPC bus interface
- x1 PCI Express* interface for Intel® 82573E Gigabit Ethernet Controller
- DMI (Direct Media Interface)
- Integrated dual-port Serial ATA Host controller
- Universal Serial Bus (USB) 2.0 interface
- PC-compatible timer/counter and DMA controllers
- APIC and 82C59 interrupt controller
- Power management
- System RTC

- ▪ Supports the SmBUS 2.0 Specification
- ▪ General-purpose I/O (GPIO)

The following are the descriptions of how each supported feature is used for the Intel® ICH7R on the board.

3.2.2.1.1   SATA Controller

The Intel® ICH7R contains four SATA ports. The data transfer rates are up to 150Mbyte/s per port.

3.2.2.2   Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The Intel® ICH7R provides the functionality of two-cascaded 82C59 with 15 interrupts handling. It supports a processor system bus interrupt.

3.2.2.2.1   Advanced Programmable Interrupt Controller (APIC)

Interrupt generation and notification to the processor is done by the APICs in the Intel® ICH7R using messages on the front side bus.

3.2.2.2.2   Universal Serial Bus (USB) Controller

The Intel® ICH7R contains one EHCI USB 2.0 controller and four USB ports. The USB controller moves data between main memory and up to four USB connectors. All ports function identically and with the same bandwidth. The Intel® Entry Server Board SE7230CA1-E implements four ports on the board.

Two external USB ports are provided on the back of the server board. The *Universal Serial Bus Specification, Revision 1.1,* defines the external connectors.

The third/fourth USB port is optional and can be accessed by cabling from an internal 9-pin connector located on the server board to an external USB port located either in front of or the rear of a given chassis.

3.2.2.2.3   Enhanced Power Management

One of the embedded functions of the Intel® ICH7R is a power management controller. This is used to implement ACPI-compliant power management features. The server board supports sleep states S0, S1, S4, and S5.

3.3   Memory Sub-System

The server board supports up to four DIMM sockets for a maximum memory capacity of 8 GB. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 533/667MTs. The memory controller supports the following:

- Memory scrubbing
- Single-bit error correction
- Multiple-bit error detection
- Intel® x4 Single Device Data Correction support with x4 DIMMs

Memory can be implemented with either single-sided (one row) or double-sided (two row) DIMMs

3.3.1   Memory Configuration

The memory interface between the MCH and the DIMMs is a 64-bit (non-ECC) or 72-bit (ECC) wide interface.

There are two banks of DIMMs, labeled Bank 1 and Bank 2. Bank 1 contains DIMM socket locations DIMM_1A and DIMM_2A. Bank 2 contains DIMM socket locations DIMM_1B and DIMM_2B. The sockets associated with each bank or channel are located next to each other and the DIMM socket identifiers are marked on the server board silkscreen, near the DIMM socket. Bank 1 is associated with Memory Channel A while Bank 2 is associated with Memory Channel B. When only two DIMM modules are being used, the population order must be DIMM_1A, DIMM_1B to ensure dual channel operating mode.

In order to operate in dual channel dynamic paging mode, the following conditions must be met:

- Two identical DIMMs are installed, one each in DIMM_1A and DIMM_1B
- Four identical DIMMs are installed (one in each socket location)

Note: Installing only three DIMMs is not supported. Do not use DIMMs that are not matched (same type and speed). Use of identical memory parts is always the preferred method.

DIMM and memory configurations must adhere to the following:

- DDR2 533/667, un-buffered, DDR2 DIMM modules
- DIMM organization: x72 ECC or x 64 Non-ECC
- Pin count: 240
- DIMM capacity: 256 MB, 512 MB, 1 GB and 2 GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage options: 1.8 V
- Interface: SSTL2

Table 6. Memory Bank Labels and DIMM Population Order

Location	DIMM Label	Channel	Population Order
J2D1	(DIMM_1A)	A	1
J1D3	(DIMM_2A)	A	3
J1D2	(DIMM_1B)	B	2
J1D1	(DIMM_2B)	B	4
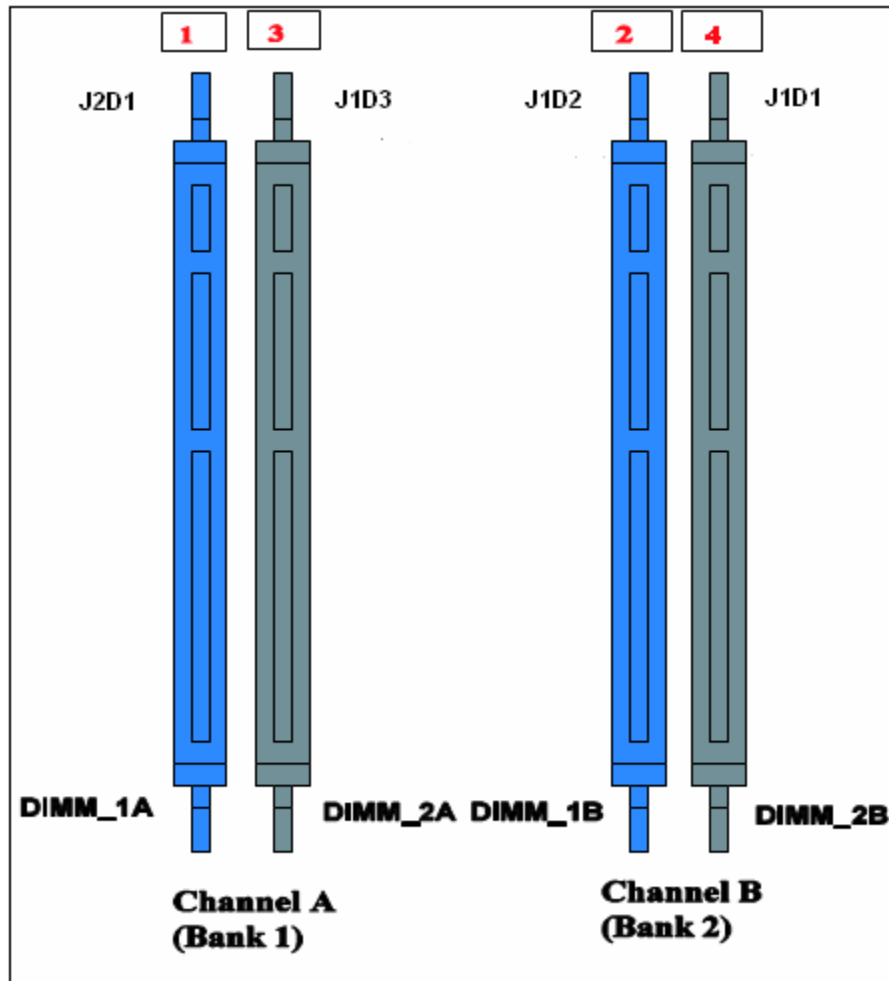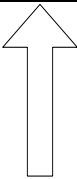
Figure 3. Memory Bank Label Definition

Table 7. Characteristics of Dual/Single Channel Configuration with or without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual channel with dynamic paging mode	All DIMMs matched
	Dual channel without dynamic paging mode	DIMMs matched from Channel A to Channel B DIMMs not matched within channels
	Single channel with dynamic paging mode	Single DIMM or DIMMs matched with a channel
Lowest	Single channel without dynamic paging mode	DIMMs not matched

3.3.2   Memory DIMM Support

The board supports un-buffered (not registered) DDR2 533/667 ECC or Non-ECC DIMMs operating at 533/667MT/s. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on this board. A list of qualified DIMMs is available at http://support.intel.com/support/motherboards/server/.

Note all DIMMs are supported by design, but only fully qualified DIMMs will be supported on the board.

The minimum supported DIMM size is 256 MB. Therefore, the minimum main memory configuration is 1 x 256 MB or 256 MB. The largest size DIMM supported is 2 GB and as such, the maximum main memory configuration is 8 GB implemented by 4 x 2-GB DIMMs.

- Only un-buffered DDR2 533/667 compliant, ECC x8 and non-ECC x8 or x16 memory DIMMs are supported.
- ECC single-bit errors (SBE) will be corrected; multiple-bit error (MBE) will only be detected.
- Intel® Entry Server Board SE7230CA1-E supports Intel® x4 Single Device Data Correction with x4 DIMMs.
- The maximum memory capacity is 8 GB via four 2 GB DIMM modules.
- The minimum memory capacity is 256 MB via a single 256 MB DIMM module.

3.4   I/O Sub-System

3.4.1   PCI Subsystem

The primary I/O buses for the Intel® Entry Server Board SE7230CA1-E are two independent PCI bus segments providing PCI, PCI Express*. The PCI buses comply with the *PCI Local Bus Specification, Rev 2.3*.

PCI Segments A and B are directed through the Intel® ICH7R. The following table lists the characteristics of the two PCI bus segments.

Table 8. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Card Slots
A	3.3V	32 bits	33MHz	PCI 32	NIC 1
B	3.3V	1 lane	1.5GHz	x1 PCI Express*	NIC 2

3.4.1.1   P32-A: 32-bit, 33-MHz PCI Subsystem

The Intel® ICH7R provides a Legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface. P32-A supports the following embedded devices and connectors:

- One Intel® 82541PI Network Controller

All 32-bit/33-MHz PCI I/O for the board is directed through the Intel® ICH7R. The 32-bit/33-MHz PCI segment created by the Intel® ICH7R is known as PCI Segment A. Segment A supports the following embedded device:

- One 10/100/1000-T Network Interface Controller: Intel® 82541PI Gigabit Ethernet Controller.

3.4.1.1.1   Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD (31:16), which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for Segment A devices and the corresponding device description.

Table 9. Segment A Configuration IDs

IDSEL Value	Device
21	Intel® 82541PI LAN (NIC2)

3.4.1.1.2   Segment A Arbitration

PCI Segment A supports two PCI devices: the Intel® ICH7R and one PCI bus masters (NIC). All PCI masters must arbitrate for PCI access, using resources supplied by the Intel® ICH7R. The host bridge PCI interface (ICH7R) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 10. Segment A Arbitration Connections

Server Board Signals	Device
PCI REQ_N5/GNT_N5	Intel® 82541PI LAN (NIC2)

3.4.1.2   PCI Interface for ATI Video subsystem

The graphics subsystem is connected to the Intel® ICH7R via a 32/33MHz PCI bus.

3.4.2   Interrupt Routing

The board interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the ICH7R.

3.4.2.1   Legacy Interrupt Routing

For PC-compatible mode, the ICH7R provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The Intel® ICH7R contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

The ICH7R handles both PCI and IRQ interrupts. The Intel® ICH7R translates these to the APIC bus. The numbers in the following table indicate the Intel® ICH7R PCI interrupt input pin to which the associated device interrupt (INTA, INTB, INTC, INTD, INTE, INTF, INTG, INTH for PCI bus and PXIRQ0, PXIRQ1, PXIRQ2, PXIRQ3 for PCI-X bus) is connected. The Intel® ICH7R I/O APIC exists on the I/O APIC bus with the processors.

Table 11. PCI Interrupt Routing/Sharing

Interrupt	INT A	INT B	INT C	INT D
Intel® 82541PI	PIRQB			
ATIES 1000	PIRQC			

3.4.2.2   APIC Interrupt Routing

For APIC mode, the server board interrupt architecture incorporates three Intel® I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The Intel® I/O APICs monitor each interrupt on each PCI device; including PCI slots in addition to the ISA compatibility interrupts IRQ (0-15).

When an interrupt occurs, a message corresponding to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bidirectional data lines.

3.4.2.3   Legacy Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the board. The actual interrupt map is defined using configuration registers in the ICH7R.

Table 12. Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ0	System timer
IRQ1	Keyboard interrupt.
IRQ2	Slave PIC
IRQ3	Serial port 1 interrupt from Super I/O* device, user-configurable.
IRQ4	Serial port 1 interrupt from Super I/O* device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	Generic
IRQ8_L	Active low RTC interrupt.
IRQ9	SCI*
IRQ10	Generic
IRQ11	Generic
IRQ12	Mouse interrupt.
IRQ13	Floaty processor.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	Secondary IDE Cable
SMI*	System Management Interrupt. General purpose indicator sourced by the Intel® ICH7R to the processors.

3.4.2.4   Serialized IRQ Support

The Intel® Entry Server Board SE7230CA1-E supports a serialized interrupt delivery mechanism. Serialized Interrupt Requests (SERIRQ) consists of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

3.5   PCI Error Handling

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.
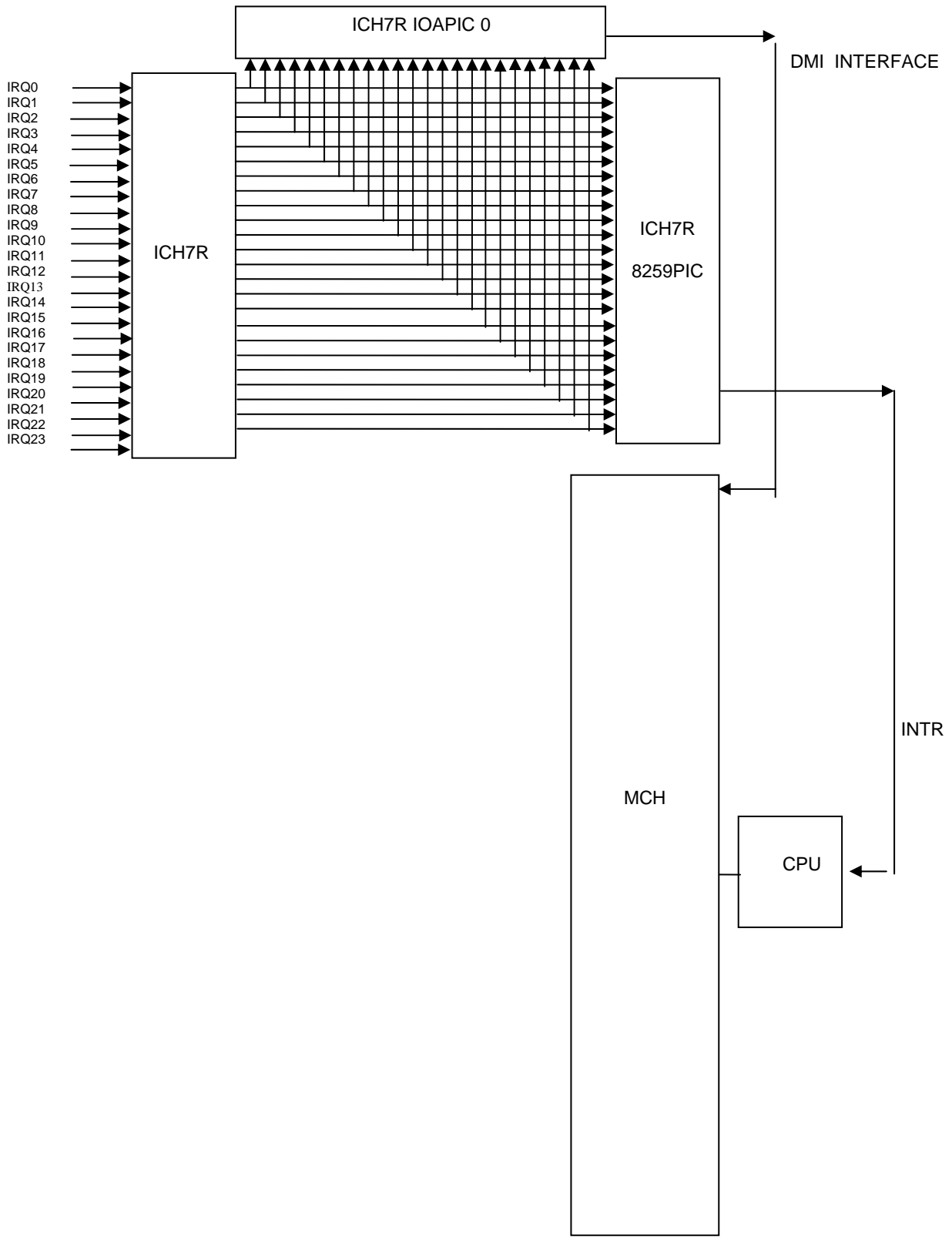
Figure 4. Interrupt Routing Diagram
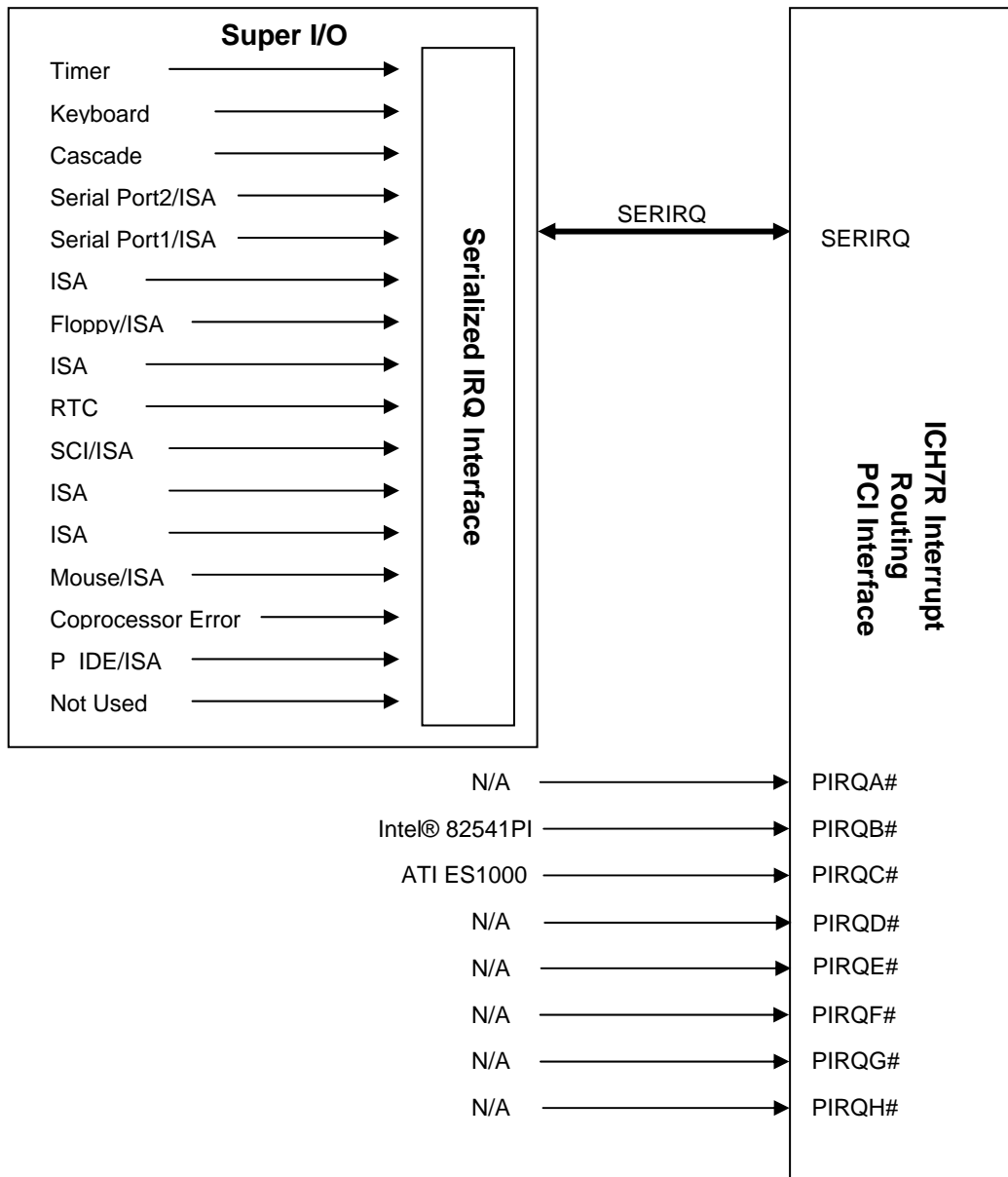
Figure 5. Intel® ICH7R Interrupt Routing Diagram

3.5.1   Video Support

The Intel® Entry Server Board SE7230CA1-E includes an integrated stand-alone ATI* ES1000 graphics engine that supports standard SVGA drivers with analog display capabilities. The graphics subsystem has 16 MB of dedicated memory to support the onboard video controller. The server board provides a standard 15-pin VGA connector at the rear of the system.

3.5.1.1   Video Modes

Table 13. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–

3D Mode	Refresh Rate (Hz)	3D Video Mode Support with Z Buffer Enabled			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–

3D Mode	Refresh Rate (Hz)	3D Video Mode Support with Z Buffer Disabled			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

3.5.2   Network Interface Controller (NIC)

The Intel® Entry Server Board SE7230CA1-E supports two 10/100/1000 Base-T network interfaces.

- NIC1 is an Intel® 82573E Gigabit Ethernet Controller resourced with a x1 PCI Express* interface from the Intel® ICH7R (PCI Segment B).
- NIC2 is an Intel® 82541PI Gigabit Ethernet Controller resourced with a 32bit/33MHz PCI Segment from the Intel® ICH7R (PCI Segment A).

Both the Intel® 82573E and Intel® 82541PI Gigabit Ethernet Controllers are single, compact components with an integrated gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) function. The Intel® 82573E and Intel® 82541PI Gigabit Ethernet Controller allow for a gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs. The Intel® 82541PI Gigabit Ethernet Controller and Intel® 82573E integrate fourth and fifth generation (respectively) gigabit MAC design with fully integrated physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66 MHz.

3.5.2.1   NIC Connector and Status LEDs

The NICs drive two LEDs located on each network interface connector.

Table 14. Intel® 82573E (NIC 1 and NIC 2)

LED	Color	LED State	Condition
Left	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Right	N/A	Off	10 Mbit/sec data rate is selected.
	Green	On	100 Mbit/sec data rate is selected.
	Yellow	On	1000 Mbit/sec data rate is selected.

3.5.3   Super I/O Chip

The SMsC* LP47M182NR SIO devices contain all of the necessary circuitry to control the serial/parallel ports, floppy disk, PS/2-compatible keyboard, mouse and hardware monitor controller. The server board implements the following features:

- GPIOs
- Two serial port
- Local hardware monitoring
- Wake up control
- System health support

3.5.3.1   Serial Ports

The board provides a serial port implemented as an external 9-pin serial port; an internal 9-pin serial port is also provided. The following sections provide details on the use of the serial port.

3.5.3.1.1   *Serial Port A*

Serial A is a standard DB9 interface located at the rear I/O panel of the server board, above the video connector. Serial A is designated by a Serial_A on the silkscreen. The reference designator is J3A1.

Serial B is a 9-pin header interface located near the DIMMs. Serial B is designated by a Serial_B on the silkscreen. The reference designator is J1C2.

Table 15. Serial A Header Pin-out

Pin	Signal Name	Serial Port A Header Pin-out
1	DCD	
2	RX	
3	TX	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	RI	

Table 16. Serial B Header Pin-out

Pin	Signal Name	Serial Port B Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

3.5.3.2   Keyboard and Mouse Support

USB ports can be used to support keyboard and mouse.

3.5.3.3   Wake-up Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

3.5.4   BIOS Flash

The board incorporates an 8-MB firmware Hub flash memory component. This flash device is connected through the LPC bus from the ICH7R controller.

3.5.5   System Health Support

The I^{2}C interface to the Heceta* sensors (fan monitor and control [FMC]) support:
- One PWM-based fan control
- Software or local temperature feedback control
- Chassis intrusion detection

3.6   Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to ten years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠   WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠   ADVARSEL**!**

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

⚠   ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

⚠   VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

⚠   VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

4. System BIOS

4.1   BIOS Setup Utility

The BIOS Setup Utility is provided to perform system configuration changes and to display current settings and environment information.

The BIOS Setup Utility stores configuration settings in system non-volatile storage. Changes affected by BIOS Setup will not take effect until the system is rebooted. The BIOS Setup Utility can be accessed when prompted during POST by using the F2 key.

4.1.1   Localization

The BIOS Setup program and help messages currently support up to six languages. However, depending upon space requirements, the following applies with regard to language support.

- Flex BIOS handles languages based upon OEM requirements. This is a stretch goal.
- The default language is US English. This is the only language that is guaranteed to be properly translated and functional.

4.1.2   Configuration Reset

There are different mechanisms for resetting the system configuration to default values. When a reset system configuration request is detected, the BIOS will load the default system configuration values during the next POST.

A reset system configuration request can be generated by moving the Clear CMOS jumper.

4.1.3   Keyboard Commands

The bottom right portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times.

Each Setup menu page contains a number of features. Except those used for informative purposes, each feature is associated with a value field. This field contains user-selectable parameters. Depending on the security option chosen and in effect by the password, a menu feature's value may or may not be changeable. If a value is non-changeable, the feature's value field is inaccessible. It displays as "grayed out."

The Keyboard Command Bar supports the following keys.

Table 17. BIOS Setup Keyboard Command Bar Options

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.

Key	Option	Description
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered.
		When the ESC key is pressed, any sub-menu, the parent menu is re-entered. When the ESC key is pressed, any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If No is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing any settings. If Yes is selected and the Enter key is pressed, setup is exited and the BIOS continues with POST.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
Tab	Select Field	The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu.
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect.
F9	Setup Defaults	Pressing F9 causes the following to appear: Load Setup Defaults? [OK] [Cancel] If OK is selected and the Enter key is pressed, all setup fields are set to their default values. If Cancel is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values.
F10	Save Changes and Exit	Pressing F10 causes the following message to appear: Save configuration changes and exit setup? [OK] [Cancel] If OK is selected and the Enter key is pressed, all changes are saved and setup is exited. If Cancel is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

4.1.4   Entering BIOS Setup

The BIOS Setup Utility can be accessed by pressing the [F2] hotkey during POST.

4.1.4.1   Main Menu

The first screen displayed when entering the BIOS Setup Utility is the Main Menu selection. This screen displays the major menu selections available. The following tables describe the available options on the top-level and lower-level menus. Default values are in **bold** text.

Table 18. BIOS Setup, Main Menu Options

Feature	Options	Help Text	Description
BIOS Version	N/A	N/A	BIOS ID string (excluding the build time and date)
Processor Type	N/A	N/A	
Hyper Threading Technology	Enable Disable	N/A	Select disable if your operating system does not support Hyper Threading
Processor speed	N/A	N/A	Calculates processor speed
System Bus speed	N/A	N/A	Displays the system bus speed
System Memory speed	N/A	N/A	Displays the system memory speed
L2 Cache RAM	N/A	N/A	
Total Memory	N/A	N/A	Detects amount of physical memory
Memory Mode	N/A	N/A	Displays the memory mode
Memory Channel 1A	N/A	N/A	Displays the memory detected
Memory Channel 2A	N/A	N/A	
Memory Channel 1B	N/A	N/A	
Memory Channel 2B	N/A	N/A	
Additional System Information	N/A	N/A	Selects submenu with additional system information details
System Date	DAY MM/DD/YYYY	Use [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system date.	Configures the system date. Default is [Tue 01/01/2002]. Day of the week is automatically calculated
System Time	HH:MM:SS	Use [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system time.	Configures the system time on a 24-hour clock. Default is 00:00:00

4.1.4.1.1   Additional System Information Sub-menu

Table 19. BIOS Setup, Additional System Information Sub-menu Selections

Feature	Options	Help Text	Description
System Information			Informational display.
Manufacturer	N/A	N/A	

Feature	Options	Help Text	Description
Product Name	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Server Board Information			
Manufacturer	N/A	N/A	
Product Name	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Chassis Information			
Manufacturer	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Asset Tag	N/A	N/A	

4.1.4.2   Advanced Menu

Table 20. BIOS Setup, Advanced Menu Options

Feature	Options	Help Text	Description
Boot configuration	N/A	Configure boot devices	Selects submenu
Peripheral configuration	N/A	Configure peripheral devices	Selects submenu
Drive configuration	N/A	Configure primary master slave and secondary master and slave	Selects submenu
Event log configuration	N/A	View the events in the event log or clear current events	Selects submenu
Video configuration	N/A	Configure video	Selects submenu
Hardware monitoring	N/A	Configure hardware monitoring	Selects submenu
Chipset configuration	N/A	Configure chipset	Selects submenu
Management configuration	N/A	Configure management	Selects submenu
USB configuration	N/A	Configure USB support.	Selects submenu

4.1.4.2.1   Boot Configuration Sub-menu

Table 21. BIOS Setup, Advanced Menu, Boot Configuration Sub-menu Selections

Feature	Options	Help Text	Description
CPU Fan Control	Disable Enable	Enable or Disable CPU fan control	
System Fan Control	Disable Enable	N/A	

Feature	Options	Help Text	Description
Lowest Fan speed	Slow Off	These options define the lower limit of chassis fan speed operation. Slow: At low system temperatures, the fans will continue to run at a slow speed. Off: At low system temperatures, the fans will turn off.	
Max CPUID Value Limit	Disable Enable	This should be enabled in order to boot legacy operating systems that cannot support CPUs with extended CPUID functions	
Display Setup Prompt	Off On	Displays "Press F2 to Enter Setup" message during POST	

4.1.4.2.2   *Peripheral Configuration Sub-menu*

Table 22. BIOS Setup, Advanced Menu, Peripheral Configuration Sub-menu

Feature	Options	Help Text	Description
Serial Port A	Disable **Enable**	Enable or Disable the On board Serial port	
Serial Port B	Disable **Enable**	Enable or Disable the On board Serial port	
PCI Express* On-board LAN	Disable **Enable**	Enable or Disable the PCI Express* On-board LAN Device (NIC1 Intel 82573E)	
PCI On-board LAN	Disable **Enable**	Enable or Disable the PCI On-board LAN Device (NIC2 Intel 82541PI)	

4.1.4.2.3   *Drive Configuration Sub-menu*

Table 23. BIOS Setup, Advanced Menu, Drive Configuration Menu Options

Feature	Options	Help Text	Description
Use Automatic Mode	Disable **Enable**		
Use Serial ATA as	**Enable** Disable	Enable or Disable the on-board Serial ATA ports	
ATA/IDE Mode	Legacy **Enhanced**	Configure SATA for either Enhanced (native) or Legacy mode	Controls state of integrated S-ATA and P-ATA controller.
Configure SATA as	**IDE** RAID AHCI	Configure SATA into the appropriate type	In Enhance mode this item will display.
S.M.A.R.T.	**Enable** Disable	S.M.A.R.T. stands for Self-Monitoring, Analysis, and Reporting Technology	The Auto setting should work in most cases.
SATA Port 0	N/A	N/A	Displays the SATA HDD detected

Feature	Options	Help Text	Description
SATA Port 1	N/A	N/A	Displays the SATA HDD detected
Hard Disk Pre-Delay (Sec)	0 5 10 15 20 25 30 35	Indicates the amount of time in seconds that the firmware will wait to detect hard disk drives	

4.1.4.2.4   Event Log Configuration Sub-menu

Table 24. BIOS Setup, Advanced Menu, Event Log Configuration Sub-menu Selections

Feature	Options	Help Text	Description
View Event Log		Views the events	
Clear Event Log	**Disable** Enable	Clears the events	When Disable is selected, the event log will be cleared during the next system reset
Event Logging	Disable **Enable**		Enables/Disables the event log
ECC Event Logging	Disable **Enable**		Enables/Disables ECC Events recorded in the event log

4.1.4.2.5   Video Configuration Sub-menu

Table 25. BIOS Setup, Advanced Menu, Video Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Console Redirection Serial Port	Disable **Enable**	Enable/Disable Console Redirection via Serial Port (COM1). Video resolution set to 640x480. Serial Port baud rate set to 57600	

4.1.4.2.6 Hardware Monitoring

Table 26. BIOS Setup, Advanced Menu, Hardware Monitoring Sub-menu Selections

Feature	Options	Help Text	Description
Hardware Monitoring	N/A	N/A	
Display H/W Settings	N/A	N/A	Selects submenu, determined by the real system.
Processor Fan Speed	2280		
System Fan1 Speed	0000		
System Fan2 Speed	0000		
Processor Temp	64 C		
Internal Temp	34 C		
V12.0	12.000 V		
V5.0	5.084 V		
V3.3	3.250 V		
V1.5	1.516 V		
Vccp	1.324 V		

4.1.4.2.7 Chipset Configuration Sub-menu Selections

Table 27. BIOS Setup, Advanced Menu, Chipset Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Memory Configuration	N/A	N/A	Selects submenu with memory configuration details
PCI Express* Configuration	N/A	N/A	Selects submenu with PCI Express* configuration details
PCI Latency timer	32 64 96 128 160 192 224 248		

4.1.4.2.7.1 Memory Configuration Sub-menu

This sub-menu provides information about the DIMMs detected by the BIOS. The DIMM number is printed on the server board next to each device.

Table 28. BIOS Setup, Advanced Menu, Chipset Configuration, Memory Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Memory correction	Non-ECC **ECC**	Allow the user to turn error reporting on or off if the system and all the memory installed supports ECC (Error Correction Code)	
Memory frequency	N/A	N/A	Informational display
SDRAM tCL	N/A	N/A	
SDRAM tRCD	N/A	N/A	
SDRAM tRP	N/A	N/A	
SDRAM tRASmin	N/A	N/A	
DDR2 voltage	N/A	N/A	
Total memory	N/A	N/A	
Memory mode	N/A	N/A	
DIMM 1A	N/A	N/A	
DIMM 2A	N/A	N/A	
DIMM 1B	N/A	N/A	
DIMM 2B	N/A	N/A	

4.1.4.2.7.2　　PCI Configuration Sub-menu

This sub-menu provides control over PCI devices and their option ROMs. If the BIOS is reporting POST error 146, use this menu to disable option ROMs that are not required to boot the system.

Table 29. BIOS Setup, Advanced Menu, Chipset Configuration, PCI Express* Configuration Sub-menu Selections

Feature	Options	Help Text	Description
PEG Negotiated Width	N/A	N/A	
Compliance Test Pattern	**Disable** Enable	N/A	

4.1.4.2.8　　Management Configuration Sub-menu

Table 30. BIOS Setup, Advanced Menu, Management Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Enter Intel@ AMT BX Setup	**Disable** Enable	Allows Intel® AMT to be force enabled or disabled. Also controls ability to individually set AMTBX, SOL, IDER capabilities.	

4.1.4.2.9 USB Mass Storage Device Configuration Sub-menu

Table 31. BIOS Setup, Advanced Menu, USB Mass Storage Device Configuration Sub-menu Selections

Feature	Options	Help Text	Description
USB 2.0	**Enable** Disable	N/A	Enable/Disable all USB ports

4.1.4.3   Security Menu

Table 32. BIOS Setup, Security Menu Options

Feature	Options	Help Text	Description
Supervisor password	N/A	Install / Not install	Informational display
User password	N/A	Install / Not install	Informational display
Set supervisor password	N/A	Set supervisor password	Set password to null to clear
Set user password	N/A	Set user password	This node is grayed out until Admin password is installed. Set password to null to clear.
Chassis intrusion	Disable **Enable**	N/A	Chassis intrusion enable will log chassis intrusion to the event log
XD technology	Disable **Enable**	N/A	Enables/Disables the CPU execute disable bit.

4.1.4.4   Power Menu

Table 33. BIOS Setup, Power Menu Selections

Feature	Options	Help Text	Description
After Power Failure	**Stay off** Last State Power On	Determines the mode of operation if a power loss occurs. Stays Off: System will remain off once power is restored. Last State: Restores system to the same state it was before power failed. Power On: System will power on once power is restored.	
Wake on LAN from S5	Stay Off Power On	Determines the action taken when the system power is off and a PCI Power management wake-up event occurs.	

4.1.4.5   Boot Menu

Table 34. BIOS Setup, Boot Menu Selections

Feature	Options	Help Text	Description
Boot menu type	**Normal** Advance	N/A	
Boot device priority	Varies	N/A	Select the boot drive order
Hard drive order	Varies	N/A	Select the boot order of available hard drive devices
CD/DVD-ROM drive order	Varies	N/A	Select the boot order of available CD/DVD devices
Removable drive order	Varies	N/A	Select the boot order of removable devices
Boot to optical devices	Disable **Enable**	Enables or disables boot to optical devices	
Boot to removable devices	Disable **Enable**	Enables or disables boot to removable devices	
Boot to network	Disable **Enable**	Enables or disables boot to network	
USB boot	Disable **Enable**	Enables or disables USB boot	
Zip emulation type	**Floppy** Hard Disk	Sets the emulation type for zip drives	

4.1.4.6   Exit menu

Table 35. BIOS Setup, Exit Menu Selections

Feature	Options	Help Text
Exit saving changes	N/A	Exit system setup after saving the changes. F10 key can be used for this operation.
Exit discarding changes	N/A	Exit system setup without saving any changes. ESC key can be used for this operation.
Load optimal defaults	N/A	Load Setup default values for all the setup questions. F9 key can be used for this operation.
Load custom defaults	N/A	Load custom defaults.
Save custom defaults	N/A	Save custom defaults.
Discard changes	N/A	Discard changes done so far to any of the setup questions.

The BIOS Setup Utility is a text-based utility that allows the user to configure the system and view current settings and environment information for the platform devices. The Setup Utility controls the platform's built-in devices.

The BIOS Setup interface consists of a number of pages or screens. Each page contains information or links to other pages. The first page in Setup displays a list of general categories as links. These links lead to pages containing a specific category's configuration.

The following sections describe the look and behavior for platform Setup.

4.1.5   Operation

BIOS Setup has the following features:

- Localization: BIOS Setup uses the Unicode standard and is capable of displaying Setup forms in all languages currently included in the Unicode standard. The Intel® Server Board BIOS will only be available in English.
- BIOS Setup is functional via console redirection over various terminal emulation standards. This may limit some functionality for compatibility, e.g., usage of colors or some keys or key sequences or support of pointing devices.

4.1.5.1   Setup Page Layout

The setup page layout is sectioned into functional areas. Each occupies a specific area of the screen and has dedicated functionality. The following table lists and describes each functional area.

Table 36. BIOS Setup Page Layout

Functional Area	Description
Title Bar	The title bar is located at the top of the screen and displays the title of the form (page) the user is currently viewing. It may also display navigational information.
Setup Item List	The Setup Item List is a set of controllable and informational items. Each item in the list occupies the left and center columns in the middle of the screen. The left column, the "Setup Item", is the subject of the item. The middle column, the "Option", contains an informational value or choices of the subject. A Setup Item may also be a hyperlink that is used to navigate formsets (pages). When it is a hyperlink, a Setup Item only occupies the "Setup Item" column.
Item Specific Help Area	The Item Specific Help area is located on the right side of the screen and contains help text for the highlighted Setup Item. Help information includes the meaning and usage of the item, allowable values, effects of the options, etc.
Keyboard Command Bar	The Keyboard Command Bar is located at the bottom right of the screen and continuously displays help for keyboard special keys and navigation keys. The keyboard command bar is context-sensitive—it displays keys relevant to current page and mode.
Status Bar	The Status Bar occupies the bottom line of the screen. This line would display the BIOS ID.

4.1.5.2   Entering BIOS Setup

BIOS Setup is started by pressing <F2> during boot time when the OEM or Intel logo is displayed.

When Quiet Boot is disabled, there will be a message "press <F2> to enter setup" displayed on the diagnostics screen.

4.1.5.3   Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the major menu selections available to the user.

4.2   Flash Memory Update Utility

4.2.1   BIOS Update

4.2.1.1   DOS Flash Utility

The BIOS can be upgraded from a HDD, diskette or CD-ROM using the Intel® iFlash Utility. This utility supports the following functions:
- Updates the BIOS from a file or file set
- Verifies that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- RPM support (this includes VBIOS update, etc.). RPM support is a stretch goal.

4.2.1.2   iFlash Update Version Checking

When Flash BIOS Updates and Flash Language Updates are performed, a certain amount of identification information will be checked before allowing the process to proceed. This checking prevents a BIOS from being flashed into the wrong system, possibly causing boot failure. This checking also prevents an incoherent language file from being flashed into a functional machine.

4.2.1.3   Standard Flash BIOS Updates

Whenever a Flash BIOS Update is performed, the Board Identifier, the Board Revision and the OEM Identifier must match.

4.2.1.4   Flash Language Updates

Whenever Flash Language Updates are performed, the Board Identifier, Board Revision, OEM Identifier and Build Identifier must match.

4.2.1.5   RPM (Replaceable Program Modules) Updates

Whenever RPM operations are performed, the Board Identifier and Board Revision must match. This currently only applies to video OPROM code.

- RPM support is a stretch goal.

4.2.2   O/S Present Flash Utility

The BIOS can be upgraded from a HDD, diskette or CD-ROM using the Intel® Express BIOS Update utility. This utility supports the following functions:

- Updates the BIOS from a file or file set
- Verifies that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- Works under Microsoft Windows 2000* and Microsoft Windows XP*

4.3 DMI/SMBIOS Support

4.3.1   DMI/SMBIOS Write Tool

A DMI/SMBIOS write utility allows OEMs to write their specific data into SMBIOS structures type 1 and 3 (chassis info – asset tag field only).

4.4   Operating System Boot, Sleep, and Wake

4.4.1   Boot Device Selection

The Boot Device Selection phase is responsible for controlling the boot of the system. The boot option variables are set by an operating system during operating system installation or manually added by the user through the Boot Maintenance Manager of Setup. The Boot Maintenance Manager provides the capability to make permanent changes to the boot order. It is also possible to change the first boot option for a single boot.

4.4.1.1   Server Management Boot Device Control

The IPMI 2.0 specification includes provisions for server management devices to set certain boot parameters by setting boot flags. Among the boot flags (parameter #5 in the IPMI specification) the BIOS will check data 1-3 for forced boot options.

The BIOS supports forced booting from the following:

- PXE
- HDD (USB, SATA and PATA)
- USB FDD
- USB key
- CD-ROM drive

On each boot, the BIOS invokes the *Get System Boot Options* command to determine what changes to boot options have been set. The BIOS takes the appropriate action and clears these settings.

4.4.2   Operating System Support

4.4.2.1   Microsoft Windows* Compatibility

Intel Corporation and Microsoft Corporation co-author design guides for system designers who will use Intel® processors and Microsoft* operating systems. The *Hardware Design Guide for Microsoft Windows 2000 Server*, Version 3.0 is intended for systems that are designed to work

with Windows Server* class operating systems. The specification further classifies the systems and includes sets of requirements based on the intended usage for that system. For example, a server system that is used in small home / office environments has different requirements than one used for enterprise applications.

This product supports the *Hardware Design Guide for Microsoft Windows 2000 Server*, Version 3.0 enterprise requirements.

4.4.2.2   Advanced Configuration and Power Interface (ACPI)

The primary role of the ACPI BIOS is to supply the ACPI tables. POST creates the ACPI tables and locates them in extended memory (above 1 MB). The location of these tables is conveyed to the ACPI-aware operating system through a series of tables located throughout memory. The format and location of these tables is documented in the publicly available ACPI specifications (*Advanced Configuration and Power Interface Specification*, Revision 1.0b and *Advanced Configuration and Power Interface Specification*, Revision 2.0).

The BIOS supports both ACPI 2.0 and 1.0b tables. To prevent conflicts with a non-ACPI-aware operating system, the memory used for the ACPI tables is marked as "reserved" in INT 15h, function E820h.

As described in the ACPI specifications, an ACPI-aware operating system generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by setting up all system (chipset) specific configurations required to support ACPI, issues the appropriate command to enable ACPI mode, and sets the SCI_EN bit as defined by the ACPI specification. The system automatically returns to legacy mode on hard reset or power-on reset.

There are three runtime components to ACPI:

- ▪ **ACPI Tables:**
  These tables describe the interfaces to the hardware. ACPI tables can make use of ACPI Machine Language (AML), the interpretation of which is performed by the operating system. The operating system contains and uses an AML interpreter that executes procedures encoded in AML and is stored in the ACPI tables. AML is a compact, tokenized, abstract machine language. The tables contain information about power management capabilities of the system, APICs, and bus structure. The tables also describe control methods that the operating system uses to change PCI interrupt routing, control legacy devices in the Super I/O, find out the cause of a wake event, and handle PCI hot plug, if applicable.

- ▪ **ACPI Registers:**
  This is the constrained part of the hardware interface, described (at least in location) by the ACPI tables.

- ▪ **ACPI BIOS:**
  This is the code that boots the machine and implements interfaces for sleep, wake, and some restart operations. The ACPI Description Tables are also provided by the ACPI BIOS.

The ACPI specification requires the system to support at least one sleep state. The BIOS supports S0, S1, S4, and S5 states. S1 is considered a sleep state.

This platform can wake up from S1 state using USB devices in addition to the sources described below.

The wake-up sources are enabled by the ACPI operating systems with cooperation from the drivers; the BIOS has no direct control over the wakeup sources when an ACPI operating system is loaded. The role of the BIOS is limited to describing the wakeup sources to the operating system and controlling secondary control / status bits via the Differentiated System Description Table (DSDT).

The S5 state is equivalent to operating system shutdown. No system context is saved when going into S5.

The OEM Table ID field of ACPI Tables are initialized with the Platform Identification string.

4.4.3   Front Control Panel Support

The platform supports a power button and a reset button on the control panel.

4.4.3.1   Power Button

The BIOS supports a front control panel power button. Pressing the power button initiates a request, which is forwarded to the ACPI power state machines in the chipset.

4.4.3.2   Reset Button

The platform supports a front control panel reset button. Pressing the reset button initiates a request to the chipset.

4.4.4   Sleep and Wake Support

4.4.4.1   System Sleep States

The platform supports the following ACPI system sleep states:

- ACPI S0 (working) state
- ACPI S1 (sleep) state
- ACPI S4 (hibernate) state
- ACPI S5 (soft-off) state

4.4.4.2   Wake Events / SCI Sources

The server board supports the following wake-up sources in the ACPI environment. The operating system controls enabling and disabling these wake sources:

- Devices that are connected to all USB ports, such as USB mice and keyboards can wake the system up from S1 sleep state.
- PCI devices, such as onboard NIC devices, can wake the system from the S4/S5 state.

As required by ACPI specification, the power button can wake the system from S1 state

5.   Server Management

The BIOS supports many standards-based server management features and several proprietary features.

5.1   Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM port). When console redirection is enabled, the local (host server) keyboard input and POST video output are passed both to the local keyboard and video connections, and to the remote console through the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs.

As an option, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console, including BIOS Setup.

5.1.1   Serial Configuration Settings

Both EMP and console redirection require N, 8, 1 mode (no parity, 8-bit data, 1 stop bit).

The BIOS does not require that the splash logo be turned off for console redirection to function. The BIOS supports multiple consoles, some of which are in graphics mode and some in text mode. The graphics consoles can display the logo and the text consoles can receive the redirected text.

Console redirection ends at the beginning of the legacy operating system boot (INT 19h). The operating system is responsible for continuing the redirection from that point.

5.1.2   Keystroke Mappings

During console redirection, the remote terminal sends keystrokes to the local server. The remote terminal may be a dumb terminal with a direct connection running a communication program. The keystroke mappings follow VT-UTF8 format with the following extensions.

5.1.2.1   Setup Alias Keys

The <Del> and <Ctrl>-function key combinations are synonyms for the <F2> or "Setup" key. They are implemented and documented, but are not to be prompted for in screen messages. These hot keys are defined for console redirection support, and are not to be implemented for locally attached keyboards.

5.1.2.2   Standalone <Esc> Key for Headless Operation

The *Microsoft Headless Design Guidelines* describes a specific implementation for the <Esc> key as a single standalone keystroke:

- <Esc> followed by a two-second pause must be interpreted as a single escape.
- <Esc> followed within two seconds by one or more characters that do not form a sequence described in this specification must be interpreted as <Esc> plus the character or characters, not as an escape sequence.

The escape sequence in the following table is an input sequence. This means it is sent to the BIOS from the remote terminal.

Table 37. Console Redirection Escape Sequences for Headless Operation

Escape Sequence	Description
<Esc>R<Esc>r<Esc>R This will implement but will default to "disabled".	Remote Console Reset

5.1.3 Limitations

- BIOS Console redirection terminates after an EFI-aware operating system calls EFI Exit Boot Services. The operating system is responsible for continuing console redirection after that.
- BIOS console redirection is a text console. Graphical data, such as a logo, are not redirected.

5.2 Intel® Active Management Technology (AMT)

Intel Active Management Technology architecture is based on market demand for a platform management solution that provides remote management capabilities independent of system power states. The Intel® AMT architecture is centered around the Intel® ICH7R IO controller and Intel® 82573E Gigabit LAN components. The ICH7R provides an interface to a new SPI flash device for potential cost savings.

Because Intel® AMT depends on the availability of the Intel® 82573E PCI manageability functions, the Intel® AMT does not operate with third-party LANs.

The main objectives of Intel AMT are:

- **Deployable** – Intel® AMT uses existing protocols and services available in today's IT networks to minimize cost. Intel® AMT is constrained to the use of DHCP, DNS, SOAP/XML/HTTP, and TLS; which are available on most IT networks today.
- **Highly Available –** The ability to provide remote management in the event of operating system or hardware failure. Intel® AMT provides baseline services whenever there is (at the minimum) auxiliary power available to the platform. Currently, system auxiliary power is maintained by the main power supply when the system is plugged into the wall. This will significantly reduce IT expenses for system repair.
- **OS-Independent Agent** – Baseline platform management capabilities that simplify system management running different operating system types and versions. Intel® AMT provides common remote management and persistent storage features that run independently of the operating system.
- **Secure and Tamper Resistant** - Intel® AMT provides access control, data security, and protection against attacks by using standard security protocols (e.g., TLS) and application-level security mechanisms. Intel® AMT also provides tamper resistance to prevent the end-user from removing or disabling remote management service.

Intel® 82573E is a multi-functional device with an embedded microcontroller for manageability purposes. Manageability functions of the Intel® 82573E PCI are as follows:

- IDE-R – for remote boot and SW installation
- Serial Port – for Keyboard and text redirection
- KCS – for configuration of the manageability content

The Intel® 82573E controller is a PCI Express* GBit Ethernet endpoint device, the first GbE controller to support Intel® AMT as the next-generation client manageability architecture. Intel® 82573E provides three PCI functions for management purposes: serial port, IDE, and KCS. When the Intel® AMT is disabled, the Intel® 82573E controller disables these three PCI functions. When these management functions are disabled, the functions do not response to PCI configuration cycles (effectively becoming invisible to software). When Intel® AMT is enabled, the Intel® 82573E controller enables the PCI functions, which appear to software as standard PCI devices.

Serial Port Function: The Serial Port function supports redirection of keyboard and POST messages to a terminal window on a remote console. The keyboard and text redirection enables the control of the client machine through the network without the need to be physically near that machine. Text and keyboard redirection allows the remote machine to monitor POST progress of the client machine and allows the remote machine to control and configure the client by entering BIOS Setup. The Intel® 82573E controller redirects data from the serial port to the management console via the LAN; hence, providing Serial Over LAN (SOL) capability.

IDE Function: The IDE function provides IDE-R, an IDE redirection interface that provides client connection to management console ATA/ATAPI devices. When booting from IDE-R, the IDE-R interface will send the client's ATA/ATAPI command to the management console. The management console responds back to the client. A remote machine can setup diagnostic software or an operating system installation image and direct the client to boot from IDE-R. The IDE-R interface is the same as the IDE interface and is compliant with ATA/ATAPI-6 specifications. IDE-R does not conflict with the usage of PXE boot. The system can support both interfaces and can continue to boot from PXE as with any other boot devices. However, during a management boot session, the Intel® AMT solution will use IDE-R when remote boot is required. The devices attached to the IDE-R channel are only visible to software during a management boot session. During a normal boot session, the IDE-R channel appears as no device present.

KCS Function: The KCS (Keyboard Controller Style) function provides a physical interface used to convey messages between the host software and the AMT device. The KCS function defines a set of memory-mapped IO (MMIO) registers. These MMIO registers follow the usage model used in the Intel® 8742 Universal Peripheral Interface microcontroller. The term 'Keyboard Controller Style' reflects the fact that the Intel® 8742 interface is used as the system keyboard controller interface in PC architecture computer systems.

The AMT BIOS Extension (AMTx) is provided by Intel and is included in the system BIOS at build time. The AMTx Module communicates with the Intel® 82573E firmware via the KCS interface. The AMTx Module collects system hardware configuration via ACPI and the SMBIOS tables, and sends hardware information to the remote management system via the KCS interface.

Table 38. Function List

Function	Vendor ID	Device ID
Intel® 82573E Lan	0x8086	0x108B/0x108C (V/E)
IDE	0x8086	0x108D
Serial Port	0x8086	0x108F
KCS	0x8086	0x108E

5.3 Wired For Management (WFM)

Wired for Management is an industry-wide initiative to increase overall manageability and reduce total cost of ownership. WFM allows a server to be managed over a network. The system BIOS supports the *System Management BIOS Reference* Specification, Version 2.4 to help higher-level instrumentation software meet the *Wired For Management Baseline Specification*, Revision 2.0 requirements.

5.3.1 PXE BIOS Support

The BIOS supports the EFI PXE implementation as specified in Chapter 15 of the *Extensible Firmware Interface Reference Specification*, Version 1.1. To utilize this, the user must load the EFI Simple Network Protocol driver. The UNDI driver is specific to the network controller and must be included with the network card. The Simple Network Protocol driver can be obtained from http://developer.intel.com/technology/framework.

The BIOS supports legacy PXE option ROMs in legacy mode and includes the necessary PXE ROMs in the BIOS image for the onboard controllers. The legacy PXE ROM is required to boot a non-EFI operating system over the network.

5.4 System Management BIOS (SMBIOS)

The BIOS provides support for the *System Management BIOS Reference* Specification, Version 2.4 to create a standardized interface for manageable attributes that are expected to be supported by DMI-enabled computer systems. The BIOS provides this interface via data structures through which the system attributes are reported. Using SMBIOS, a system administrator can obtain the types, capabilities, operational status, installation date and other information about the server components.

5.5 Security

The BIOS provides several security features. This section describes the security features and operating model.

5.5.1 Operating Model

The following table summarizes the operation of security features supported by the BIOS.

Table 39. Security Features Operating Model

Mode	Entry Method / Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Password on boot	Power On / Reset	User password set and password on boot enabled in BIOS Setup. Secure boot disabled in BIOS Setup.	System halts for user password before scanning option ROMs. The system is not in secure mode. No mouse or keyboard input is accepted except the password.	User password. Administrator password.	Front control panel buttons are re-enabled. The server boots normally. Boot sequence is determined by setup options.

5.5.2 Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the server setup. Both user and administrator passwords are supported by the BIOS. An Administrator password must be entered in order to set the user password. The maximum length of a password can be seven characters. The password cannot have characters other than alphanumeric (a-z, A-Z, 0-9). It is not case sensitive.

Once set, a password can be cleared by changing it to a null string. Entering the user password will allow the user to modify the time, date, and user password. Other setup fields can be modified only if the administrator password is entered. If only one password is set, this password is required to enter BIOS Setup.

The administrator has control over all fields in BIOS Setup, including the ability to clear the user password.

If the user or administrator enters an incorrect password three times in a row during the boot sequence, the system is placed into a halt state. A system reset is required to exit out of the halt state. This feature makes it difficult to break the password by guessing at it.

5.5.3 Password Clear Jumper

If the user and/or administrator password is lost or forgotten, both passwords may be cleared by moving the password clear jumper into the clear position. The BIOS determines if the password clear jumper is in the clear position during BIOS POST and clears any passwords if required. The password clear jumper must be restored to its original position before a new password can be set.

6.   Error Reporting and Handling

This chapter defines the following error handling features:

- ▪ Error Handling and Logging
- ▪ Error Messages and Beep Codes

6.1   Error Handling and Logging

This section defines how errors are handled by the system BIOS. In addition, error-logging techniques are described and beep codes for errors are defined.

6.1.1   Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors that can be enabled and disabled individually or as a group can be categorized as follows:

- ▪ PCI bus
- ▪ Memory single- and multi-bit errors
- ▪ Errors detected during POST, logged as POST errors

The error list that would be logged is as follows:

Table 40. Event List

Event Name	Description	When Error Is Caught
Processor thermal trip of last boot	Processor thermal trip happened on last boot.	POST
Memory channel A Multi-bit ECC error	Multi-bit ECC error happened on DIMM channel A.	POST / Runtime
Memory channel A Single-bit ECC error	Single-bit ECC error happened on DIMM channel A.	POST / Runtime
Memory channel B Multi-bit ECC error	Multi-bit ECC error happened on DIMM channel B.	POST / Runtime
Memory channel B Single-bit ECC error	Single-bit ECC error happened on DIMM channel B.	POST / Runtime
CMOS battery failure	CMOS battery failure or CMOS clear jumper is set to clear CMOS.	POST
CMOS checksum error	CMOS data crushed	POST
CMOS time not set	CMOS time is not set	POST
Keyboard not found	PS/2 KB is not found during POST	POST
Memory size decrease	Memory size is decreased compared with last boot	POST
Chassis intrusion detected	Chassis is open	POST
Bad SPD tolerance	Some fields of the DIMM SPD may not be supported, but could be tolerated by the Memory Reference Code.	POST

PCI PERR error	PERR error happens on PCI bus	POST / Runtime
PCI SERR error	SERR error happens on PCI bus	POST / Runtime

6.1.2   Error Logging via SMI Handler

The SMI handler is used to handle and log system level events. The SMI handler pre-processes all system errors, even those that are normally considered to generate an NMI.

The SMI handler logs the event to NVRAM. For example, the BIOS programs the hardware to generate a SMI on a single-bit memory error and logs the error in the NVRAM in terms of a SMBIOS Type 15. After the BIOS finishes logging the error it will assert the NMI if needed.

6.1.2.1   PCI Bus Error

The PCI bus defines two error pins, PERR# and SERR#. These are used for reporting PCI parity errors and system errors, respectively.

In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. All PCI-to-PCI bridges are configured so that they generate SERR# on the primary interface whenever there is SERR# on the secondary side.

6.1.2.2   PCI Express* Errors

Fatal and critical PCI Express* errors are logged as PCI system errors and are promoted to an NMI. All non-critical PCI Express errors are logged as PCI parity errors.

6.1.2.3   Memory Errors

The hardware is programmed to generate an SMI on correctable data errors in the memory array. The SMI handler records the error to the NVRAM. The uncorrectable errors may have corrupted the contents of SMRAM. The SMI handler will log the error to the NVRAM if the SMRAM contents are still valid.

6.1.3   SMBIOS Type 15

Errors are logged to the NVRAM in terms of the SMBIOS Type 15 (System Event Log). Please refer to the *SMBIOS Specification*, version 2.4 for more detail information. The format of the records is also defined in the following section.

6.1.4   Logging Format Conventions

The BIOS logs an error into the NVRAM area with the following record format, which is also defined in the *SMBIOS Specification*, version 2.3.4.

Table 41. Logging Format Conventions

Offset	Name	Length	Description
00h	EventType	Byte	Specifies the "Type" of event noted in an event-log entry as defined in table.
01h	Length	Byte	Specifies the byte length of the event record, including the record's Type and Length fields.
02h	Year	Byte	Indicates the time when error is logged.
03h	Month	Byte	
04h	Day	Byte	
05h	Hour	Byte	
06h	Minute	Byte	
07h	Second	Byte	
08h	EventData1	DWORD	EFI_STATUS_CODE_TYPE
0Ch	EventData2	DWORD	EFI_STATUS_CODE_VALUE

Table 42. Event Type Definition Table

Value	Description	Used by this platform (Y/N)
00h	Reserved	N
01h	Single-bit ECC memory error	Y
02h	Multi-bit ECC memory error	Y
03h	Parity memory error	N
04h	Bus time-out	N
05h	I/O Channel Check	N
06h	Software NMI	N
07h	POST Memory Resize	N
08h	POST Error	Y
09h	PCI Parity Error	Y
0Ah	PCI System Error	Y
0Bh	CPU Failure	N
0Ch	EISA FailSafe Timer time-out	N
0Dh	Correctable memory log disabled	N
0Eh	Logging disabled for a specific Event Type – too many errors of the same type received in a short amount of time	N
0Fh	Reserved	N
10h	System Limit Exceeded (e.g. voltage or temperature threshold exceeded)	Y
11h	Asynchronous hardware timer expired and issued a system reset	N
12h	System configuration information	N
13h	Hard-disk information	N
14h	System reconfigured	N
15h	Uncorrectable CPU-complex error	N
16h	Log Area Reset/Cleared	Y
17h	System boot. If implemented, this log entry is guaranteed to be the first one written on any system boot.	N

18h-7Fh	Unused, available for assignment by SMBIOS Specification Version 2.3.4.	N
80h-FEh	Available for system- and OEM-specific assignments	Y
FFh	End-of-log. When an application searches through the event-log records, the end of the log is identified when a log record with this type is found.	Y

For more information about the EFI_STATUS_CODE_TYPE and EFI_STATUS_CODE_VALUE definitions, refer to "Intel Platform Innovation Framework for EFI Status Codes Specification", version 0.92.

The errors are also displayed on the BIOS Setup screen under Server Management / View EventLog menu in the following format:

> EventName (times)   Time of Occurrence

EventName is the same as that shown in the Table 58. It is followed by the number of occurrences of the same event. The 'Time of Occurrence' is the last time the event occurred.

6.2   Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Before video initialization, beep codes inform the user of errors. POST error codes are logged in the event log. The BIOS displays POST error codes on the video monitor.

6.2.1   Diagnostic LEDs

During the system boot process, the BIOS executes several platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS will display the POST code on the POST code diagnostic LEDs found on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, the diagnostic LEDs can be used to identify the last POST process to be executed.

Each POST code is represented by a combination of colors from the four LEDs. The LEDs are capable of displaying three colors: green, red, and amber. The POST codes are divided into an upper nibble and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibbles then both red and green LEDs are lit, resulting in an amber color. If both bits are clear, then the LED is off.

In the below example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

- Red bits = 1010b = Ah
- Green bits = 1100b = Ch

Since the red bits correspond to the upper nibble and the green bits correspond to the lower nibble, the two are concatenated to be ACh.

Table 43. POST Progress Code LED Example

	8h		4h		2h		1h	
LEDs	**Red**	**Green**	**Red**	**Green**	**Red**	**Green**	**Red**	**Green**
ACh	1	1	0	1	1	0	0	0
Result	Amber		Green		Red		Off	
	MSB						LSB	
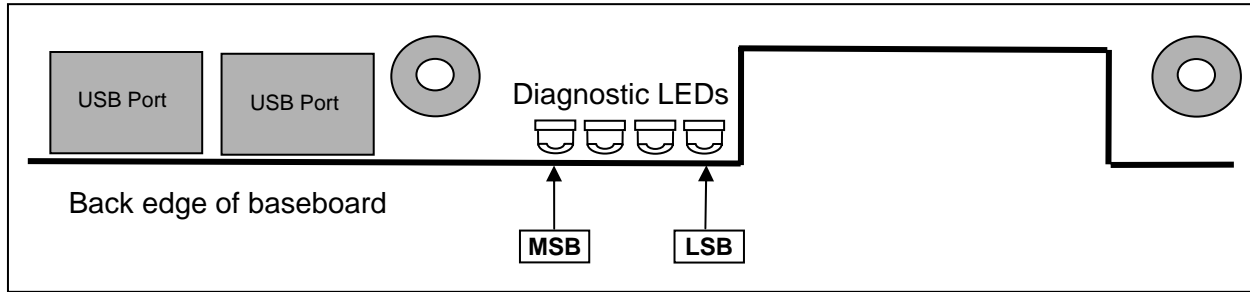
Figure 6. Location of Diagnostic LEDs on Server Board

6.2.2　　POST Code Checkpoints

Table 44. POST Code Checkpoints

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			**LSB**	
Host Processor					
0x10h	OFF	OFF	OFF	R	Power-on initialization of the host processor (bootstrap processor)
0x11h	OFF	OFF	OFF	A	Host processor cache initialization (including AP)
0x12h	OFF	OFF	G	R	Starting application processor initialization
0x13h	OFF	OFF	G	A	SMM initialization
Chipset					
0x21h	OFF	OFF	R	G	Initializing a chipset component
Memory					
0x22h	OFF	OFF	A	OFF	Reading configuration data from memory (SPD on DIMM)
0x23h	OFF	OFF	A	G	Detecting presence of memory
0x24h	OFF	G	R	OFF	Programming timing parameters in the memory controller
0x25h	OFF	G	R	G	Configuring memory parameters in the memory controller
0x26h	OFF	G	A	OFF	Optimizing memory controller settings
0x27h	OFF	G	A	G	Initializing memory, such as ECC init
0x28h	G	OFF	R	OFF	Testing memory
PCI Bus					
0x50h	OFF	R	OFF	R	Enumerating PCI busses

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			**LSB**	
0x51h	OFF	R	OFF	A	Allocating resources to PCI busses
0x52h	OFF	R	G	R	Hot Plug PCI controller initialization
0x53h	OFF	R	G	A	Reserved for PCI bus
0x54h	OFF	A	OFF	R	Reserved for PCI bus
0x55h	OFF	A	OFF	A	Reserved for PCI bus
0x56h	OFF	A	G	R	Reserved for PCI bus
0x57h	OFF	A	G	A	Reserved for PCI bus
USB					
0x58h	G	R	OFF	R	Resetting USB bus
0x59h	G	R	OFF	A	Reserved for USB devices
ATA / ATAPI / SATA					
0x5Ah	G	R	G	R	Begin PATA / SATA bus initialization
0x5Bh	G	R	G	A	Reserved for ATA
SMBUS					
0x5Ch	G	A	OFF	R	Resetting SMBUS
0x5Dh	G	A	OFF	A	Reserved for SMBUS
Local Console					
0x70h	OFF	R	R	R	Resetting the video controller (VGA)
0x71h	OFF	R	R	A	Disabling the video controller (VGA)
0x72h	OFF	R	A	R	Enabling the video controller (VGA)
Remote Console					
0x78h	G	R	R	R	Resetting the console controller
0x79h	G	R	R	A	Disabling the console controller
0x7Ah	G	R	A	R	Enabling the console controller
Keyboard (PS2 or USB)					
0x90h	R	OFF	OFF	R	Resetting the keyboard
0x91h	R	OFF	OFF	A	Disabling the keyboard
0x92h	R	OFF	G	R	Resetting the keyboard
0x93h	R	OFF	G	A	Enabling the keyboard
0x94h	R	G	OFF	R	Clearing keyboard input buffer
0x95h	R	G	OFF	A	Instructing keyboard controller to run Self Test (PS2 only)
Mouse (PS2 or USB)					
0x98h	A	OFF	OFF	R	Resetting the mouse
0x99h	A	OFF	OFF	A	Detecting the mouse
0x9Ah	A	OFF	G	R	Detecting the presence of mouse
0x9Bh	A	OFF	G	A	Enabling the mouse
Fixed Media					
0xB0h	R	OFF	R	R	Resetting fixed media device
0xB1h	R	OFF	R	A	Disabling fixed media device
0xB2h	R	OFF	A	R	Detecting presence of a fixed media device (IDE hard drive detection, etc.)
0xB3h	R	OFF	A	A	Enabling / configuring a fixed media device
Removable Media					

Checkpoint	Diagnostic LED Decoder				Description
	G=Green, R=Red, A=Amber				
	MSB			LSB	
0xB8h	A	OFF	R	R	Resetting removable media device
0xB9h	A	OFF	R	A	Disabling removable media device
0xBAh	A	OFF	A	R	Detecting presence of a removable media device (IDE CDROM detection, etc.)
0xBCh	A	G	R	R	Enabling / configuring a removable media device
Boot Device Selection					
0xD0	R	R	OFF	R	Trying boot device selection
0xD1	R	R	OFF	A	Trying boot device selection
0xD2	R	R	G	R	Trying boot device selection
0xD3	R	R	G	A	Trying boot device selection
0xD4	R	A	OFF	R	Trying boot device selection
0xD5	R	A	OFF	A	Trying boot device selection
0xD6	R	A	G	R	Trying boot device selection
0xD7	R	A	G	A	Trying boot device selection
0xD8	A	R	OFF	R	Trying boot device selection
0xD9	A	R	OFF	A	Trying boot device selection
0XDA	A	R	G	R	Trying boot device selection
0xDB	A	R	G	A	Trying boot device selection
0xDC	A	A	OFF	R	Trying boot device selection
0xDE	A	A	G	R	Trying boot device selection
0xDF	A	A	G	A	Trying boot device selection
Pre-EFI Initialization (PEI) Core					
0xE0h	R	R	R	OFF	Started dispatching an PEIM
0xE1h	R	R	R	G	Completed dispatching an PEIM
0xE2h	R	R	A	OFF	Initial memory found, configured, and installed correctly
0xE3h	R	R	A	G	Reserved for initialization module use (PEIM)
Driver eXecution Environment (DXE) Core					
0xE4h	R	A	R	OFF	Entered EFI driver execution phase (DXE)
0xE5h	R	A	R	G	Reserved for DXE core use
0xE6h	R	A	A	OFF	Started connecting drivers
0xEBh	A	R	A	G	Started dispatching a driver
0xECh	R	A	A	OFF	Completed dispatching a driver
DXE Drivers					
0xE7h	R	A	A	G	Waiting for user input
0xE8h	A	R	R	OFF	Checking password
0xE9h	A	R	R	G	Entering BIOS setup
0xEAh	A	R	A	OFF	Flash Update
0xEEh	A	A	A	OFF	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	A	A	A	G	Reserved for DXE Drivers use
Runtime Phase / EFI Operating System Boot					
0xF4h	R	A	R	R	Entering Sleep state
0xF5h	R	A	R	A	Exiting Sleep state

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
0xF8h	A	R	R	R	Operating system has requested EFI to close boot services (ExitBootServices ( ) has been called)
0xF9h	A	R	R	A	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) has been called)
0xFAh	A	R	A	R	Operating system has requested the system to reset (ResetSystem () has been called)
Pre-EFI Initialization Module (PEIM) / Recovery					
0x30h	OFF	OFF	R	R	Crisis recovery has been initiated because of a user request
0x31h	OFF	OFF	R	A	Crisis recovery has been initiated by software (corrupt flash)
0x34h	OFF	G	R	R	Loading crisis recovery capsule
0x35h	OFF	G	R	A	Handing off control to the crisis recovery capsule
0x3Fh	G	G	A	A	Unable to complete crisis recovery.

6.2.3   POST Error Messages and Handling

Whenever possible, the BIOS will output the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response column in the following table is divided into two types:

- **Pause:** The message is displayed in the Error Manager screen, an error may be logged to the NVRAM, and user input is required to continue. The user can take immediate corrective action or choose to continue booting.
- **Halt:** The message is displayed in the Error Manager screen, an error is logged to the NVRAM, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

Table 45. POST Error Messages and Handling

Error Code	Error Message	Response	Log Error
	CMOS date / time not set	Pause	Y
	Configuration cleared by jumper	Pause	Y
	Configuration default loaded	Pause	N
	Password check failed	Halt	N
	PCI resource conflict	Pause	N
	Insufficient memory to shadow PCI ROM	Pause	N
	Processor thermal trip error on last boot	Pause	Y

6.2.4   POST Error Beep Codes

The following table lists the POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users of error conditions. The beep code is followed by a user visible code on the POST Progress LEDs.

Table 46. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error		System halted because a fatal error related to the memory was detected.

6.2.5   POST Error Pause Option

In the event of POST error(s) that are listed as "Pause", the BIOS will enter the error manager and wait for the user to press an appropriate key before booting the operating system or entering BIOS Setup.

The user can override this option by setting "POST Error Pause" to "disabled" in the BIOS Setup main menu page. If the "POST Error Pause" option is set to "disabled", the system will boot the operating system without user intervention. The default value is set to "enabled".

7.   Connectors and Jumper Blocks

7.1   Power Connectors

The power supply connection is supplied to the system through the 18-pin connector. The following table defines the pin-outs of the connector.

Table 47. Power Connector Pin-out (J3K1)

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1*	+3.3VDC	Orange	10	+3.3VDC	Orange
	3.3V RS	Orange (24AWG)	11	-12VDC	Blue
2	COM	Black	12	COM	Black
3*	COM	Black	13	PSON#	Green
	COM RS	Black (24AWG)	14	+5VDC	Red
4*	+5VDC	Red	15	+12V1	Yellow
	5V RS	Red (24AWG)	16	COM	Black
5	5 VSB	Purple	17	COM	Black
6	COM	Black	18	+12V3	Yellow
7	COM	Black			
8	+12V1	Yellow			
9	+12V2	Yellow			

7.2   I^{2}C Header

Table 48. HSBP Header Pin-out (J1C1)

Pin	Signal Name	Description
1	SMB_DATA_5V_BP	Data Line
2	GND	GROUND
3	SMB_CLK_5V_BP	Clock Line
4	GND	GROUND

7.3   Front Panel Connector

A standard SSI 34-pin header is provided to support a system front panel. The header contains reset, NMI, power control buttons, and LED indicators. The following table details the pin-out of this header.

Table 49. Front Panel 14-pin Header Pin-out (J4k2)

Signal Name	Pin	Signal Name	Pin
Power LED Anode	1	NIC1 Activity LED Anode	2
Power LED Cathode	3	NIC1 Activity LED Cathode	4
HDD Activity LED Anode	5	NIC2 Activity LED Anode	6
HDD Activity LED Cathode	7	NIC2 Activity LED Cathode	8
Power Switch	9	Reset Switch	10
Power Switch(GND)	11	Reset Switch(GND)	12
Key	13	NC	14

Note: NC (No Connect)

7.4   I/O Connectors

7.4.1   VGA Connector

The following table details the pin-out of the VGA connector. This connector is combined with the COM1 connector.

Table 50. VGA Connector Pin-out (J3A1)

Signal Name	Pin	Signal Name	Pin
RED	B1	Fused VCC (+5V)	B9
GREEN	B2	GND	B10
BLUE	B3	NC	B11
NC	B4	DDCDAT	B12
GND	B5	HSY	B13
GND	B6	VSY	B14
GND	B7	DDCCLK	B15
GND	B8		

Note: NC (No Connect)

7.4.2 NIC Connectors

The Intel® Entry Server Board SE7230CA1-E supports two NIC RJ-45 connectors. The following tables detail the pin-out of the connector.

Table 51. NIC1-Intel® 82573E (10/100/1000) Connector Pin-out (JA5A1)

Signal Name	Pin	Signal Name	Pin
P2V5_NIC1	9	NIC1_MDI3_DP	16
NIC1_MDI0_DP	10	NIC1_MDI3_DN	17
NIC1_MDI0_DN	11	GND	18
NIC1_MDI1_DP	12	NIC1_LINK_1_N	19
NIC1_MDI1_DN	13	P3V3_AUX	20
NIC1_MDI2_DP	14	NIC1_LINK_0_N	21
NIC1_MDI2_DN	15	NIC1_LINK_2_N	22

Table 52. NIC2- Intel® 82541PI (10/100/1000) Connector Pin-out (JA4A1)

Signal Name	Pin	Signal Name	Pin
P1V8_NIC_RC	1	NIC2_MDI3_DN	9
NIC2_MDI2_DN	2	NIC2_MDI0_DN	10
NIC2_MDI2_DP	3	NIC2_MDI0_DP	11
NIC2_MDI1_DP	4	P1V8_NIC_RC	12
NIC2_MDI1_DN	5	NIC2_LINK1000_N	13
P1V8_NIC_RC	6	NIC2_LINK100_N	14
P1V8_NIC_RC	7	NIC2_ACT_LED_N	15
NIC2_MDI3_DP	8	NIC2_LINK_UP_N	16

7.4.3 SATA Connectors

The Intel® ICH7R integrates a SATA controller with four SATA ports. The pin-out for these four connectors is listed below.

Table 53. SATA Connector Pin-out (J5C1, J5C2)

Pin	Signal Name
1	GND
2	SATA0_TX_P
3	SATA0_TX_N
4	GND
5	SATA0_RX_N
6	SATA0_RX_P
7	GND

7.4.4 Serial Port Connectors

One serial port is provided on the Intel® Entry Server Board SE7230CA1-E. A standard, external DB9 serial connector is located on the back edge of the server board to supply a Serial A interface. This connector is combined with the VGA connector (J3A1). An internal 9-pin header supplies a Serial B interface.

Table 54. External DB9 Serial A Port Pin-out (J3A1)

Signal Name	Pin	Signal Name	Pin
DCD	T1	DSR	T6
RXD	T2	RTS	T7
TXD	T3	CTS	T8
DTR	T4	RI	T9
GND	T5		

Table 55. Internal 9-pin Serial B Port Pin-out (J1C2)

Signal Name	Pin	Signal Name	Pin
DCD	1	CTS	6
DSR	2	DTR	7
RX	3	RI	8
RTS	4	GND	9
TX	5		

7.4.5　USB Connector

The following table provides the pin-out for the dual external USB connectors. This connector is combined with an RJ-45 (connected to NIC1 signals).

Table 56. USB Connectors Pin-out (JA5A1)

Pin	Signal Name
U1	P5V_USB_BP_MJ
U2	USB_BACK5_R_DN
U3	USB_BACK5_R_DP
U4	GND
U5	P5V_USB_BP_MJ
U6	USB_BACK4_R_DN
U7	USB_BACK4_R_DP
U8	GND

A header on the server board provides an option to support two additional USB ports. The pin-out of the header is detailed in the following table.

Table 57. Optional USB Connection Header Pin-out (J9F2)

Signal Name	Pin	Signal Name	Pin
NC	1	Key	2
GND	3	GND	4
USB_FRONT1_INDUCTOR_DP	5	USB_FRONT2_INDUCTOR_DP	6
USB_FRONT1_INDUCTOR_DN	7	USB_FRONT2_INDUCTOR_DN	8
USB_FNT_PWR (Fused VCC, +5V /w over current monitor of both port 1)	9	USB_FNT_PWR (Fused VCC, +5V /w over current monitor of both port 1)	10

7.5   Fan Headers

There are two general-purpose (system) fan headers (J3K2, J4K1). These fan headers have the same pin-out and are detailed below.

Table 58. Four-pin Fan Headers Pin-out (J3K2, J4K1)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Fan Power +12VDC
3	Fan Tach	Out	FAN_TACH signal is connected to the Heceta* to monitor the fan speed.
4	PWM	Control	Pulse Width Modulation – Fan speed Control signal

7.6   Miscellaneous Headers and Connectors

7.6.1   Chassis Intrusion Header

A 1x2 pin header (J3B2) is used in the chassis to support a chassis intrusion switch. The pin-out definition for this header is found in the following table.

Table 59. Intrusion Cable Connector (J3B2) Pin-out

Pin	Signal Name
1	FP_INTRUDER_HDR_P1(Power)
2	FP_INTRUDER_HDR_N

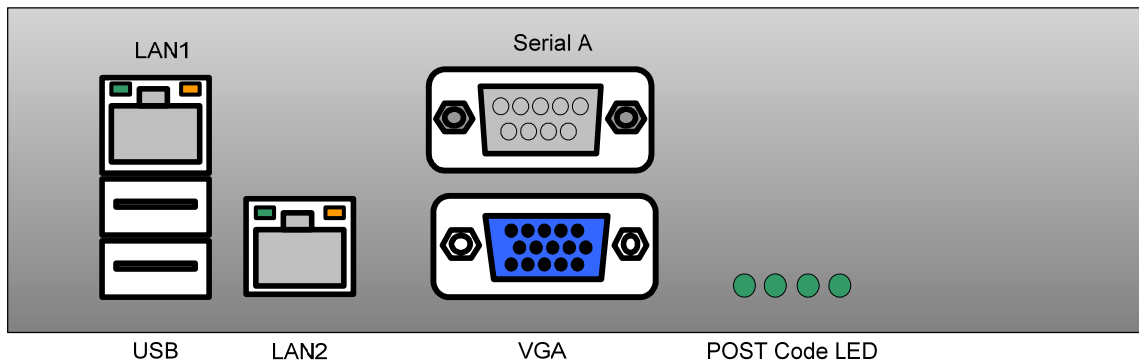### 7.6.2   Back Panel I/O Connectors

Figure 7. Back Panel I/O Connections (not to scale)

7.6.3 POST Code LEDs
Four POST code LEDs display POST code progression activities using hexadecimal format, read from the least significant bit to the most significant bit.

7.7   Jumper Blocks

This section describes configuration jumper options on the Intel® Entry Server Board SE7230CA1-E.

7.7.1   Clear CMOS and System Maintenance Mode Jumpers

Both the CMOS Clear and the system maintenance mode jumpers consist of 3-pin headers (CMOS Clear = J3B1, Config Mode = J1A3) located just beside the Front panel and SATA 1 connectors. The Intel® Entry Server Board SE7230CA1-E provides two 3-pin jumper blocks that are used to perform clearing of NVRAM and system maintenance mode options. The factory defaults are set to Normal mode for each function.

The following tables describe each jumper option.

Table 60. System Maintenance Mode (J1A3)

Name	Pin – Pin	Function	Description
Normal	1-2	Normal operation	Allows normal system operation with correct BIOS settings. System will POST normally.
Config (Maintenance)	2-3	Machine Config Mode	Maintenance mode overrides incorrect BIOS settings which would otherwise prohibit normal POST with safe settings for specific hardware configuration.
Recovery boot	Off	BIOS Recovery Mode	Used to recover from a corrupted BIOS.

Table 61. Clear CMOS Jumper Options (J3B2)

Name	Pin – Pin	Function	Description
Normal	1-2	Normal operation	Jumper in normal position allows system to successfully POST and boot to operating system environment. BIOS settings are maintained intact.
CMOS Clear	2-3	Clears CMOS (NVRAM)	Jumper in CLEAR position initiates clear of NVRAM following POST. System message confirms CMOS clear operation successful. This setting enforces default BIOS settings, which can be changed by entering setup via F2, then exiting setup via F10 and saving changes.

8.   Absolute Maximum Ratings

Operating the board at conditions beyond those shown in the following table may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 62. Absolute Maximum Ratings

Operating Temperature	5 °C to 50 °C [1]
Storage Temperature	-55 °C to +150 °C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:

1. Chassis design must provide proper airflow to avoid exceeding the processor maximum case temperature.

2. VDD means supply voltage for the device

8.1   Mean Time Between Failures (MTBF) Test Results

This section provides results of MTBF testing conducted by an Intel testing facility. MTBF is a standard measure for the reliability and performance of the board under extreme working conditions. For the Intel® Entry Server Board SE7230CA1-E, MTBF was measured at **40** degrees Centigrade.

9. Design and Environmental Specifications

9.1 Power Budget

The following table shows the power consumed on each supply line for the Intel® Entry Server Board SE7230CA1-E that is configured with one processor (130W max). This configuration includes four 1-GB DDR2 DIMMs stacked burst at 90% max. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at higher than average stress levels.

Table 63. The Board Power Budget

Watts			Power Supply Rail Voltages						Units
			AMPS						
Functional Unit	Utilization	Power	3.3V	5.V	12.V	12V VRM	-12v	5VSB	
Server Board Input Totals		260W	2.9	13.9	2.8	12.2	0.05	1.54	Amps
Server Board Discrete Totals	50%	45W	2.9	0.5	0.00	0.00	0.00	0.04	Amps
Server Board Converters	Efficiency	40W	0.00	13.4	0.00	12.2	0.00	1.5	Amps
Server Board Config Totals		175.8W	0.00	0.00	2.8	0.00	0.05	0.00	Amps
System Components		29W	0.00	2.8	3.6	0.00	0.00	0.00	Amps
System Totals		291W	2.9	15.2	4.7	12.2	0.05	1.54	Amps
3.3V / 5V Combined Power									
Power Supply Requirements – 1U		300W	14A	18A	Max 12V+ 12V VRM		0.5A	2A	
		350W peak							
3.3V/5V Combined Power		100W	1Amin	1Amin	2Amin	2Amin	0Amin	1Amin	

9.2 Product Regulatory Compliance

9.2.1 Product Safety Compliance

The Intel® Entry Server Board SE7230CA1-E complies with the following safety requirements:

- UL60950 – CSA 60950(USA / Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate and Report, IEC60950 (report to include all country national deviations)

▪ CE - Low Voltage Directive 73/23/EEE (Europe)

9.2.2   Product EMC Compliance – Class A Compliance

Note: Legally the product is required to comply with Class A emission requirements as it is intended for a commercial type market place. Intel targets 10db margin to Class A Limits

The Intel® Entry Server Board SE7230CA1-E has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel® host system. For information on compatible host system(s), refer to Intel's Server Builder Web site or contact your local Intel representative.

▪ FCC /ICES-003 - Emissions (USA/Canada) Verification
▪ CISPR 22 – Emissions (International)
▪ EN55022 - Emissions (Europe)
▪ CE – EMC Directive 89/336/EEC (Europe)
▪ AS/NZS 3548 Emissions (Australia / New Zealand)

9.2.3   Certifications / Registrations / Declarations

▪ UL Certification (US/Canada)
▪ CB Certification (International)
▪ CE Declaration of Conformity (CENELEC Europe)
▪ FCC/ICES-003 Class A Attestation (USA/Canada)
▪ C-Tick Declaration of Conformity (Australia)
▪ MED Declaration of Conformity (New Zealand)

9.2.4   Product Regulatory Compliance Markings

This product is marked with the following Product Certification Markings:

Table 64. Product Certification Markings

Regulatory Compliance	Region	Marking
UL Mark	USA/Canada	 E139761
CE Mark	Europe	
Canada EMC Mark	Canada	CANADA ICES-003 CLASS A
C-Tick Mark	Australia	 **N232**
Country of Origin	Exporting Requirements	MADE IN xxxxx (provided by label not silkscreen)
Model Designation	Regulatory Identification	Board PB Number will be used for the Model number
PB Free Marking	Environmental Requirements	

9.3   Electromagnetic Compatibility Notices

9.3.1   Industry Canada (ICES-003)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Apparelis Numériques", NMB-003 édictee par le Ministre Canadian des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: Digital Apparatus, ICES-003 of the Canadian Department of Communications.

9.3.2   Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.3.3   Australia / New Zealand

This product has been tested and complies with AS/NZS 3548. The product has been marked with the C-Tick mark to illustrate compliance.

9.4   Restriction of Hazardous Substances (RoHS)

Intel has a system in place to restrict the use of banned substances in accordance with the European Directive 2002/95/EC. Compliance is based on declaration that materials banned in the RoHS Directive are either (1) below all applicable substance threshold limits or (2) an approved/pending RoHS exemption applies.

Note: RoHS implementing details are not fully defined and may change.

Threshold limits and banned substances are noted below.

- Quantity limit of 0.1% by mass (1000 PPM) for:
    - Lead
    - Mercury
    - Hexavalent Chromium
    - Polybrominated Biphenyls Dipheny Ethers (PBDE)
- Quantity limit of 0.01% by mass (100 PPM) for:
    - Cadmium

9.5   Calculated Mean Time Between Failures (MTBF)

The MTBF (Mean Time Between Failures) for the Intel® Entry Server Board SE7230CA1-E as configured from the factory is shown in the table below.

Table 65. MTBF Data

Product Code	Operating Temperature
Intel® Entry Server Board SE7230CA1-E	40 degrees C

9.6   Mechanical Specifications

The following figure shows a mechanical drawing of the Intel® Entry Server Board SE7230CA1-E.
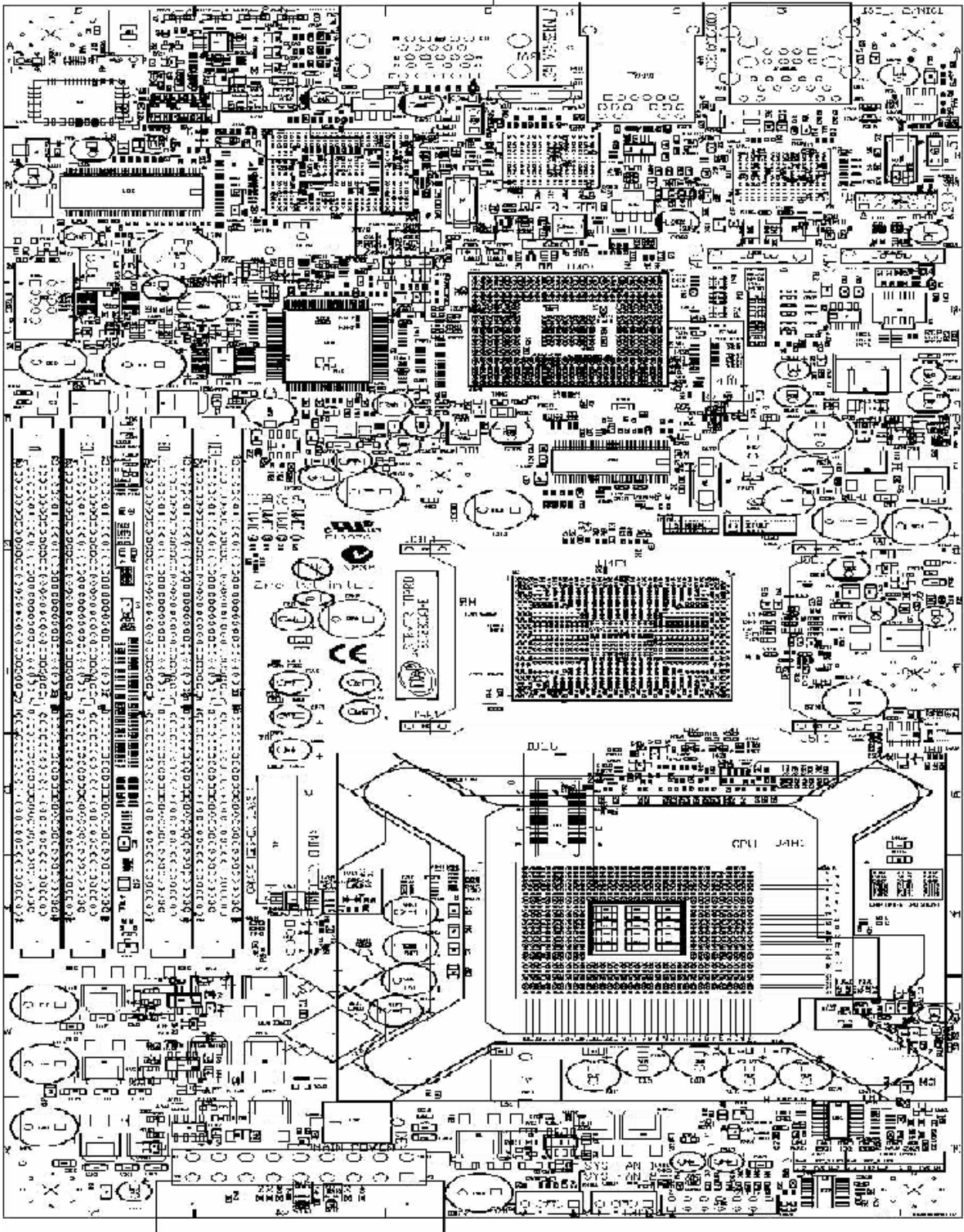
Figure 8. Intel® Entry Server Board SE7230CA1-E Mechanical Drawing

10. Hardware Monitoring

10.1   Monitored Components

The Intel® Entry Server Board SE7230CA1-E has an integrated Heceta chip that is responsible for hardware monitoring. The Heceta chip provides basic server hardware monitoring which alerts a system administrator if a hardware problem occurs on the board. The SMsC* LP47M182NR has implemented some fan speed control/monitor pins. Below is a table of monitored headers and sensors on the board.

Table 66. Monitored Components

| Item		Description	
Voltage	VCCP (PIN #23)	Monitors processor voltage	Heceta*
	P12V (PIN #21)	Monitors +12Vin for system +12V supply	Heceta*
	2.5V (PIN #22)	Monitors 1.5V Core power	Heceta*
	P5V (PIN #20)	Monitors +5V	Heceta*
Fan Speed	PWM1 (PIN #24)	N/A	Heceta*
	PWM2 (PIN #10)	Controls system fan 1 (J3K2)	Heceta*
	PWM3 (PIN #13)	Controls system fan 2 (J4K1)	Heceta*
	TACH1 (PIN #11)	N/A	Heceta*
	TACH2 (PIN #12)	Monitors system fan 1 (J3K2)	Heceta*
	TACH3 (PIN #9)	Monitors system fan 2 (J4K1)	Heceta*
Temperature	H_THEMP_DA/C	Monitors processor temperature	Heceta*

10.1.1   Fan Speed Control
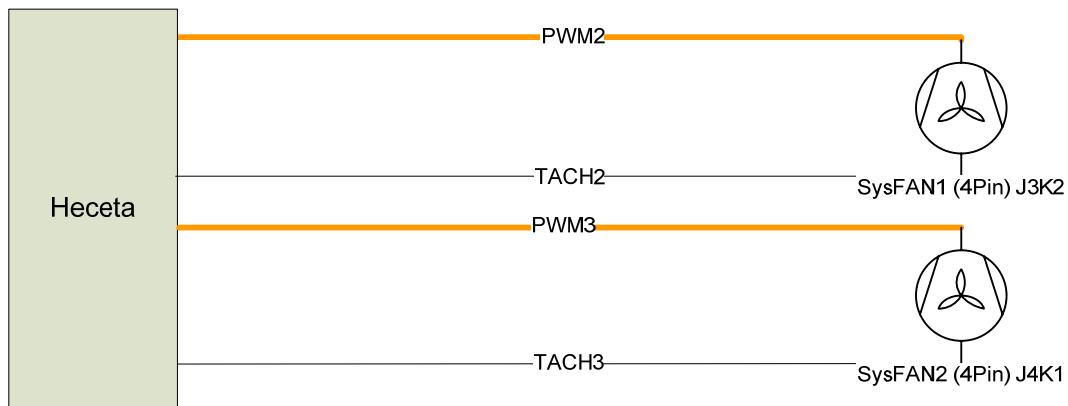
Figure 9. Fan Speed Control Block Diagram

10.2   Chassis Intrusion

The Intel® Entry Server Board SE7230CA1-E supports a chassis security feature that detects if the chassis cover is removed. This security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the open position.

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., "82460GX") with alpha entries following (e.g., "AGP 4x"). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
AP	Application Processor
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BGA	Ball-grid Array
BIOS	Basic input/output system
Byte	8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DCD	Data Carrier Detect
DMA	Direct Memory Access
DMTF	Distributed management Task Force
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
Hz	Hertz (1 cycle/second)
HDG	Hardware Design Guide
I_2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IMB	Inter Module Bus
IP	Internet Protocol
IRQ	Interrupt Request
ITP	In-target probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local area network
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count

Term	Definition
LSB	Least Significant Bit
MB	1024 KB
MBE	Multi-Bit Error
Ms	milliseconds
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
Mux	multiplexor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance
PBGA	Pin Ball Grid Array
PERR	Parity Error
PIO	Programmable I/O
PMB	Private Management Bus
PMC	Platform Management Controller
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAIDIOS	RAID I/O Steering
RAM	Random Access Memory
RI	Ring Indicate
RISC	Reduced instruction set computing
RMCP	Remote Management Control Protocol
ROM	Read Only Memory
RTC	Real Time Clock
SBE	Single-Bit Error
SCI	System Configuration Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System event log
SERIRQ	Serialized Interrupt Requests
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter

Term	Definition
USB	Universal Serial Bus
VGA	Video Graphic Adapter
VID	Voltage Identification
VRM	Voltage Regulator Module
Word	16-bit quantity
ZCR	Zero Channel RAID

References

- *Advanced Configuration and Power Interface Specification*, Revision 1.0b, February 1999, http://www.acpi.info/

- *Advanced Configuration and Power Interface Specification*, Revision 2.0, July 2000, http://www.acpi.info/

- *Advanced Configuration and Power Interface Specification*, Revision 3.0, , http://www.acpi.info/

- *BIOS Boot Specification Version 1.01.* Compaq Computer Corporation, Phoenix Technologie Ltd., Intel Corporation. 1996, http://www.phoenix.com/resources/specs-bbs101.pdf

- *El Torito CD-ROM Boot Specification*, Version 1.0, http://www.phoenix.com/resources/specs-cdrom.pdf

- *Extensible Firmware Interface Reference Specification*, Version 1.1, http://www.intel.com/technology/efi/index.htm

- *Tiano EFI Shell EPS*, Revision 0.10. Intel Corporation, 2002

- *EFI 1.1 Shell Commands Specification*, v0.3, Available from: EFI1.1ShellCommands.pdf, EFI sample implementation, revision 1.10.14.62, http://developer.intel.com/technology/efi/main_sample.htm

- *IA-32e BIOS Writer's Guide*, Revision 0.5, Intel Corporation

- *Platform Management FRU Information Storage Definition* v1.0, http://developer.intel.com/design/servers/ipmi

- *Hardware Design Guide for Microsoft Windows 2000 Server*, Version 3.0, http://www.microsoft.com/whdc/system/platform/pcdesign/desguide/serverdg.mspx#ESB

- *Application Note AP-485: Intel Processor Identification and the CPUID Function*, http://www.intel.com/design/xeon/applnots/241618.htm

- *Intelligent Platform Management Bus Specification*, Version 1.0, http://developer.intel.com/design/servers/ipmi/spec.htm

- *Intelligent Platform Management Interface Specification*, Version 1.5, http://developer.intel.com/design/servers/ipmi/spec.htm

- *Intelligent Platform Management Interface Specification*, Version 2.0, http://developer.intel.com/design/servers/ipmi/spec.htm

- *Multiprocessor Specification*, Revision 1.4, May 1997

- *Microsoft Headless Design Guidelines*, http://www.microsoft.com/HWDEV/PLATFORM/server/headless/default.asp

- *PCI Local Bus Specification, Revision 3.0, http://www.pcisig.org/*

- *PCI Local Bus Specification*, Revision 2.2, http://www.pcisig.org/

- *PCI BIOS Specification*, Revision 2.1, http://www.pcisig.org/

- *PCI to PCI Bridge Specification*, Revision 1.1, http://www.pcisig.org/

- *PCI Express Base Specification*, Revision 1.0a, http://www.pcisig.org/

- *PCI Hot-Plug Specification*, Revision 1.1, http://www.pcisig.org/

- *PCI IRQ Routing Table Specification*, Revision 1.0, Microsoft Corporation

- *Plug and Play BIOS Specification*, Revision 1.0a (relevant portions only), http://www.microsoft.com/whdc/system/pnppwr/pnp/default.mspx

- *Sahalee Baseboard Management Controller Core External Product Specification for Silverwood Systems*, Intel Corporation

- *System Management BIOS Reference* Specification, Version 2.4, http://www.dmtf.org/standards/smbios

- *ACPI Static Resource Affinity Table,* Version 1.2, http://www.microsoft.com/whdc/hwdev/platform/proc/SRAT.mspx

- *SYSID BIOS Support Interface Requirement Specification*, Version 1.2

- *Intel® Platform Innovation Framework for EFI Firmware Volume Specification*, Revision 0.9, Intel Corporation, 2004, ftp://download.intel.com/technology/framework/docs/Fv.pdf

- *Universal Host Controller Interface Design Guide*, http://developer.intel.com/design/USB/UHCI11D.htm

- *Universal Serial Bus Revision 1.1 Specification, http://www.usb.org/developers/docs*

- *Universal Serial Bus Revision 2.0 Specification, http://www.usb.org/developers/docs*

- *Wired For Management Baseline Specification*, Revision 2.0, http://www.intel.com/labs/manage/wfm/wfmspecs.htm

- *DMTF Systems Standard Groups Definition*