Ordering number : ENA0179

SANYO Semiconductors
DATA SHEET

LC750512E — CMOS IC
Audistry support Audio DSP

Overview

The LC750512E is a single-chip audio DSP equipped with an Audio interface unit with features such as audio algorithm and lip-sync functions, which are required by audio/video-related products for which higher and higher sound quality levels are being demanded. The microcontroller has a CCB (Computer Control Bus) and I^2C (Inter-Integrated Circuit) –support interface.

Features

1. Hardware configuration that allows installation of audio algorithm functions related to audio/video products
   - Program ROM: 24 bits×8K words
   - Data RAM: 24 bits×4K words×2 planes, 24 bits×1K words×2 planes
   - Audio interface: I^2S input, MSB first right justified, MSB first left justified (1 port)
   - Audio interface: I^2S output, MSB first right justified, MSB first left justified (3 ports)
   - Analog input: 1 port (2 channel stereo), Analog output: 1 port (2 channel stereo)

2. Audio algorithms for audio/video-related products installed
   - Lip sync function (correcting time lags up to 80ms between audio and video at a 48kHz sampling frequency)
   - Audistry function (Mono-to-Stereo Creator, Suound Space Expander, Sound Space for Headphones, Intelligent Volume Control, Natural bass)
   - Equalizer function (3 bands/channel, common to L and R channels)
   - Volume control function (0 to -79dB, in 1dB increments, -∞)
   - Bass/treble control (±18 dB in 1dB increments) and other basic control functions
   - Audistry mode/S3S mode user selectable, enabling SANYO's proprietary surround mode

Audistry mode

Effect	Algorithm (Name)	Remarks
Audistry	Mono-to-Stereo Creator	Generates a pseudo stereo sound from a mono signal
	Sound Space Expander	Creates pseudo sound field (speaker)
	Sound Space for Headphones	Creates pseudo sound field (headphone)
	Intelligent Volume Control	AGC processing
	Natural Bass	Low frequency enhancement

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

S3S mode

Effect	Algorithm (Name)	Remarks
Low frequency enhancement	S-Live	SANYO's proprietary low frequency enhancement algorithm
Surround	Digital AViSS	SANYO's proprietary sound field control algorithm

The audio processing functions listed in the table below can be installed by making changes to the program ROM. (These functions have not been installed in the LC750512E).

Effect	Algorithm (Name)	Remarks
Surround	Dolby Prologic II	Registered trademark of Dolby Laboratories, Inc.
Low frequency enhancement	TruBass	Registered trademark of SRS Labs, Inc.
Sound field correction	Focus	Registered trademark of SRS Labs, Inc.
Virtual surround	SRS 3D,TruSurround	Registered trademark of SRS Labs, Inc.
Low- and high-frequency enhancement	Dedekind	Registered trademark of Dedekind R&D
Low- and high-frequency augumentation	BBE	Registered trademark of BBE Sound Inc.

Note 1: Users must be licensees of the algorithms listed. Model names are subject to change.

Note 2: Processing estimates for using the algorithms will be based on the combinations in which the desired functions are used.

3. Microcontroller interface
   - CCB and I^2C support

4. Supply voltages
   - Analog: 3.3V, 5V
   - Digital: 1.8V, 3.3V

Specifications

Absolute Maximum Ratings at V_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (A/D, D/A, volume, etc.)	V_{DD} max1	$AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$	-0.3		+6.0	V
Supply voltage (A/D, D/A, volume, etc.)	V_{DD} max1	$BV_{DD}1$	-0.3		+3.96	V
Supply voltage (crystal oscillator)	V_{DD} max2	XV_{DD}	-0.3		+3.96	V
Supply voltage (I/O interface block)	V_{DD} max3	$CV_{DD}1$, $CV_{DD}2$, $CV_{DD}3$, $CV_{DD}4$	-0.3		+3.96	V
Supply voltage (DSP core block, PLL block)	V_{DD} max4	$DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$, $DV_{DD}4$ $PLLDV_{DD}$, $PLLAV_{DD}$, PLLPWRR	-0.3		+2.16	V
Maximum input voltage (A/D, D/A, volume, etc.)	$V_{IN}1$	INL, INR EVRINL, EVRINR	-0.3		AV_{DD}+0.3 (max+6.0V)	V
Maximum input voltage (DSP core block) (I/O interface block)	$V_{IN}2$	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	-0.3		CV_{DD}+0.3 (max+3.96V)	V
Maximum output voltage	V_{OUT}	CV_{DD}	-0.3		CV_{DD}+0.3	V
Allowable power dissipation	Pd max	Conditions: audio disabled operating state, mounted on a standard board*			850	mW
Maximum output current	I_O	SDA/DO	0		4	mA
Operating temperature	Topr		-20		+75	°C
Storage temperature	Tstg		-55		+125	°C

*****: Standard board: 76.1mm×114.3mm×1.6mm; glass epoxy resin

Allowable Operating Ranges at Ta = -20 to +75°C, V_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (analog block)	AV_{DD}	$AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$	+4.75		+5.25	V
Supply voltage (analog block)	BV_{DD}	$BV_{DD}1$	+3.0		+3.6	V
Supply voltage (crystal oscillator)	XV_{DD}	XV_{DD}	+3.0		+3.6	V
Supply voltage (digital block)	CV_{DD}	$CV_{DD}1$, $CV_{DD}2$, $DV_{DD}3$, $DV_{DD}4$	+3.0		+3.6	V
Supply voltage (digital block, PLL)	DV_{DD}	$DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$, $DV_{DD}4$ $PLLDV_{DD}$, $PLLAV_{DD}$, PLLPWRR	+1.62		+1.98	V
High-level input voltage	V_{IH}_D	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	0.8×CV_{DD}		CV_{DD}	V
Low-level input voltage	V_{IL}_D	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	V_{SS}		0.2×CV_{DD}	V
Crystal oscillator frequency	Fop	XIN, XOUT		18.432		MHz

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin name	Conditions	Ratings			unit
				min	typ	max	
High-level input current	I_{IH}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	$V_{IN}2$=$V_{IN}3$=CV_{DD}			5	μA
Low-level input current	I_{IL}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	$V_{IN}2$=$V_{IN}3$=0V	-5			μA
High-level output voltage	V_{OH}(1)	TEST6, TEST7, LRCKO, BCKO, DATAO0, DATAO1, DATAO2, I^2CBUSY/DI, EMPF, GPFLAG, MRREQ, XSEL0, XSEL1, XSEL2	I_{OH}=-2mA	CV_{DD}-0.4			V
	V_{OH}(2)	SCKO, SDA/DO	I_{OH}=-4mA	CV_{DD}-0.4			

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Parameter	Symbol	Pin name	Conditions	Ratings			unit
				min	typ	max	
Low-level output voltage	V_{OL}(1)	TEST6, TEST7, LRCKO, BCKO, DATAO0, DATAO1, DATAO2, I^2CBUSY/DI, SDA/DO EMPF, GPFLAG, MRREQ, XSEL0, XSEL1, XSEL2	I_{OH}=2mA			0.4	V
	V_{OH}(2)	SCKO, SDA/DO	I_{OH}=4mA			0.4	
Output off leakage current	IOFF(1)	XSEL0, XSEL1, XSEL2, TEST6, I^2CBUSY/DI, SCKO, SDA/DO	V_{OUT}=CV_{DD}			5	µA
	IOFF(2)	XSEL0, XSEL1, XSEL2, TEST6, I^2CBUSY/DI, SCKO, SDA/DO	V_{OUT}=0V	-5			
Full scale input level	V_{IN}	INL, INR				0.4×AV_{DD} (max2Vp-p)	Vp-p
Analog output level	V_{OUT}	AOUT1, AOUT2				0.6×AV_{DD} (max3Vp-p)	Vp-p
Reference voltage output	Vref	VREF1, VREF2		2.35	2.5	2.65	V
Current drain	I_XV_{DD}	XV_{DD}	Conditions: audio disabled operating state, mounted on a standard board* XV_{DD}=3.3V		1.2	1.6	mA
	I_AV_{DD}	AV_{DD}1, AV_{DD}2, AV_{DD}3	Conditions: audio disabled operating state, mounted on a standard board* AV_{DD}=5V,		50	65	
	I_BV_{DD}	BV_{DD}1	Conditions: audio disabled operating state, mounted on a standard board* BV_{DD}=3.3V		2	3.5	
	I_CV_{DD}	CV_{DD}1, CV_{DD}2, CV_{DD}3, CV_{DD}4	Conditions: audio disabled operating state, mounted on a standard board* CV_{DD}=3.3V		1.8	2.4	
	I_DV_{DD}	DV_{DD}1, DV_{DD}2, DV_{DD}3, DV_{DD}4 PLLDV_{DD}, PLLAV_{DD}, PLLPWRR	Conditions: audio disabled operating state, mounted on a standard board* DV_{DD}=1.8V		65	85	

*****: Standard board: 76.1mm×114.3mm×1.6mm; glass epoxy resin

Analog Characteristics

Conditions: AV_{DD} = 5V, BV_{DD} = CV_{DD} = 3.3V, DV_{DD} = 1.8V, fs = 48kHz, audio signal frequency = 1kHz
Frequency bandwidth measured from A/D input to volume output: 10Hz to 20kHz, with a SANYO DSP evaluation board used
Test circuit configured with circuits externally attached to LC750512E; tested with signals passed straight through the DSP at room temperature using an audio analyzer (System 2) as the test device

Parameter	Ratings			unit	Conditions
	min	typ	max		
S/N	80	90		dB	A-weighted, input conditions: 2Vp-p
Dynamic range	80	90		dB	A-weighted
THD+N		-75	-70	dB	Input conditions: 1.5Vp-p, See Note.

Note: THD+N denotes the characteristics at which the input (1.5Vp-p) reduced by 3dB from the full-scale input is optimum.

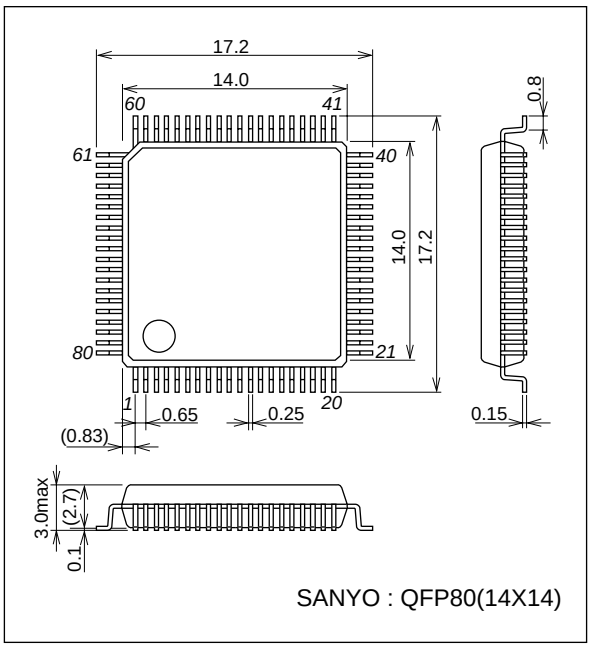
Conditions: AV_{DD} = 5V, BV_{DD} = CV_{DD} = 3.3V, DV_{DD} = 1.8V, fs = 48kHz, audio signal frequency = 1kHz
Frequency bandwidth measured from digital input to volume output: 10Hz to 20kHz, SANYO DSP evaluation board used
Test circuit configured with circuits externally attached to LC750512E; tested with signals passed straight through the DSP at room temperature using an audio analyzer (System2) as the test device

Parameter	Ratings			unit	Conditions
	min	typ	max		
S/N	83	93		dB	A-weighted, input conditions: 0dBFS
Dynamic range	83	93		dB	A-weighted
THD+N		-75	-70	dB	Input conditions: -3dBFS, See Note.

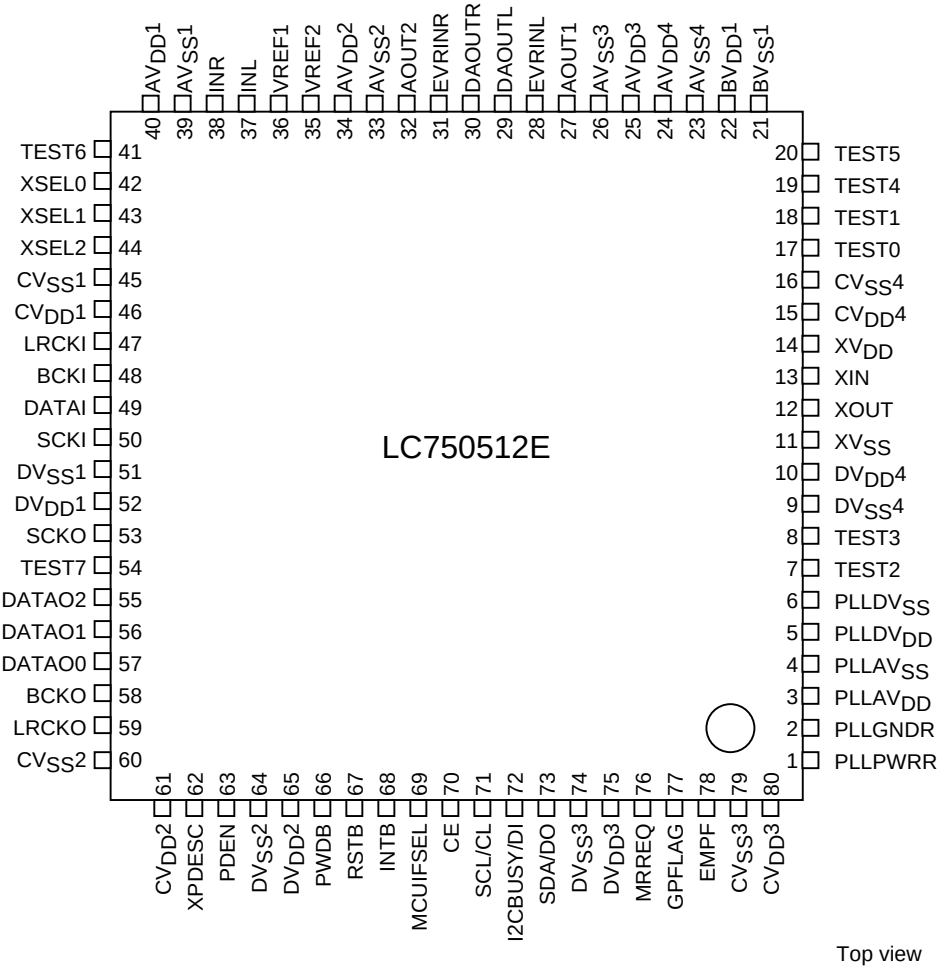
Note: THD+N denotes the characteristics at which the input reduced by 3dB from the full-scale input is optimum.

Package Dimensions

unit : mm
3255



Pin Assignment



Top view

Pin Functions

Pin Name	Input/Output	Function	Pin No.
INL	AI	Lch ADC analog input	37
INR	AI	Rch ADC analog input	38
DAOUTL	AO	Lch DAC analog output	29
DAOUTR	AO	Rch DAC analog output	30
EVRINL	AI	Lch EVR input	28
EVRINR	AI	Rch EVR input	31
AOUT1	AO	Lch EVR output	27
AOUT2	AO	Rch EVR output	32
LRCKI	I	LR clock input	47
BCKI	I	Bit clock input	48
DATAI	I	Data input	49
LRCKO	O	LR clock output	59
BCKO	O	Bit clock output	58
DATAO0	O	Data output 0	57
DATAO1	O	Data output 1	56
DATAO2	O	Data output 2	55
SCKI	I	External clock input	50
SCKO	I/O	DAC master clock output	53
RSTB	I	Reset input (low active)	67
PWDB	I	Power down input (low active)	66

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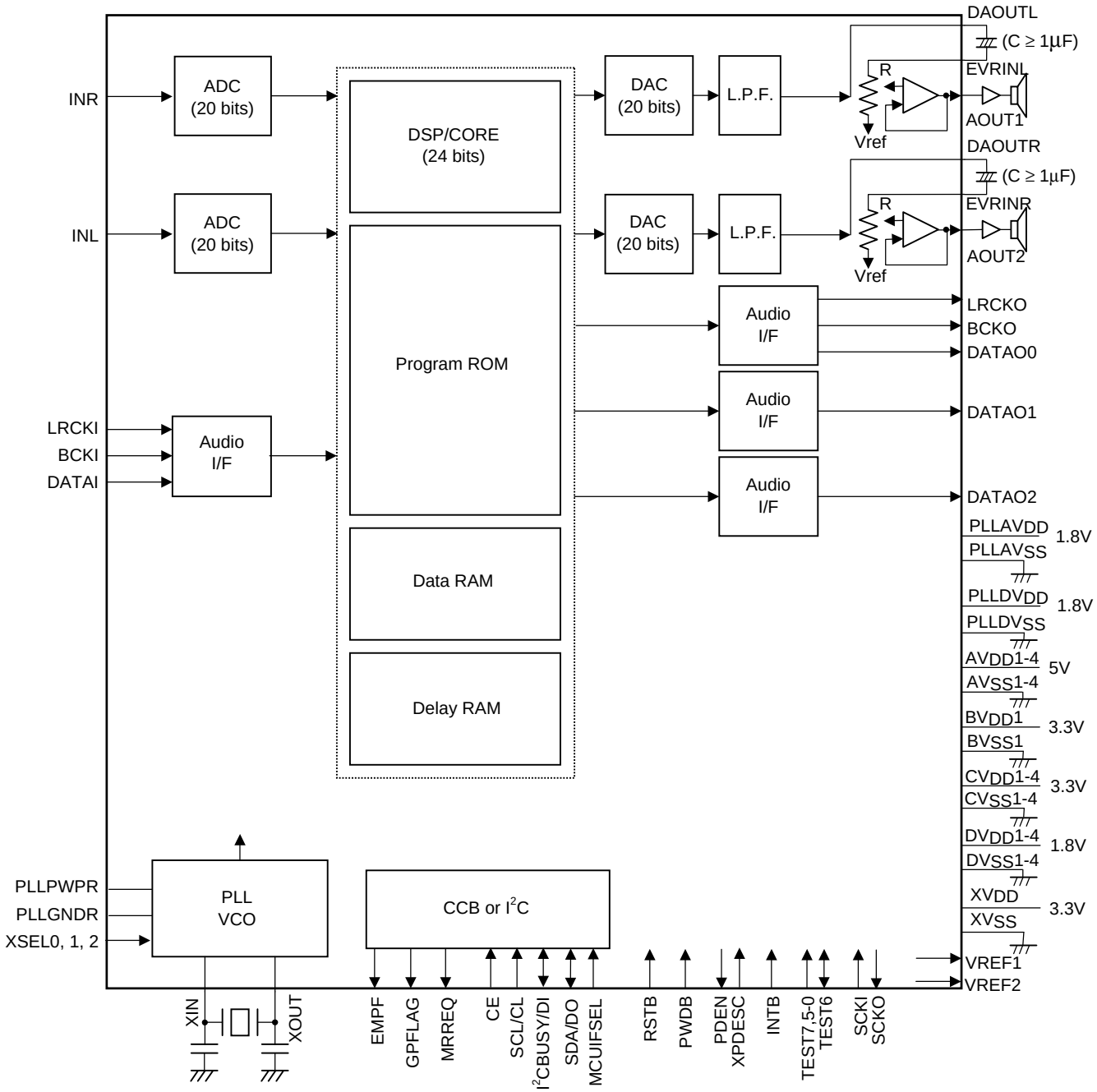
Pin Name	Input/Output	Function	Pin No.
INTB	I	Interrupt input (low active)	68
MCUIFSEL	I	Microcontroller interface select input (CCB: low, I^2C: high)	69
CE	I	Microcontroller interface chip enable, fixed at high when I^2C is selected.	70
SCL/CL	I	Microcontroller interface clock input	71
I^2CBUSY/DI	I/O	Microcontroller interface data input/I^2C BUSY output	72
SDA/DO	I/O	Microcontroller interface data input/output	73
EMPF	O	CCB input register status monitor flag	78
GPFLAG	O	DSP-to-MCU general-purpose flag (high active)	77
MRREQ	O	DSP-to-MCU communication error flag	76
XPDESC	I	DSP power down reset signal (low active)	62
PDEN	O	DSP power down signal (high active)	63
XSEL0	I/O	Crystal frequency select signal 0	42
XSEL1	I/O	Crystal frequency select signal 1	43
XSEL2	I/O	Crystal frequency select signal 2	44
TEST7	I	Test pin	54
TEST0, TEST1, TEST2, TEST3, TEST4, TEST5	I	Test pin	17, 18, 7, 8, 19, 20
TEST6	I/O	Test pin	41
XIN		Crystal oscillator input	13
XOUT		Crystal oscillator output	12
XV_{DD}		Power supply for crystal oscillator	14
XV_{SS}		GND for crystal oscillator	11
VREF1	AO	Reference voltage output pin 1 (ADC)	36
VREF2	AO	Reference voltage output pin 2 (DAC, EVR)	35
$AV_{DD}1$		ADC analog power supply (+5V)	40
$AV_{SS}1$		ADC analog GND	39
$AV_{DD}2$		VREF V_{DD} (+5V)	34
$AV_{SS}2$		VREF GND	33
$AV_{DD}3$		EVR analog V_{DD} (+5V)	25
$AV_{SS}3$		EVR analog GND	26
$AV_{DD}4$		DAC analog V_{DD} (+5V)	24
$AV_{SS}4$		DAC analog GND	23
$BV_{DD}1$		Analog chip logic power supply (+3.3V)	22
$BV_{SS}1$		Analog chip logic GND	21
$CV_{DD}1$, $CV_{DD}2$, $CV_{DD}3$, $CV_{DD}4$		Digital power supply (3.3V)	46, 61, 80, 15
$CV_{SS}1$, $CV_{SS}2$, $CV_{SS}3$, $CV_{SS}4$		Digital GND	45, 60, 79, 16
$DV_{DD}1$, $DV_{DD}2$, $DV_{DD}3$, $DV_{DD}4$		Digital power supply (1.8V)	52, 65, 75, 10
$DV_{SS}1$, $DV_{SS}2$, $DV_{SS}3$, $DV_{SS}4$		Digital GND	51, 64, 74, 9
PLLPWRR		Powering for PLL (ESD) (1.8V)	1
PLLGNDR		GND for PLL (ESD)	2
$PLLAV_{DD}$		Power supply for PLL (1.8V)	3
$PLLAV_{SS}$		GND for PLL	4
$PLLDV_{DD}$		Digital power supply for PLL (1.8V)	5
$PLLDV_{SS}$		Digital GND for PLL	6

Block Diagram



For sample external circuit configurations, see "LC750512E External Circuit Configuration Examples (Draft)."