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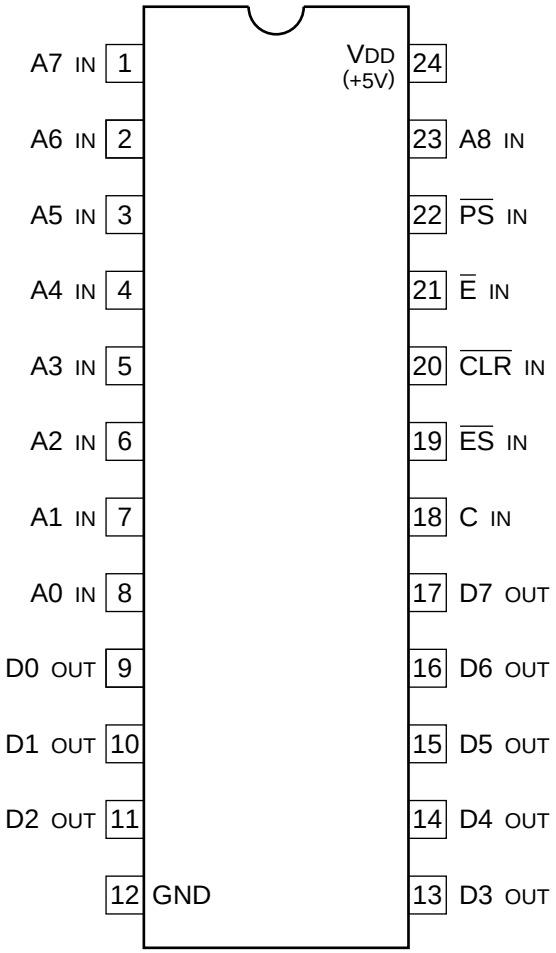
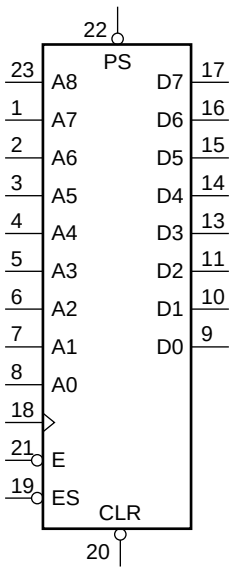
IL00

C-MOS 4 K (512 × 8)-BIT PROM WITH REGISTER

-TOP VIEW-



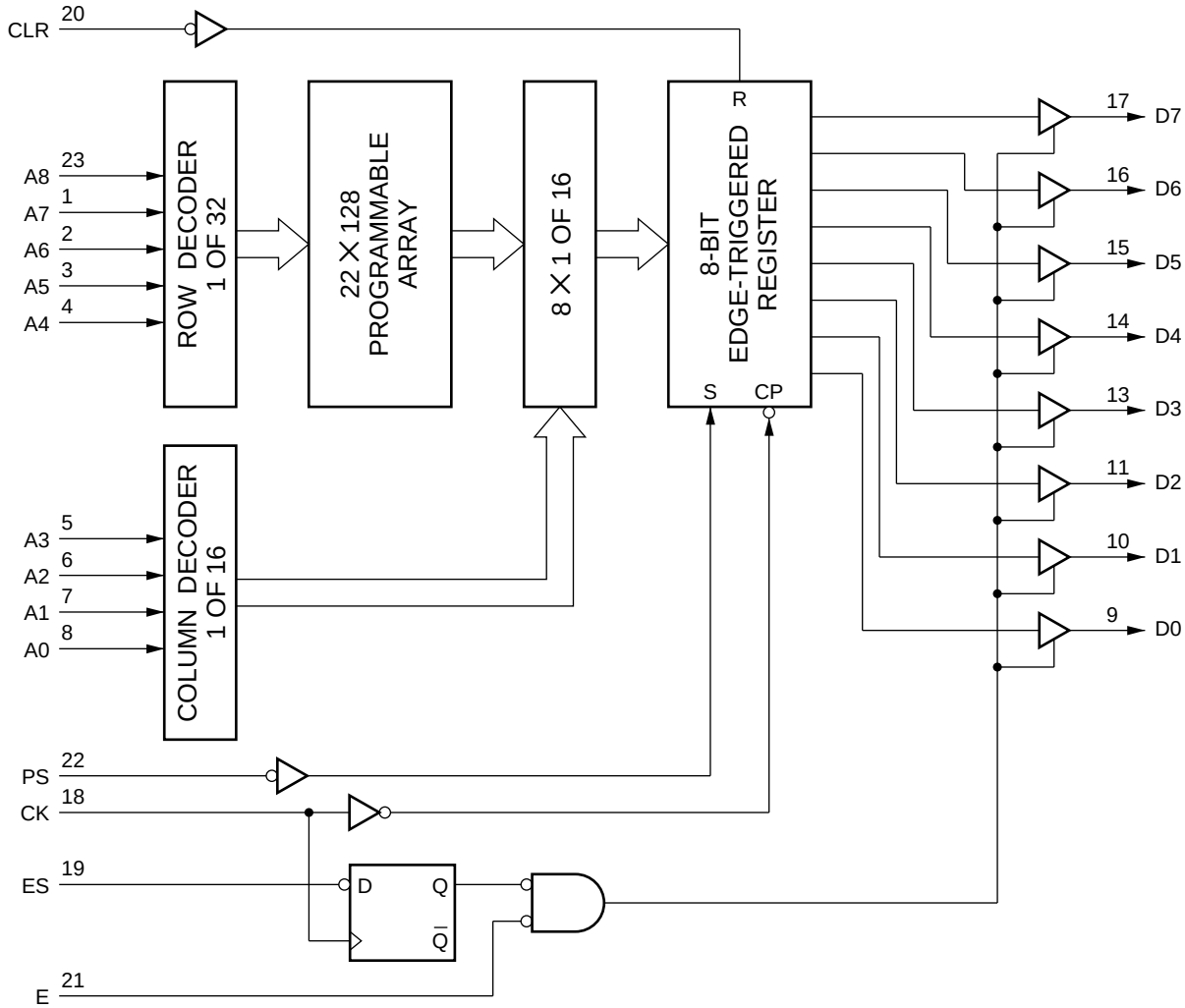


A0 - A14 ; ADDRESS INPUTS
CLR ; CLEAR INPUT
CK ; CLOCK INPUT
D0 - D7 ; DATA OUTPUTS
E ; ASYNCHRONOUS ENABLE INPUT
ES ; SYNCHRONOUS ENABLE INPUT
PS ; PRESET INPUT

MODE SELECTION

CK	ES	CLR	E	PS	OUTPUTS	MODE
×	0	1	0	1	DATA OUT	READ
×	1	1	×	1	HI-Z	OUTPUT DISABLE
×	×	1	1	1	HI-Z	OUTPUT DISABLE
×	0	0	0	1	ZEROS	CLEAR
×	0	1	0	0	ONES	PRESET
0	1	VPP	1	1	DATA IN	PROGRAM
1	0	VPP	1	1	DATA OUT	PROGRAM VERIFY
1	1	VPP	1	1	HI-Z	PROGRAM INHIBIT
0	1	VPP	1	1	DATA IN	INTELLIGENT PROGRAM
VPP	0	0	0	1	DATA OUT	BLANK CHECK ONES
VPP	1	0	0	1	HI-Z	BLANK CHECK ZEROS

0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CARE (NOT TO EXCEED VPP)
HI-Z ; HIGH IMPEDANCE
VPP ; PROGRAM VOLTAGE (+13V TO +14V)


CLR
20
A8
23
A7
1
A6
2
A5
3
A4
4
ROW DECODER
1 OF 32
22 X 128
PROGRAMMABLE
ARRAY
8 X 1 OF 16
R
8-BIT
EDGE-TRIGGERED
REGISTER
S
CP
17
D7
16
D6
15
D5
14
D4
13
D3
11
D2
10
D1
9
D0
A3
5
A2
6
A1
7
A0
8
COLUMN DECODER
1 OF 16
PS
22
CK
18
ES
19
D
Q
Q
21
E