



SANYO Semiconductors

DATA SHEET

LC75051E — CMOS IC Lip-Sync Enabling Audio DSP

Overview

The LC75051E is a single-chip audio DSP equipped with an Audio interface unit with features such as audio algorithm and lip-sync functions, which are required by audio/video-related products for which higher and higher sound quality levels are being demanded. The microcontroller has a CCB (Computer Control Bus) and I²C (Inter-Integrated Circuit) –support interface.

Features

1. Hardware configuration that allows installation of audio algorithm functions related to audio/video products
 - Program ROM: 24 bits×8K words
 - Data RAM: 24 bits×4K words×2 planes, 24 bits×1K words×2 planes
 - Audio interface: I²S input, MSB first right justified, MSB first left justified (1 port)
 - Audio interface: I²S output, MSB first right justified, MSB first left justified (3 ports)
 - Analog input: 1 port (2 channel stereo), Analog output: 1 port (2 channel stereo)
2. Audio algorithms for audio/video-related products installed
 - Lip sync function (correcting time lags up to 80ms between audio and video at a 48kHz sampling frequency)
 - Low frequency enhancement function (S-Live: SANYO Low frequency Intelligence Virtual Excitation)
 - Surround function (Digital AViSS: Digital Acoustic Virtual Sound System)
 - Equalizer function (3 bands/channel, common to L and R channels)
 - Volume control function (0 to –79dB, in 1dB increments, –∞)
 - Bass/treble/middle control (±18dB in 1dB increments) and other basic control functions
 - Wide variety of audio processing functions

Audio processing functions already installed in LC75051E

Effect	Algorithm (Name)	Remarks
Low frequency enhancement	S-Live	SANYO's proprietary low frequency enhancement algorithm
Surround	Digital AViSS	SANYO's proprietary sound field control algorithm

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC75051E

The audio processing functions listed in the table below can be installed by making changes to the program ROM. (These functions have not been installed in the LC75051E).

Effect	Algorithm (Name)	Remarks
Surround	AViSS	SANYO's proprietary sound field control algorithm
Virtual surround	VASIL	SANYO's proprietary sound field control algorithm
Surround	Dolby Prologic II	Registered trademark of Dolby Laboratories, Inc.
Low frequency enhancement	TruBass	Registered trademark of SRS Labs, Inc.
Sound field correction	Focus	Registered trademark of SRS Labs, Inc.
Virtual surround	SRS 3D,TruSurround	Registered trademark of SRS Labs, Inc.
Low- and high-frequency enhancement	Dedekind	Registered trademark of Dedekind R&D
Low- and high-frequency augmentation	BBE	Registered trademark of BBE Sound Inc.

Note 1: Users must be licensees of the algorithms listed. Model names are subject to change.

Note 2: Processing estimates for using the algorithms will be based on the combinations in which the desired functions are used.

3. Microcontroller interface

- CCB and I²C support

4. Supply voltages

- Analog: 3.3V, 5V
- Digital: 1.8V, 3.3V

Specifications

Absolute Maximum Ratings at V_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (A/D,D/A,volume,etc)	V _{DD max1}	AV _{DD1} , AV _{DD2} , AV _{DD3}	-0.3		+6.0	V
Supply voltage (A/D,D/A,volume,etc)	V _{DD max1}	BV _{DD1}	-0.3		+3.96	V
Supply voltage (crystal oscillator)	V _{DD max2}	XV _{DD}	-0.3		+3.96	V
Supply voltage (I/O interface block)	V _{DD max3}	CV _{DD1} , CV _{DD2} , CV _{DD3} , CV _{DD4}	-0.3		+3.96	V
Supply voltage (DSP core block, PLL block)	V _{DD max4}	DV _{DD1} , DV _{DD2} , DV _{DD3} , DV _{DD4} PLLDV _{DD} , PLLAV _{DD} , PLLPWRR	-0.3		+2.16	V
Maximum input voltage (A/D,D/A,volume,etc)	V _{IN1}	INL, INR EVRINL, EVRINR	-0.3		AV _{DD} +0.3 (max+6.0V)	V
Maximum input voltage (DSP core block) (I/O interface block)	V _{IN2}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I ² CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	-0.3		CV _{DD} +0.3 (max+3.96V)	V
Maximum output voltage	V _{OUT}	CV _{DD}	-0.3		CV _{DD} +0.3	V
Allowable power dissipation	P _{d max}	Conditions: audio disabled operating state, mounted on a standard board*			850	mW
Maximum output current	I _O	SDA/DO	0		4	mA
Operating temperature	T _{opr}		-20		75	°C
Storage temperature	T _{stg}		-55		125	°C

*: Standard board: 76.1mm×114.3mm×1.6mm; glass epoxy resin

LC75051E

Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$, $AV_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (analog block)	AV_{DD}	AV_{DD1} , AV_{DD2} , AV_{DD3}	+4.75		+5.25	V
Supply voltage (analog block)	BV_{DD}	BV_{DD1}	+3.0		+3.6	V
Supply voltage (crystal oscillator)	XV_{DD}	XV_{DD}	+3.0		+3.6	V
Supply voltage (digital block)	CV_{DD}	CV_{DD1} , CV_{DD2} , DV_{DD3} , DV_{DD4}	+3.0		+3.6	V
Supply voltage (digital block, PLL)	DV_{DD}	DV_{DD1} , DV_{DD2} , DV_{DD3} , DV_{DD4} $PLLDV_{DD}$, $PLLAV_{DD}$, $PLLWRR$	+1.62		+1.98	V
High-level input voltage	V_{IH_D}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2 CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	0.8 $\times CV_{DD}$		CV_{DD}	V
Low-level input voltage	V_{IL_D}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2 CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	V_{SS}		0.2 $\times CV_{DD}$	V
Crystal oscillator frequency	Fop	XIN, XOUT		18.432		MHz

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin name	Conditions	Ratings			unit
				min	typ	max	
High-level input current	I_{IH}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2 CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	$V_{IN2}=V_{IN3}=CV_{DD}$			5	μA
Low-level input current	I_{IL}	TEST0, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 SCKI, LRCKI, BCKI, DATAI, CE, SCL/CL, I^2 CBUSY/DI, SDA/DO, MCUIFSEL, XPDESC, RSTB, PWDB, INTB, XSEL0, XSEL1, XSEL2	$V_{IN2}=V_{IN3}=0\text{V}$	-5			μA
High-level output voltage	$V_{OH(1)}$	TEST6, TEST7, LRCKO, BCKO, DATAO0, DATAO1, DATAO2, I^2 CBUSY/DI, EMPF, GPFLAG, MRREQ, XSEL0, XSEL1, XSEL2	$I_{OH}=-2\text{mA}$	$CV_{DD}-$ 0.4			V
	$V_{OH(2)}$	SCKO, SDA/DO	$I_{OH}=-4\text{mA}$	$CV_{DD}-$ 0.4			

Continued on next page.

LC75051E

Continued from preceding page.

Parameter	Symbol	Pin name	Conditions	Ratings			unit
				min	typ	max	
Low-level output voltage	V _{OL} (1)	TEST6, TEST7, LRCKO, BCKO, DATA00, DATA01, DATA02, I ² CBUSY/DI, SDA/DO EMPF, GPFLAG, MRREQ, XSEL0, XSEL1, XSEL2	I _{OH} =2mA			0.4	V
	V _{OH} (2)	SCKO, SDA/DO	I _{OH} =4mA			0.4	
Output off leakage current	I _{OFF} (1)	XSEL0, XSEL1, XSEL2, TEST6, I ² CBUSY/DI, SCKO, SDA/DO	V _{OUT} =CV _{DD}			5	μA
	I _{OFF} (2)	XSEL0, XSEL1, XSEL2, TEST6, I ² CBUSY/DI, SCKO, SDA/DO	V _{OUT} =0V	-5			
Full scale input level	V _{IN}	INL, INR				0.4×AV _{DD} (max2Vp-p)	Vp-p
Analog output level	V _{OUT}	AOUT1, AOUT2				0.6×AV _{DD} (max3Vp-p)	Vp-p
Reference voltage output	V _{ref}	VREF1, VREF2		2.35	2.5	2.65	V
Current drain	I _{XVDD}	XVDD	Conditions: audio disabled operating state, mounted on a standard board* XV _{DD} =3.3V		1.2	1.6	mA
	I _{AVDD}	AVDD1, AVDD2, AVDD3	Conditions: audio disabled operating state, mounted on a standard board* AV _{DD} =5V		50	65	
	I _{BVDD}	BVDD1	Conditions: audio disabled operating state, mounted on a standard board* BV _{DD} =3.3V		2	3.5	
	I _{CVDD}	CVDD1, CVDD2, CVDD3, CVDD4	Conditions: audio disabled operating state, mounted on a standard board* CV _{DD} =3.3V		1.8	2.4	
	I _{DVDD}	DVDD1, DVDD2, DVDD3, DVDD4 PLLDVDD, PLLAVDD, PLLPWRR	Conditions: audio disabled operating state, mounted on a standard board* DV _{DD} =1.8V		65	85	

*: Standard board: 76.1mm×114.3mm×1.6mm; glass epoxy resin

LC75051E

Analog Characteristics

Conditions: $AV_{DD} = 5V$, $BV_{DD} = CV_{DD} = 3.3V$, $DV_{DD} = 1.8V$, $f_s = 48kHz$, audio signal frequency = 1kHz
 Frequency bandwidth measured from A/D input to volume output: 10Hz to 20kHz, with a SANYO DSP evaluation board used

Test circuit configured with circuits externally attached to LC75051E; tested with signals passed straight through the DSP at room temperature using an audio analyzer (System 2) as the test device

Parameter	Ratings			unit	Conditions
	min	typ	max		
S/N	80	90		dB	A-weighted, input conditions: 2Vp-p
Dynamic range	80	90		dB	A-weighted
THD+N		-75	-70	dB	Input conditions: 1.5Vp-p, See Note.

Note: THD+N denotes the characteristics at which the input (1.5Vp-p) reduced by 3dB from the full-scale input is optimum.

Conditions: $AV_{DD} = 5V$, $BV_{DD} = CV_{DD} = 3.3V$, $DV_{DD} = 1.8V$, $f_s = 48kHz$, audio signal frequency = 1kHz
 Frequency bandwidth measured from digital input to volume output: 10Hz to 20kHz, SANYO DSP evaluation board used

Test circuit configured with circuits externally attached to LC75051E; tested with signals passed straight through the DSP at room temperature using an audio analyzer (System2) as the test device

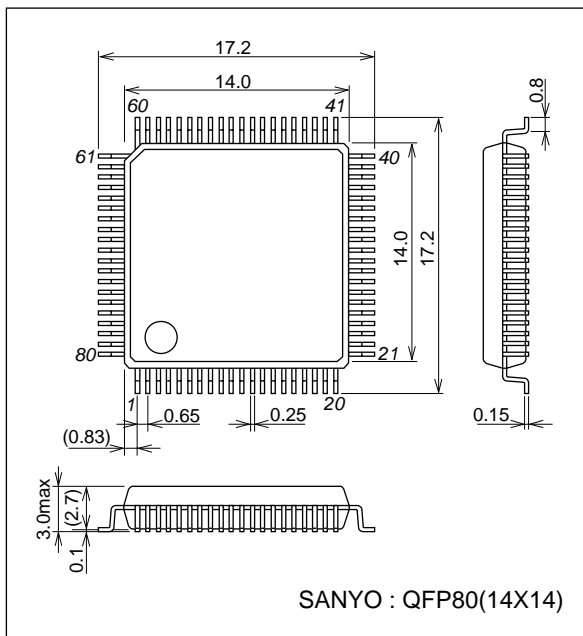
Parameter	Ratings			unit	Conditions
	min	typ	max		
S/N	83	93		dB	A-weighted, input conditions: 0dBFS
Dynamic range	83	93		dB	A-weighted
THD+N		-75	-70	dB	Input conditions: -3dBFS, See Note.

Note: THD+N denotes the characteristics at which the input reduced by 3dB from the full-scale input is optimum.

Package Dimensions

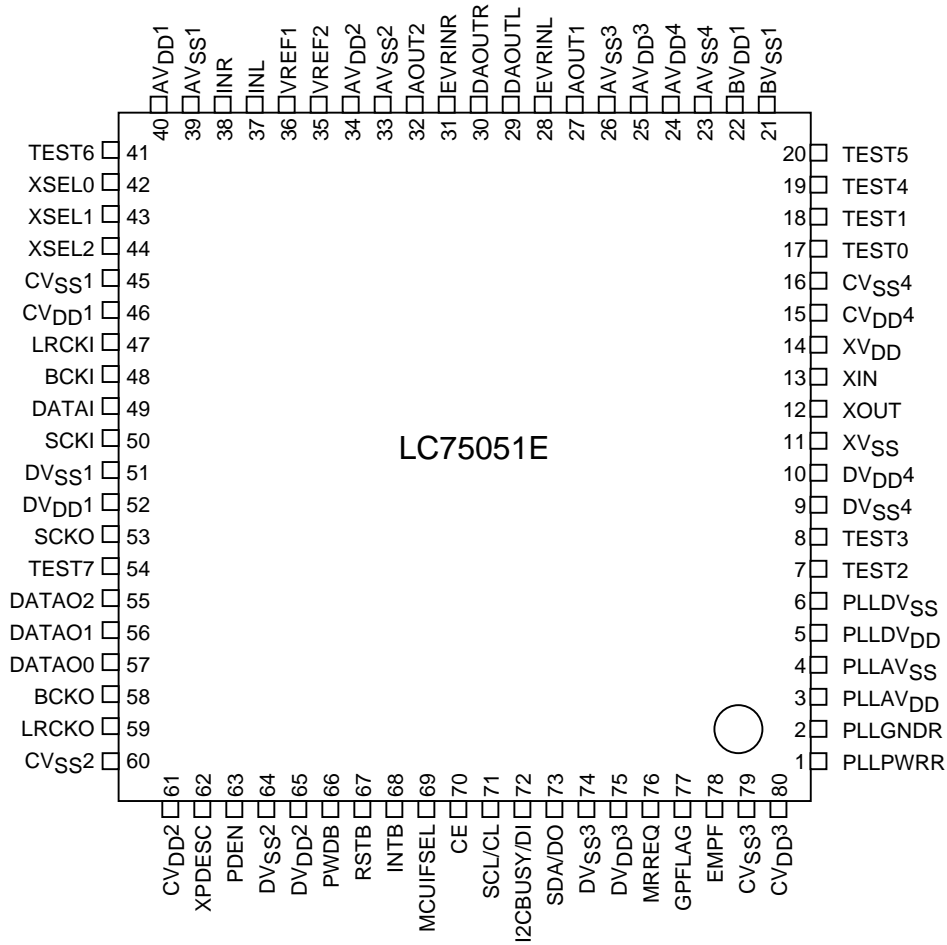
unit : mm

3255



LC75051E

Pin Assignment



Top view

Pin Functions

Pin Name	Input/Output	Function	Pin No.
INL	AI	Lch ADC analog input	37
INR	AI	Rch ADC analog input	38
DAOUTL	AO	Lch DAC analog output	29
DAOUTR	AO	Rch DAC analog output	30
EVRINL	AI	Lch EVR input	28
EVRINR	AI	Rch EVR input	31
AOUT1	AO	Lch EVR output	27
AOUT2	AO	Rch EVR output	32
LRCKI	I	LR clock input	47
BCKI	I	Bit clock input	48
DATAI	I	Data input	49
LRCKO	O	LR clock output	59
BCKO	O	Bit clock output	58
DATAO0	O	Data output 0	57
DATAO1	O	Data output 1	56
DATAO2	O	Data output 2	55
SCKI	I	External clock input	50
SCKO	I/O	DAC master clock output	53
RSTB	I	Reset input (low active)	67
PWDB	I	Power down input (low active)	66

Continued on next page.

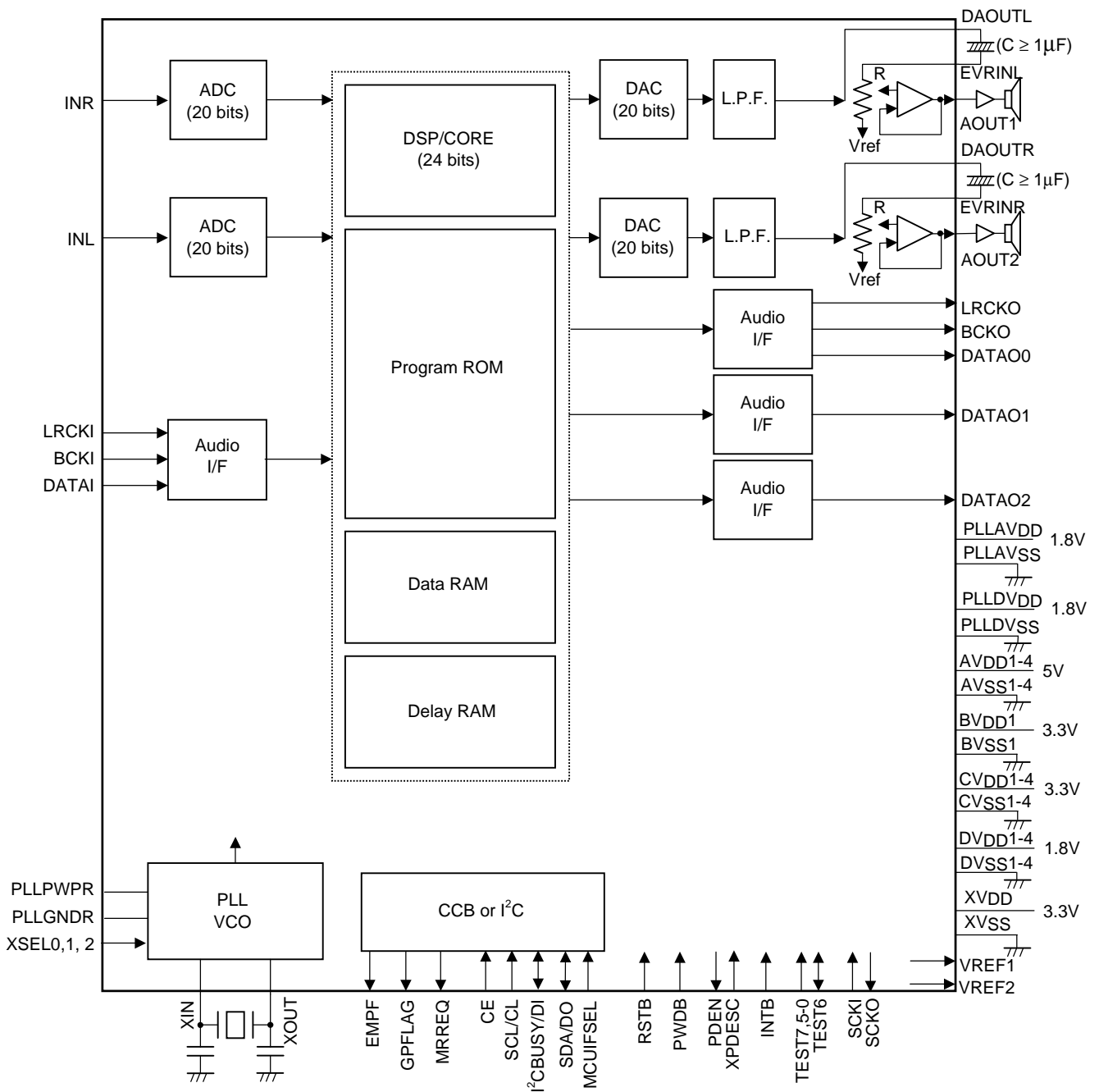
LC75051E

Continued from preceding page.

Pin Name	Input/Output	Function	Pin No.
INTB	I	Interrupt input (low active)	68
MCUIFSEL	I	Microcontroller interface select input (CCB: low, I ² C: high)	69
CE	I	Microcontroller interface chip enable, fixed at high when I ² C is selected.	70
SCL/CL	I	Microcontroller interface clock input	71
I2CBUSY/DI	I/O	Microcontroller interface data input/I ² C BUSY output	72
SDA/DO	I/O	Microcontroller interface data input/output	73
EMPF	O	CCB input register status monitor flag	78
GPFLAG	O	DSP-to-MCU general-purpose flag (high active)	77
MRREQ	O	DSP-to-MCU communication error flag	76
XPDESC	I	DSP power down reset signal (low active)	62
PDEN	O	DSP power down signal (high active)	63
XSEL0	I/O	Crystal frequency select signal 0	42
XSEL1	I/O	Crystal frequency select signal 1	43
XSEL2	I/O	Crystal frequency select signal 2	44
TEST7	I	Test pin	54
TEST0, TEST1, TEST2, TEST3, TEST4, TEST5	I	Test pin	17, 18, 7, 8, 19, 20
TEST6	I/O	Test pin	41
XIN		Crystal oscillator input	13
XOUT		Crystal oscillator output	12
XVDD		Power supply for crystal oscillator	14
XVSS		GND for crystal oscillator	11
VREF1	AO	Reference voltage output pin 1 (ADC)	36
VREF2	AO	Reference voltage output pin 2 (DAC, EVR)	35
AVDD1		ADC analog power supply (+5V)	40
AVSS1		ADC analog GND	39
AVDD2		VREF V _{DD} (+5V)	34
AVSS2		VREF GND	33
AVDD3		EVR analog V _{DD} (+5V)	25
AVSS3		EVR analog GND	26
AVDD4		DAC analog V _{DD} (+5V)	24
AVSS4		DAC analog GND	23
BVDD1		Analog chip logic power supply (+3.3V)	22
BVSS1		Analog chip logic GND	21
CVDD1, CVDD2, CVDD3, CVDD4		Digital power supply (3.3V)	46, 61, 80, 15
CVSS1, CVSS2, CVSS3, CVSS4		Digital GND	45, 60, 79, 16
DVDD1, DVDD2, DVDD3, DVDD4		Digital power supply (1.8V)	52, 65, 75, 10
DVSS1, DVSS2, DVSS3, DVSS4		Digital GND	51, 64, 74, 9
PLLPWRR		Powering for PLL (ESD) (1.8V)	1
PLLGNDR		GND for PLL (ESD)	2
PLLAVDD		Power supply for PLL (1.8V)	3
PLLAVSS		GND for PLL	4
PLLDVDD		Digital power supply for PLL (1.8V)	5
PLLDVSS		Digital GND for PLL	6

LC75051E

Block Diagram



For sample external circuit configurations, see "LC75051E External Circuit Configuration Examples (Draft)".

- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of June, 2006. Specifications and information herein are subject to change without notice.