OVERVIEW

The SM5330A is a 4-system input switching 3-channel video filter with 5th-order lowpass filter built-in. The lowpass filter cutoff frequency range is 5MHz to 13MHz (SD mode) or 16MHz to 40MHz (HD mode), controlled using an I^2C BUS*1. The lowpass filter enables the device to be utilized in the analog input stage of video signal equipment, functioning as an ADC system anti-aliasing filter for 480i to 1080i signal systems. The signal input type and input system switching, in addition to the cutoff frequency, can be controlled using the I^2C BUS. The I^2C BUS slave address is set using the ADS pin (3-state input), allowing a maximum of three SM5330A devices to be controlled simultaneously.

*1. I^2C BUS is a registered trademark of Philips Electronics N.V.

FEATURES

- Supply voltages
  - Analog : 4.75 to 5.25V
  - Digital : 3.0 to 5.5V
- 4-system input switch function (3 channels)
- Lowpass filter function with 64-level cutoff frequency setting for each of SD/HD modes
  - Cutoff frequency range
    SD : 5MHz to 13MHz
    HD : 16MHz to 40MHz
- Video input pins can be independently set to sync-tip clamp/bias/direct inputs
- Output muting function
- 2 × 8-bit D/A converters built-in for control of arbitrary external circuits
- I^2C BUS interface control
  - Slave address: 48h, 49h, 4Ah select (up to three devices can be used simultaneously, selected by ADS input)
  - Data transfer rate: fast mode (400kbit/s) compatible
  - Control register write function, status register read function
- Output gain: 6dB
- Operating ambient temperature range: –20 to 70°C
- Package: 48-pin LQFP

APPLICATIONS

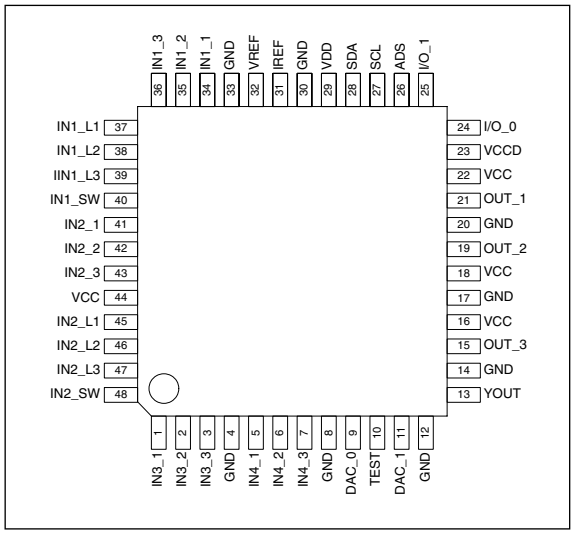
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5330AF	48-pin LQFP

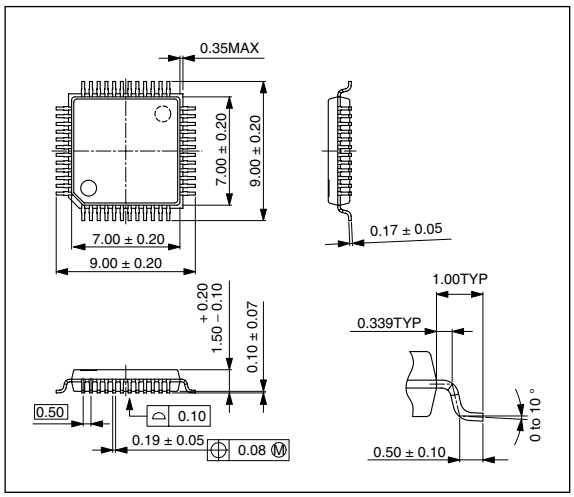
PINOUT

(Top view)

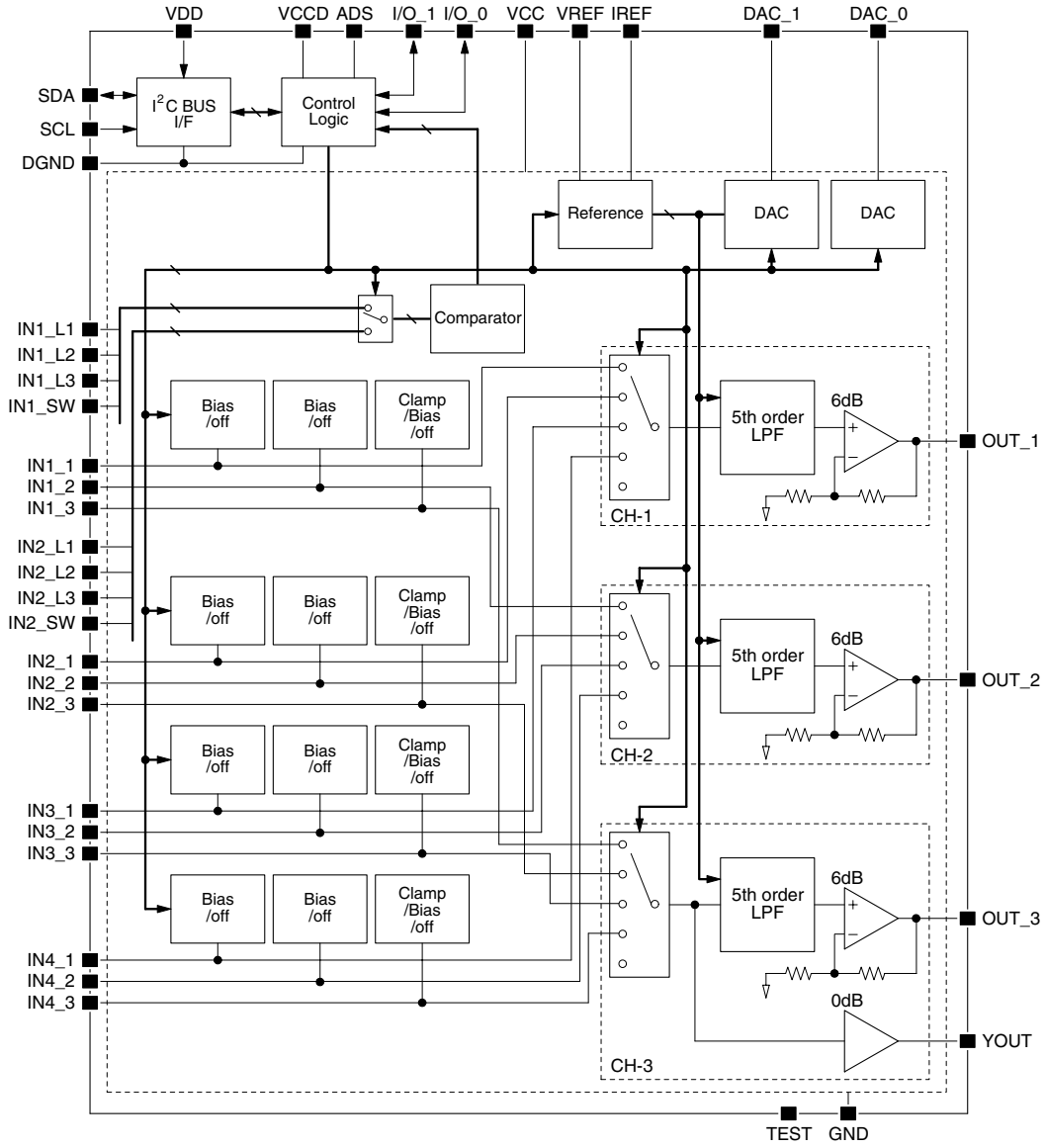


PACKAGE DIMENSION

(Unit: mm)
Weight: 0.18g



BLOCK DIAGRAM



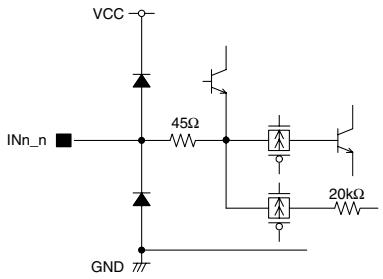
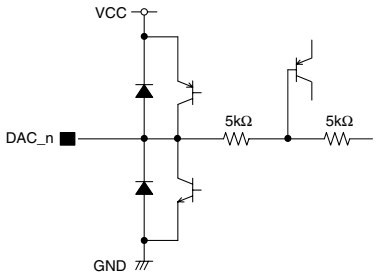
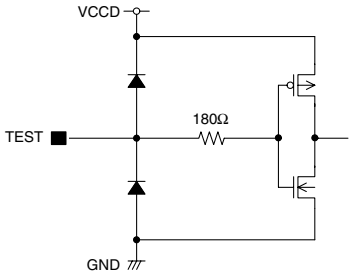
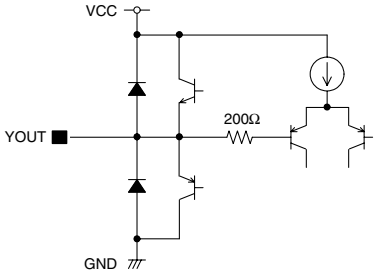
PIN DESCRIPTION

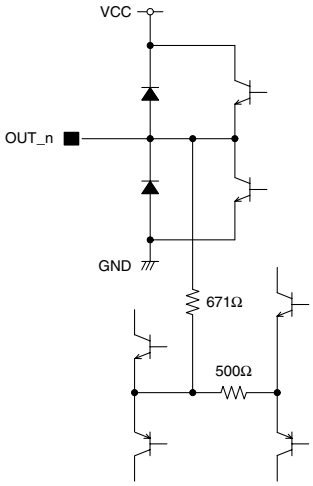
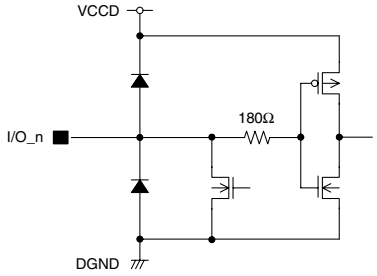
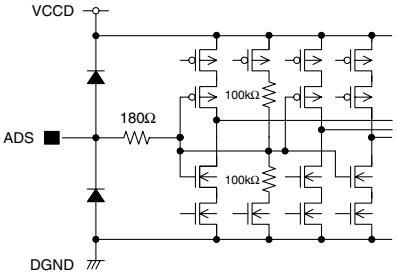
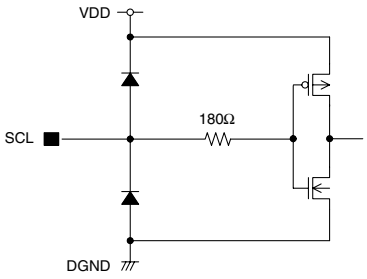
Number	Name	I/O*1	A/D*2	Description
1	IN3_1	I	A	System 3 channel 1 video signal input pin
2	IN3_2	I	A	System 3 channel 2 video signal input pin
3	IN3_3	I	A	System 3 channel 3 video signal input pin
4	GND	GND	A	Analog ground pin
5	IN4_1	I	A	System 4 channel 1 video signal input pin
6	IN4_2	I	A	System 4 channel 2 video signal input pin
7	IN4_3	I	A	System 4 channel 3 video signal input pin
8	GND	GND	A	Analog ground pin
9	DAC_0	O	A	DAC voltage output pin. Output voltage set using the I^2C BUS.
10	TEST	I	D	Test pin. Connect to ground for normal operation.
11	DAC_1	O	A	DAC voltage output pin. Output voltage set using the I^2C BUS.
12	GND	GND	A	Analog ground pin
13	YOUT	O	A	Y signal output pin. The channel 3 video signal is output without filtering.
14	GND	GND	A	Analog ground pin
15	OUT_3	O	A	Channel 3 video signal output pin. The output system is selected using the I^2C BUS.
16	VCC	P	A	Analog supply pin
17	GND	GND	A	Analog ground pin
18	VCC	P	A	Analog supply pin
19	OUT_2	O	A	Channel 2 video signal output pin. The output system is selected using the I^2C BUS.
20	GND	GND	A	Analog ground pin
21	OUT_1	O	A	Channel 1 video signal output pin. The output system is selected using the I^2C BUS.
22	VCC	P	A	Analog supply pin
23	VCCD	P	D	Logic supply pin. Connect to the same potential as VCC.
24	I/O_0	I/O	D	Logic I/O pins. Outputs are open-drain. Connect pull-up to VCCD. The open-drain outputs are turned ON/OFF using I^2C BUS settings. The input state can be read out via the I^2C BUS.
25	I/O_1	I/O	D	
26	ADS	I	D	Address select pin. 3-state input Select the I^2C BUS slave address. (L: 48h, H: 49h, Z: 4Ah)
27	SCL	I	D	I^2C BUS clock signal pin. Connect pull-up to VDD.
28	SDA	I/O	D	I^2C BUS data signal pin. Connect pull-up to VDD. The output is open-drain.
29	VDD	P	D	I^2C BUS interface-stage supply pin. 3.0V to 5.5V
30	DGND	GND	D	Logic ground pin
31	IREF	O	A	Cutoff frequency control pin. Connect a 1.8kΩ ±1% resistor between this pin and GND. The current that flows in the resistor sets the internal filter reference current.
32	VREF	O	A	Internal reference voltage pin
33	GND	GND	A	Analog ground pin
34	IN1_1	I	A	System 1 channel 1 video signal input pin
35	IN1_2	I	A	System 1 channel 2 video signal input pin
36	IN1_3	I	A	System 1 channel 3 video signal input pin

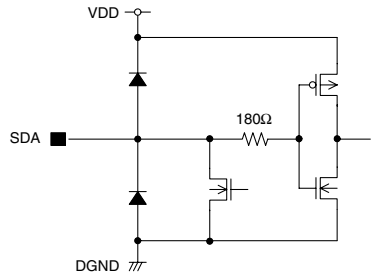
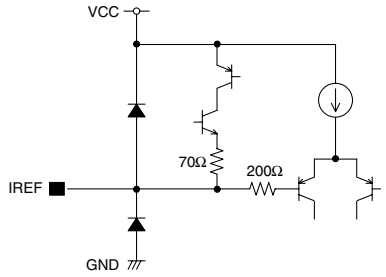
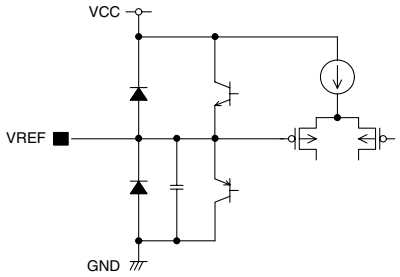
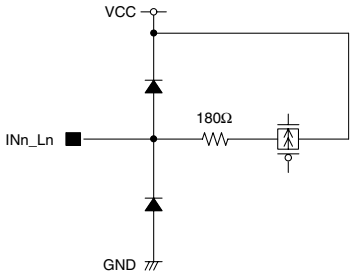
Number	Name	I/O*1	A/D*2	Description
37	IN1_L1	I	D	System 1 D-terminal signal discriminator input pin. 3-state input
38	IN1_L2	I	D	System 1 D-terminal signal discriminator input pin
39	IN1_L3	I	D	System 1 D-terminal signal discriminator input pin. 3-state input
40	IN1_SW	I	D	System 1 D-terminal signal discriminator input pin
41	IN2_1	I	A	System 2 channel 1 video signal input pin
42	IN2_2	I	A	System 2 channel 2 video signal input pin
43	IN2_3	I	A	System 2 channel 3 video signal input pin
44	VCC	P	A	Analog supply pin
45	IN2_L1	I	D	System 2 D-terminal signal discriminator input pin. 3-state input
46	IN2_L2	I	D	System 2 D-terminal signal discriminator input pin
47	IN2_L3	I	D	System 2 D-terminal signal discriminator input pin. 3-state input
48	IN2_SW	I	D	System 2 D-terminal signal discriminator input pin

*1. I: input, O: output, P: Power supply, GND: Ground
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O*1	Equivalent circuit
34 35 36 41 42 43 1 2 3 5 6 7	IN1_1 IN1_2 IN1_3 IN2_1 IN2_2 IN2_3 IN3_1 IN3_2 IN3_3 IN4_1 IN4_2 IN4_3	I	
9 11	DAC_0 DAC_1	O	
10	TEST	I	
13	YOUT	O	

Number	Name	I/O*1	Equivalent circuit
15 19 21	OUT_3 OUT_2 OUT_1	O	
24 25	I/O_0 I/O_1	I/O	
26	ADS	I	
27	SCL	I	

Number	Name	I/O*1	Equivalent circuit
28	SDA	I/O	
31	IREF	O	
32	VREF	O	
37 38 39 40 45 46 47 48	IN1_L1 IN1_L2 IN1_L3 IN1_SW IN2_L1 IN2_L2 IN2_L3 IN2_SW	I	

*1. I: input, O: output

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V, VCC = VDD = VCCD

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	VCC, VDD, VCCD	−0.3 to 7.0	V
Input voltage	V_{IN}		GND − 0.3 to V_{CC} + 0.3	V
Storage temperature range	T_{STG}		−55 to +125	°C
Power dissipation	P_D	θ_{ja} = 60°C/W (at Ta = 25°C, PCB wiring density: 100%, 0.5m/s air flow)	0.91	W
Junction temperature	T_J		125	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC, VCCD	4.75 to 5.25	V
Supply voltage 2	V_{DD}	VDD	3.0 to 5.5	V
Operating ambient temperature	Ta	Wiring density: 100%, air flow: 0.5m/s	−20 to 70	°C

Electrical Characteristics

DC Characteristics

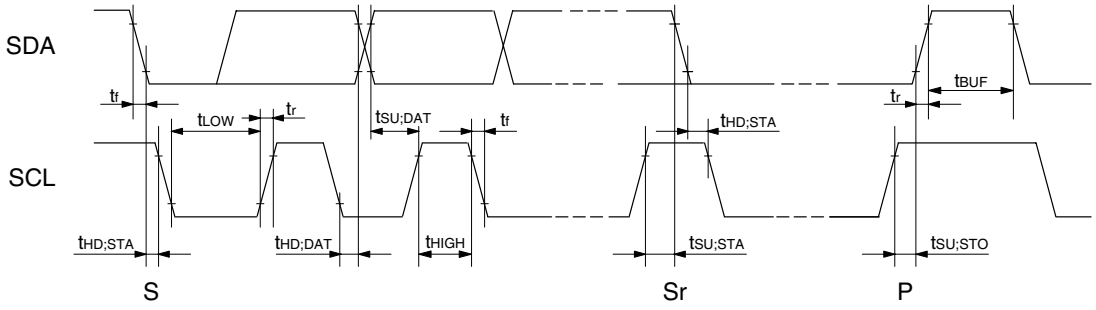
V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75kΩ, CH-1 and CH-2 bias inputs, CH-3 clamp input, FCM = H, FCSET = 3Fh, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption	I_{CC1}	V_{CC} = 5.25V, V_{IN} = 0.0V_{P-P}	–	112	154	mA	I
HIGH-level input voltage 1	V_{IH1}	SDA, SCL	0.7 V_{DD}	–	–	V	I
LOW-level Input voltage 1	V_{IL1}		–	–	0.3 V_{DD}	V	I
HIGH-level input voltage 2	V_{IH2}	ADS	0.8 V_{CC}	–	–	V	I
Middle-level input voltage 2	V_{IM2}		$V_{CC}/2$ − 0.2	–	$V_{CC}/2$ + 0.2	V	I
LOW-level input voltage 2	V_{IL2}		–	–	0.2 V_{CC}	V	I
HIGH-level input voltage 3	V_{IH3}	IN1_L1, IN1_L3, IN2_L1, IN2_L3	3.5	–	–	V	I
Middle-level input voltage 3	V_{IM3}		1.4	–	2.4	V	I
LOW-level input voltage 3	V_{IL3}		–	–	0.8	V	I
HIGH-level input voltage 4	V_{IH4}	IN1_L2, IN2_L2	3.5	–	–	V	I
LOW-level Input voltage 4	V_{IL4}		–	–	2.4	V	I
HIGH-level input voltage 5	V_{IH5}	IN1_SW, IN2_SW	3.2	–	–	V	I
LOW-level Input voltage 5	V_{IL5}		–	–	1.8	V	I
HIGH-level input voltage 6	V_{IH6}	I/O_0, I/O_1	3.0	–	–	V	I
LOW-level Input voltage 6	V_{IL6}		–	–	1.5	V	I
HIGH-level input leakage current 1	I_{LH1}	SDA, SCL at input voltage = V_{DD}	–	–	± 1.0	µA	I
LOW-level input leakage current 1	I_{LL1}	SDA, SCL at input voltage = 0V	–	–	± 1.0	µA	I
HIGH-level input leakage current 2	I_{LH2}	I/O_0, I/O_1 at input voltage = V_{CC}	–	–	± 1.0	µA	I
LOW-level input leakage current 2	I_{LL2}	I/O_0, I/O_1 at input voltage = 0V	–	–	± 1.0	µA	I
LOW-level output voltage	V_{OL}	SDA, I/O_0, I/O_1 at output current = 3mA	0.0	–	0.4	V	I

I²C BUS AC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL LOW-level clock pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL HIGH-level clock pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
Bus free time (stop condition to start condition)	t_{BUF}		1.3	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II



Note. S, Sr: start condition, P: stop condition

Analog Input Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75kΩ, FCM = H, FCSET = 3Fh, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage	V_{CLAMP}	Clamp input	1.65	1.85	2.05	V	I
Bias voltage	V_{BIAS}	Bias input	2.15	2.35	2.55	V	I
Input resistance	R_{IBIAS}	Bias input	–	20	–	kΩ	II
Input amplitude 1	V_{AI1}	Clamp input, THD < 1.0%	–	–	1.2	Vp-p	I
Input amplitude 2	V_{AI2}	Bias input, THD < 1.0%	–	–	1.2	Vp-p	I
Input DC voltage range	V_{IDC}	Direct input	1.5	–	3.0	V	I

Analog Output Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, FCM = H, FCSET = 3Fh, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Output gain	A_V	OUT_1, OUT_2, OUT_3	5.5	6.0	6.5	dB	I
Gain error between channels	dA_V	Between OUT_1, OUT_2, and OUT_3	–	–	± 0.2	dB	I
Output amplitude 1	V_{OUT1}	Clamp input, THD < 1.0%	–	–	2.4	Vp-p	I
Output amplitude 2	V_{OUT2}	Bias input, THD < 1.0%	–	–	2.4	Vp-p	I
Crosstalk between channels	$XTLK_{CH}$	0.5Vp-p input, fin = 1MHz, between 2 channels	–	–70	–	dB	II
Crosstalk between input systems	$XTLK_{MUX}$	0.5Vp-p input, fin = 1MHz, between each input system	–	–70	–	dB	II
Drive load resistance	R_L	OUT_1, OUT_2, OUT_3	75	–	–	Ω	I
I^2C response time	t_{IIC}	Response time from ACK bit output when changing settings using I^2C BUS	–	–	1	µs	II

Filter Frequency Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75kΩ, CH-1 and CH-2 bias inputs, CH-3 clamp input, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency	f_{C1}	FCM = 0, FCSET = 00h	4.50	5.11	5.72	MHz	I
	f_{C2}	FCM = 0, FCSET = 3Fh	11.71	13.30	14.89	MHz	I
	f_{C3}	FCM = 1, FCSET = 00h	13.74	15.61	17.48	MHz	I
	f_{C4}	FCM = 1, FCSET = 32h	30.96	35.18	39.40	MHz	I
	f_{C5}	FCM = 1, FCSET = 3Fh	–	40.27	–	MHz	II
4fc attenuation	A_{SB}	fin = 4fc, attenuation from fin = 100kHz	–	60	–	dB	II

DAC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Differential linearity	DLE	DAC_0, DAC_1, $\frac{V_n - V_{n-1}}{(V_{191} - V_{63})/128} - 1$, n = 1 to 255 V_n: output voltage at resister value set "n"	–1	0	+1	LSB	I
DAC HIGH-level output voltage	V_{OH-DAC}	DAC_0, DAC_1, DAC0 = DAC1 = FFh	4.30	4.45	4.60	V	I
DAC LOW-level output voltage	V_{OL-DAC}	DAC_0, DAC_1, DAC0 = DAC1 = 00h	0.25	0.35	0.45	V	I
DAC output current	I_{O-DAC}	DAC0 = DAC1 = FFh	–0.5	–	+0.5	mA	I

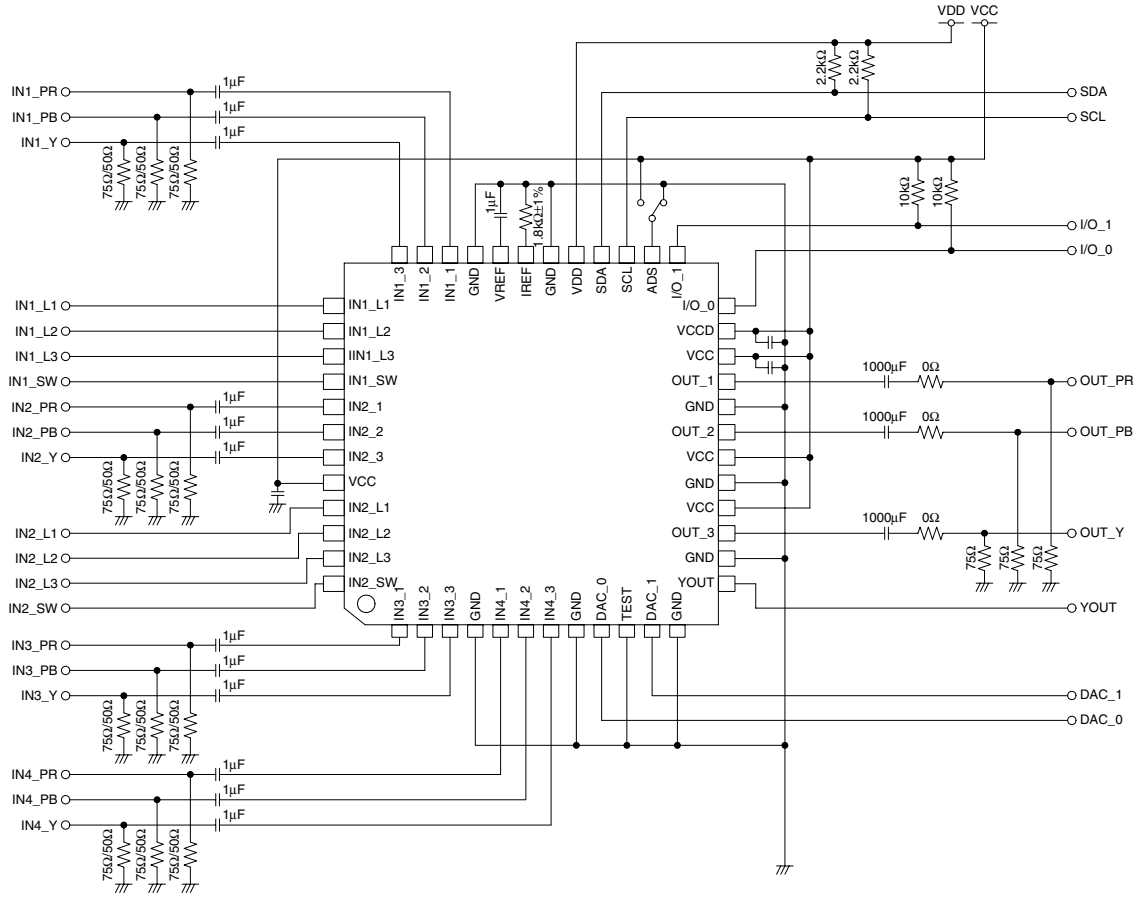
Test Level

The definition of "Test Level" shown in the electric characteristic table is as follows.

I : 100% of products tested at Ta = + 25°C.

II : Guaranteed as result of design and characteristics evaluation.

Measurement Circuit



Note. This is a circuit only for the evaluation board of an electric characteristics. (It is not a recommended application circuit.)

FUNCTIONAL DESCRIPTION

I²C BUS Control

The SM5330A uses the I²C BUS interface to control the following functions:

1) Cutoff frequency setting
2) Input type switching (synctip clamp, bias, or direct mode)
3) Mute setting
4) Input switch select
5) I/O output settings
6) DAC output settings

In addition, the interface is used to read the following status parameters:

7) I/O input state
8) D-terminal signal discrimination result

The transfer rate is compatible with fast mode (400kbit/s).

Basic Cycle

The write sequence is: SM5330A slave address → specific control register sub-address → write data. Data can be written to the SM5330A in successive bytes, as the sub-address for the register is incremented automatically after each byte. However, if the sub-address exceeds the address of the last register (04h), data write operation to the SM5330A register stops and the acknowledge signal is not returned.

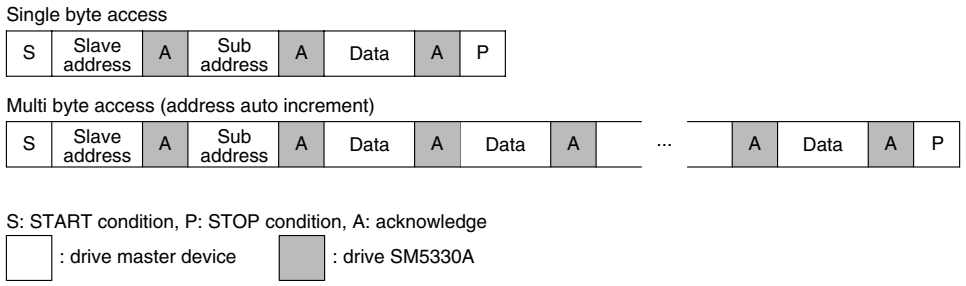


Figure 1. Write sequence

The read sequence is: SM5330A slave address → sub-address 0 status register value → sub-address 1 status register value → sub-address 2 status register value. Each read cycle comprises 3 bytes of read data. A specific status register sub-address cannot be assigned for a read operation.

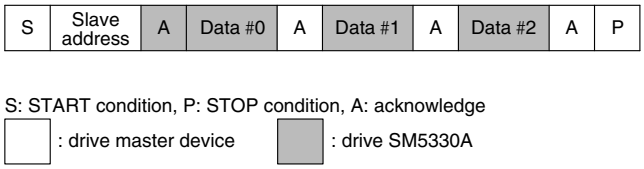


Figure 2. Read sequence

Slave Address

The 7-bit slave address is selected using the ADS pin. When ADS = “L” the address is 48h, when ADS = “H” the address is 49h, and when ADS = “Z” (open) the address is 4Ah. A maximum of three SM5330A devices can be connected to one I^2C BUS simultaneously, and controlled independently by setting the slave address of each using the ADS pin.

SLAVE ADDRESS for control register write

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SLAVE ADDRESS							R/W		
Value	1	0	0	1	0	0	0	0	90h	Indicate to write when device's slave address is 48h (ADS = "L")
	1	0	0	1	0	0	1	0	92h	Indicate to write when device's slave address is 49h (ADS = "H")
	1	0	0	1	0	1	0	0	94h	Indicate to write when device's slave address is 4Ah (ADS = "Z")

SLAVE ADDRESS for status register read

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	SLAVE ADDRESS							R/W		
Value	1	0	0	1	0	0	0	1	91h	Indicate to read when device's slave address is 48h (ADS = "L")
	1	0	0	1	0	0	1	1	93h	Indicate to read when device's slave address is 49h (ADS = "H")
	1	0	0	1	0	1	0	1	95h	Indicate to read when device's slave address is 4Ah (ADS = "Z")

Control Register

The SM5330A has a 5-byte control register.

CONTROL REGISTER MAP

Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
00h	FCM	–	FCSET						Filter fc setting
01h	IM1		IM2		IM3		IM4		Input mode setting
02h	–	INSEL			–	–	I/O1	I/O0	Input switch select, I/O output control
03h	DAC0								DAC_0 output control
04h	DAC1								DAC_1 output control

The function of each byte in the control register is described in the following tables.

SUB ADDRESS: 00h – Filter fc setting

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	FCM	–	FCSET							
default	0	0	0	0	0	0	0	0	00h	
Value	**0**									Set filter to SD mode (default)
	1									Set filter to HD mode
	0	0	**0**	**0**	**0**	**0**	**0**	**0**	00h	fc = 5.11MHz (default)
	0	0	:						:	:
	0	0	**1**	**1**	**1**	**1**	**1**	**1**	3Fh	fc = 13.30MHz
	1	0	**0**	**0**	**0**	**0**	**0**	**0**	80h	fc = 15.61MHz
	1	0	:						:	:
	1	0	**1**	**1**	**1**	**1**	**1**	**1**	BFh	fc = 40.27MHz

Sets the cutoff frequency. When FCM = “0” the filter is set to SD mode, and when FCM = “1” the filter is set to HD mode. The relationship between the register value and the cutoff frequency is described in section “Low-pass Filter”.

SUB ADDRESS: 01h – Input mode setting

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	IM1		IM2		IM3		IM4			
default	0	0	0	0	0	0	0	0	00h	
Value	**0**	**0**								IN1_3: synctip clamp input, IN1_2 and IN1_1: bias input (default)
	0	**1**								IN1_3, IN1_2 and IN1_1: bias input
	1	**0**								IN1_3, IN1_2 and IN1_1: synctip clamp input
	1	**1**								IN1_3, IN1_2 and IN1_1: direct (DC) input
			0	**0**						IN2_3: synctip clamp input, IN2_2 and IN2_1: bias input (default)
			0	**1**						IN2_3, IN2_2 and IN2_1: bias input
			1	**0**						IN2_3, IN2_2 and IN2_1: synctip clamp input
			1	**1**						IN2_3, IN2_2 and IN2_1: direct (DC) input
					0	**0**				IN3_3: synctip clamp input, IN3_2 and IN3_1: bias input (default)
					0	**1**				IN3_3, IN3_2 and IN3_1: bias input
					1	**0**				IN3_3, IN3_2 and IN3_1: synctip clamp input
					1	**1**				IN3_3, IN3_2 and IN3_1: direct (DC) input
							0	**0**		IN4_3: synctip clamp input, IN4_2 and IN4_1: bias input (default)
							0	**1**		IN4_3, IN4_2 and IN4_1: bias input
							1	**0**		IN4_3, IN4_2 and IN4_1: synctip clamp input
							1	**1**		IN4_3, IN4_2 and IN4_1: direct (DC) input

Sets the video signal input pin operating mode.

SUB ADDRESS: 02h – Input switch select, I/O output control

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	–	INSEL			–	–	I/O1	I/O0		
default	0	1	0	0	0	0	1	1	43h	
Value	0	**0**	×	×	0	0				Mute
	0	**1**	**0**	**0**	0	0				IN1_n select (default)
	0	**1**	**0**	**1**	0	0				IN2_n select
	0	**1**	**1**	**0**	0	0				IN3_n select
	0	**1**	**1**	**1**	0	0				IN4_n select
	0				0	0	**0**			I/O_1 output "L"
	0				0	0	**1**			I/O_1 output off (input available) (default)
	0				0	0		**0**		I/O_0 output "L"
	0				0	0		**1**		I/O_0 output off (input available) (default)

Sets the video signal input switching and logic I/O pin output settings. The input can be switched between 4 systems (3-channels). This setting also determines the system that performs status register D-terminal discrimination. The I/O_0 and I/O_1 pins are n-channel MOS open-drain outputs. When the I/O pins are used as inputs, these bits are set to “1” so that the output is high impedance.

SUB ADDRESS: 03h – DAC_0 output control

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	DAC0									
default	0	0	0	0	0	0	0	0	00h	
Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h	DAC_0 output 0.35V (default)
	:								:	:
	1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	FFh	DAC_0 output 4.45V

SUB ADDRESS: 04h – DAC_1 output control

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	(Hex)	Description
Name	DAC1									
default	0	0	0	0	0	0	0	0	00h	
Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h	DAC_1 output 0.35V (default)
	:								:	:
	1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	FFh	DAC_1 output 4.45V

Sets the DAC_0 and DAC_1 pins output voltage, respectively.

Status Register

The SM5330A has a 3-byte status register.

STATUS REGISTER MAP

Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
00h	–	–	–	–	–	–	IN1	IN0	I/O input status
01h	L1			L2		L3			D-terminal input status
02h	–	–	–	–	–	–	SW1	SW2	D-terminal connection status

The function of each byte in the status register is described in the following tables.

SUB ADDRESS: 00h – I/O input status

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
Name	–	–	–	–	–	–	**IN1**	**IN0**	
Value	0	0	0	0	0	0	**0**		I/O_1 input "L" (< 1.5V)
	0	0	0	0	0	0	**1**		I/O_1 input "H" (> 3.0V)
	0	0	0	0	0	0		**0**	I/O_0 input "L" (< 1.5V)
	0	0	0	0	0	0		**1**	I/O_0 input "H" (> 3.0V)

Returns the input state of the logic I/O pins. The I/O_0 and I/O_1 pins are n-channel MOS open-drain outputs. When the I/O pins are used as inputs, set the outputs “1” (high impedance) in the control register.

SUB ADDRESS: 01h – D-terminal input status

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
Name	L1			L2		L3			
Value									Decode INn_Ln input selected series via INSEL register
									(L1: screen ruling)
	0	0	1						INn_L1 input "L" (< 0.8V) means "480"
	0	1	0						INn_L1 input "M" (1.4 to 2.4V) means "720"
	1	0	0						INn_L1 input "H" (> 3.5V) means "1080"
									(L2: I/P)
				0	1				INn_L2 input "L" (< 2.4V) means "60i"
				1	0				INn_L2 input "H" (> 3.5V) means "60p"
									(L3: aspect ratio)
						0	0	1	INn_L3 input "L" (< 0.8V) means "4 : 3"
						0	1	0	INn_L3 input "M" (1.4 to 2.4V) means "Letter Box"
						1	0	0	INn_L3 input "H" (> 3.5V) means "16 : 9"

Returns the D-terminal discrimination result for the system determined by the INSEL register.

SUB ADDRESS: 02h – D-terminal connection status

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
Name	–						SW1	SW2	
Value	0	0	0	0	0	0	0		IN1_SW input "L" (< 1.8V) means "connected"
	0	0	0	0	0	0	1		IN1_SW input "H" (> 3.2V) means "unconnected"
	0	0	0	0	0	0		0	IN2_SW input "L" (< 1.8V) means "connected"
	0	0	0	0	0	0		1	IN2_SW input "H" (> 3.2V) means "unconnected"

Returns the D-terminal connection status information.

Input Circuit

The SM5330A video input pin operating mode can be switched between synctip clamp, bias, and direct (without DC restore) modes for each channel. The possible combinations are described below (set independently for each system).

Table 1. Input mode combination

Control register	Input mode		
IMn value	INn_1	INn_2	INn_3
00 b	Bias	Bias	Clamp
01 b	Bias	Bias	Bias
10 b	Clamp	Clamp	Clamp
11 b	Direct	Direct	Direct

The SM5330A has a 4-system input switch built-in, and the system selected by the control register INSEL bits is input to the lowpass filter. When muting is selected (INSEL = 000b), the signal is not input to the lowpass filter and the output pins are DC level.

Lowpass Filter

The SM5330A has a 5th-order lowpass filter built-in, with a cutoff frequency selectable from 64 levels each for SD/HD mode controlled using the I^2C BUS. The cutoff frequency settings are displayed graphically in figure 3, and shown in table 2.

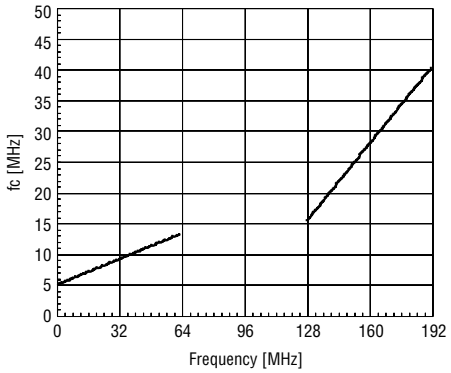


Figure 3. FCSET setting vs. Cutoff frequency

Table 2. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]
0	00	5.11	16	10	7.19	32	20	9.27	48	30	11.35
1	01	5.24	17	11	7.32	33	21	9.40	49	31	11.48
2	02	5.37	18	12	7.45	34	22	9.53	50	32	11.61
3	03	5.50	19	13	7.58	35	23	9.66	51	33	11.74
4	04	5.63	20	14	7.71	36	24	9.79	52	34	11.87
5	05	5.76	21	15	7.84	37	25	9.92	53	35	12.00
6	06	5.89	22	16	7.97	38	26	10.05	54	36	12.13
7	07	6.02	23	17	8.10	39	27	10.18	55	37	12.26
8	08	6.15	24	18	8.23	40	28	10.31	56	38	12.39
9	09	6.28	25	19	8.36	41	29	10.44	57	39	12.52
10	0A	6.41	26	1A	8.49	42	2A	10.57	58	3A	12.65
11	0B	6.54	27	1B	8.62	43	2B	10.70	59	3B	12.78
12	0C	6.67	28	1C	8.75	44	2C	10.83	60	3C	12.91
13	0D	6.80	29	1D	8.88	45	2D	10.96	61	3D	13.04
14	0E	6.93	30	1E	9.01	46	2E	11.09	62	3E	13.17
15	0F	7.06	31	1F	9.14	47	2F	11.22	63	3F	13.30

FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]	FCDATA	FCSET (hex)	fc [MHz]
128	80	15.61	144	90	21.88	160	A0	28.14	176	B0	34.40
129	81	16.01	145	91	22.27	161	A1	28.53	177	B1	34.79
130	82	16.40	146	92	22.66	162	A2	28.92	178	B2	35.18
131	83	16.79	147	93	23.05	163	A3	29.31	179	B3	35.58
132	84	17.18	148	94	23.44	164	A4	29.70	180	B4	35.97
133	85	17.57	149	95	23.83	165	A5	30.10	181	B5	36.36
134	86	17.96	150	96	24.22	166	A6	30.49	182	B6	36.75
135	87	18.35	151	97	24.62	167	A7	30.88	183	B7	37.14
136	88	18.75	152	98	25.01	168	A8	31.27	184	B8	37.53
137	89	19.14	153	99	25.40	169	A9	31.66	185	B9	37.92
138	8A	19.53	154	9A	25.79	170	AA	32.05	186	BA	38.32
139	8B	19.92	155	9B	26.18	171	AB	32.44	187	BB	38.71
140	8C	20.31	156	9C	26.57	172	AC	32.84	188	BC	39.10
141	8D	20.70	157	9D	26.96	173	AD	33.23	189	BD	39.49
142	8E	21.09	158	9E	27.36	174	AE	33.62	190	BE	39.88
143	8F	21.48	159	9F	27.75	175	AF	34.01	191	BF	40.27

YOUT Pin

The YOUT pin is the unfiltered output of the selected system input pin (IN1_3, IN2_3, IN3_3, or IN4_3). The output gain is approximately 0dB.

IREF Pin

The IREF pin controls the built-in lowpass filter reference current, using a 1.8kΩ ± 1% control resistor that must be connected. The current flows into the IREF pin in normal operating mode and during output muting.

VREF Pin

The VREF pin is the internal reference voltage output. It is recommended that a capacitor be connected between VREF and GND to ensure SM5330A operating stability. The recommended value is 1µF. The voltage on VREF is output in normal operating mode and during output muting.

D-Terminal Discrimination Function

The D-terminal signal discrimination result can be read using the I^2C BUS. The status register SW1 bit returns the state of IN1_SW, and the SW2 bit returns the state of IN2_SW. When IN1_n is selected by control register settings (INSEL = 100b), the status register L1, L2, L3 bits return the IN1_L1, IN1_L2, IN1_L3 pin states, respectively. Similarly, when IN2_n is selected (INSEL = 101b), the status register bits return the IN2_L1, IN2_L2, IN2_L3 pin states, respectively.

DAC

The SM5330A has two D/A converters controlled using the I^2C BUS. The control register DAC0 bit controls the DAC_0 pin output voltage, and the DAC1 bit controls the DAC_1 output voltage.

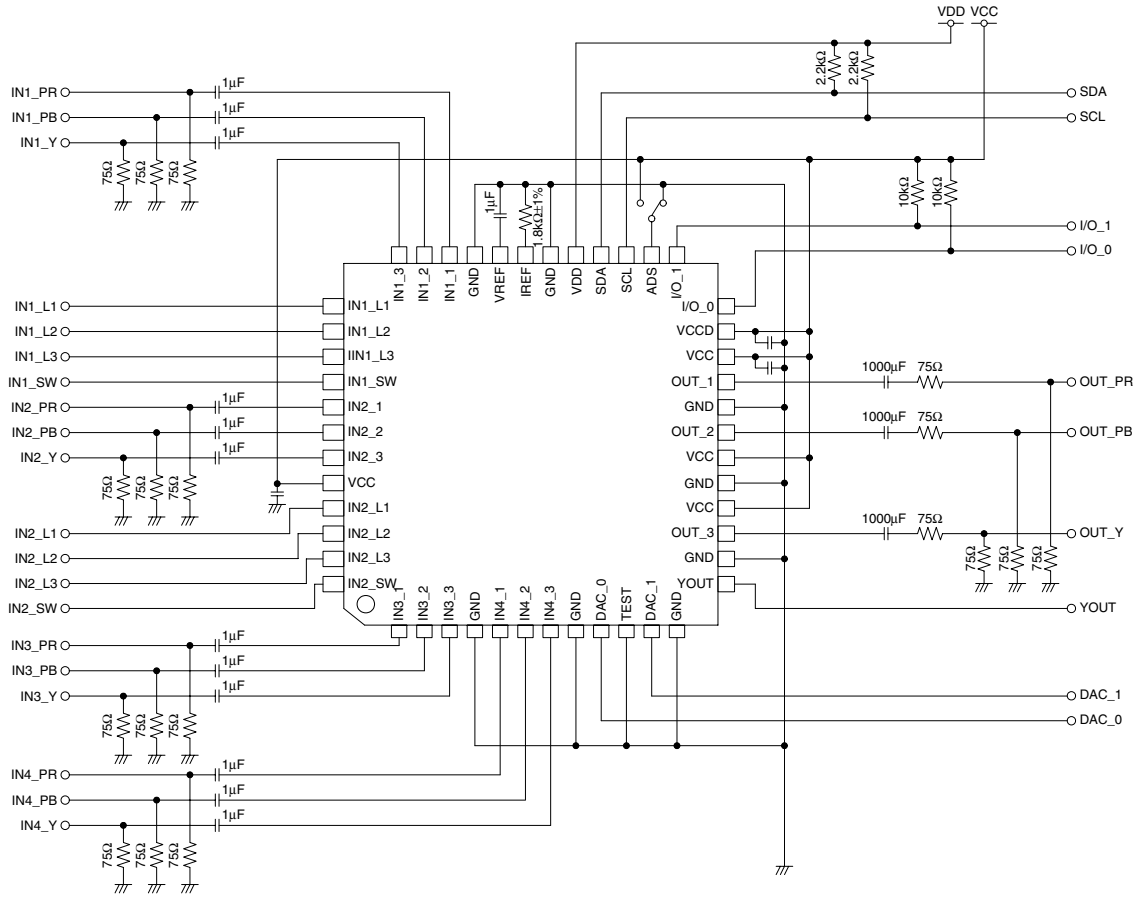
I/O

The I/O_0 and I/O_1 I/O pins in output mode are n-channel MOS open-drain outputs. Connect pull-up resistance between respective pins and the VCCD pin. Recommendation value of pull-up resistance is 10kΩ. When these pins are used as inputs, set the outputs “1” (high impedance) in the control register. When these pins are not used, they should have pull-up connections to VCCD or be connected to DGND.

Power-ON Reset

When power is applied, an internal power-ON reset circuit operates, initializing all internal register settings to their default settings. Power should be applied simultaneously on all supply pins.

RECOMMENDED APPLICATION CIRCUIT



USAGE PRECAUTIONS

Supply Connections

Ensure that the VCC and VCCD have the same potential. VDD is the I^2C BUS supply. The SCL and SDA signals should have a pull-up connection to VDD.

Setting the Slave Address to 49h

When the ADS pin is open-circuit, the slave address is set to 49h. When open, however, a large external spike noise or other interference can cause a malfunction. An external resistor should be connected to ADS as shown in figure 4 for protection.

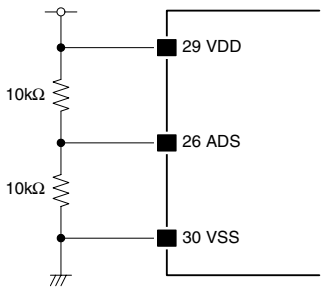


Figure 4. Slave address 49h setting

TYPICAL PERFORMANCE

V_{CC} = 5.0V, V_{DD} = 5.0V, Ta = 25°C, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 75Ω, unless otherwise noted.

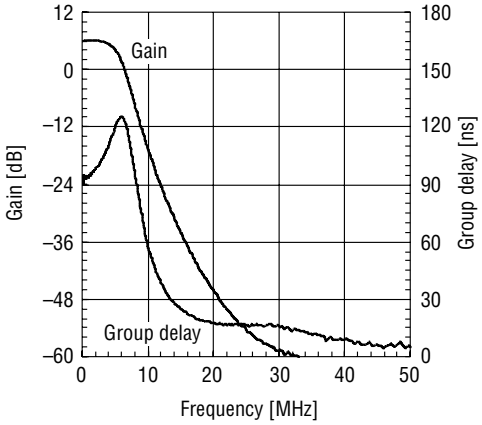


Figure 5. Gain and Group delay characteristics (FCDATA = 0)

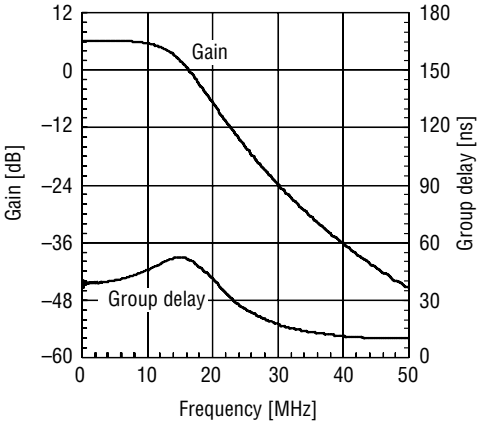


Figure 6. Gain and Group delay characteristics (FCDATA = 63)

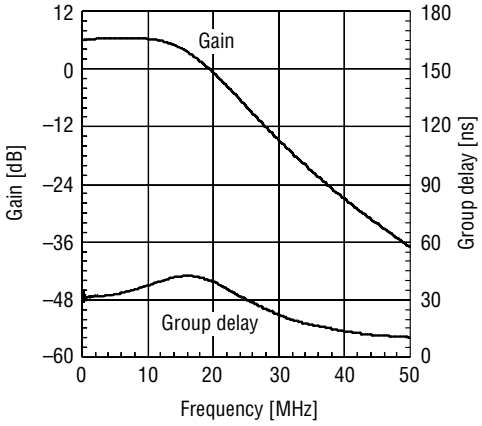


Figure 7. Gain and Group delay characteristics (FCDATA = 128)

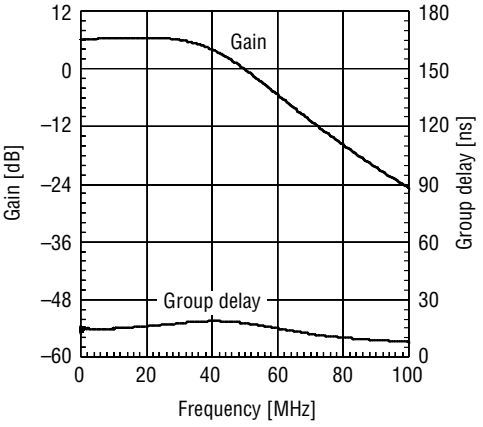


Figure 8. Gain and Group delay characteristics (FCDATA = 191)

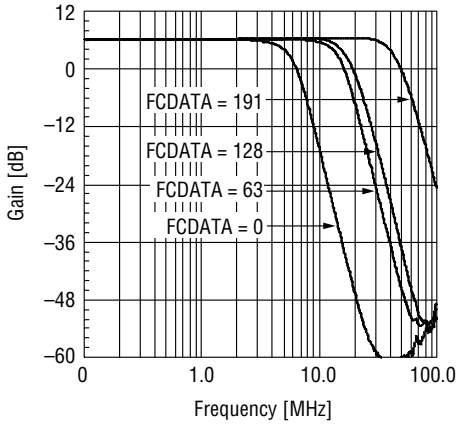


Figure 9. Gain vs. FCDATA

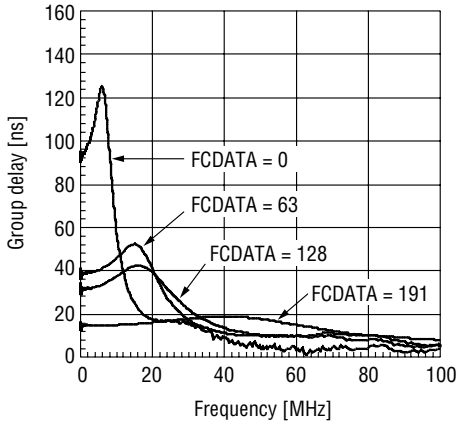


Figure 10. Group delay vs. FCDATA

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