



DIFFERENTIAL-TO-LVDS/0.7V DIFFERENTIAL PCI EXPRESS™ JITTER ATTENUATOR

ICS8741004

General Description



The ICS8741004 is a high performance Differential-to-LVDS/0.7V Differential Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS8741004 has 3 PLL bandwidth modes: 200kHz, 600kHz and 2MHz. The 200kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 600kHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 2MHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. Because some 2.5Gb serdes have x20 multipliers while others have x25 multipliers, the ICS8741004 can be set for 1:1 mode or 5/4 multiplication mode (i.e. 100MHz input/125MHz output) using the F_SEL pins.

The ICS8741004 uses IDT's 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

PLL Bandwidth

| |
|--|
| BW_SEL |
| 0 = PLL Bandwidth: ~200kHz |
| Float = PLL Bandwidth: ~600kHz (default) |
| 1 = PLL Bandwidth: ~2MHz |

Features

- Two LVDS and two 0.7V differential output pairs
Bank A has two LVDS output pairs and Bank B has two 0.7V differential output pairs
- One differential clock input pair
- CLK, $\overline{\text{CLK}}$ pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 160MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 35ps (maximum)
- Full 3.3V operating supply
- Three bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment

| | | | |
|------------------|----|----|------------------|
| QA1 | 1 | 24 | QB1 |
| QA1 | 2 | 23 | QB1 |
| V _{DDO} | 3 | 22 | V _{DDO} |
| QA0 | 4 | 21 | QB0 |
| QA0 | 5 | 20 | QB0 |
| MR | 6 | 19 | IREF |
| BW_SEL | 7 | 18 | F_SELB |
| nc | 8 | 17 | OEB |
| V _{DDA} | 9 | 16 | GND |
| F_SELA | 10 | 15 | GND |
| V _{DD} | 11 | 14 | CLK |
| OEA | 12 | 13 | CLK |

ICS8741004

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm
package body
G Package
Top View

Block Diagram

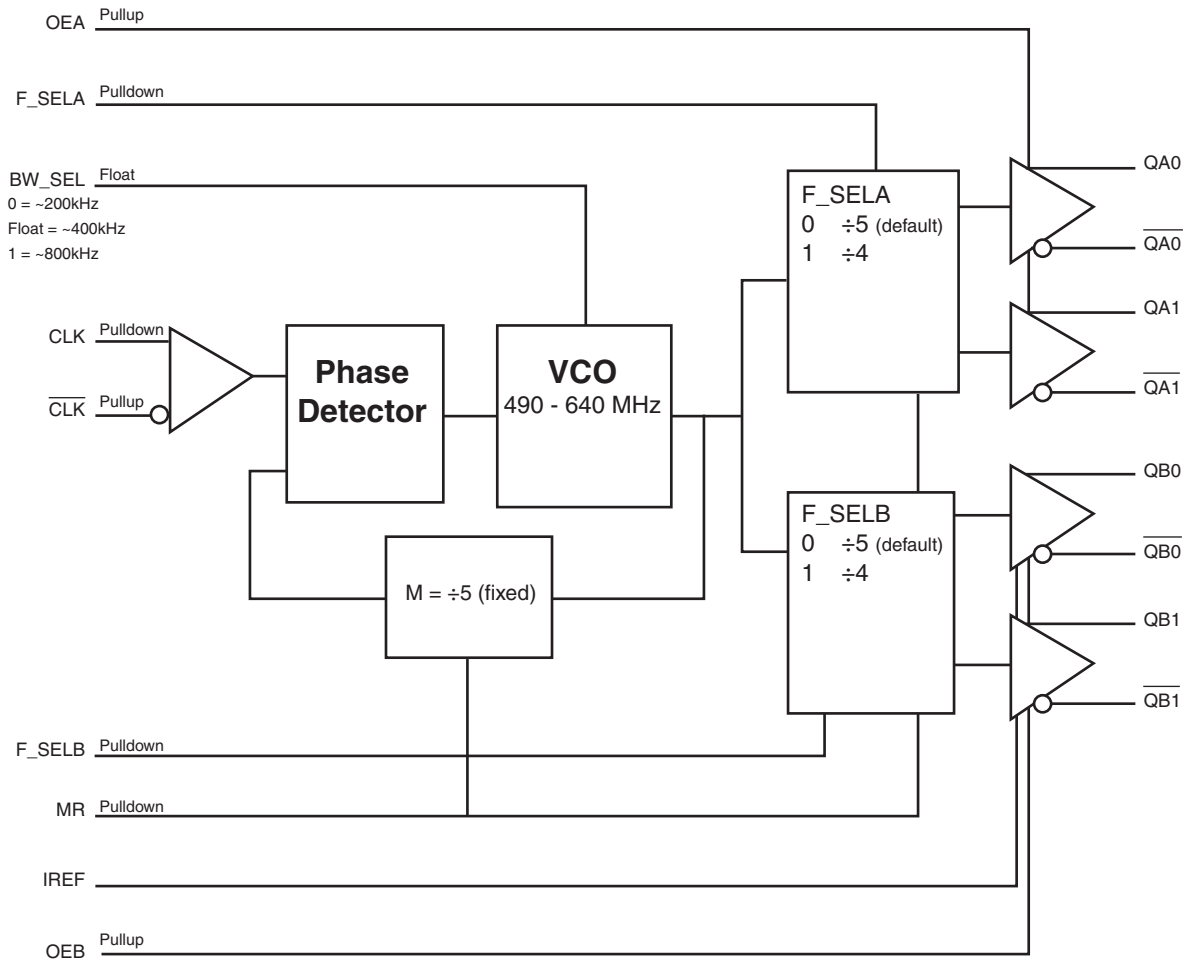


Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|--------|------------------------|--------|---------------------|---|
| 1, 24 | $\overline{QA1}$, QA1 | Output | | Differential output pair. LVDS interface levels. |
| 3, 22 | V _{DDO} | Power | | Output supply pins. |
| 4, 5 | QA0, $\overline{QA0}$ | Output | | Differential output pair. LVDS interface levels. |
| 6 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q[Ax:Bx] to go LOW and the inverted outputs $\overline{Q[Ax:Bx]}$ to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 7 | BW_SEL | Input | Pullup/ Pulldown | PLL Bandwidth input. LVCMOS/LVTTL interface levels. See Table 3B. |
| 8 | nc | Unused | | No connect. |
| 9 | V _{DDA} | Power | | Analog supply pin. |
| 10 | F_SELA | Input | Pulldown | Frequency select pins for QAx/ \overline{QAx} outputs. LVCMOS/LVTTL interface levels. See Table 3C. |
| 11 | V _{DD} | Power | | Core supply pin. |
| 12 | OEA | Input | Pullup | Output enable for QAx pins. When HIGH, QAx/ \overline{QAx} outputs are enabled. When LOW, the QAx/ \overline{QAx} outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A. |
| 13 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 14 | \overline{CLK} | Input | Pullup | Inverting differential clock input. |
| 15, 16 | GND | Power | | Power supply ground. |
| 17 | OEB | Input | Pullup | Output enable for QBx pins. When HIGH, QBx/ \overline{QBx} outputs are enabled. When LOW, the QBx/ \overline{QBx} outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A. |
| 18 | F_SELB | Input | Pulldown | Frequency select pins for QBx/ \overline{QBx} outputs. LVCMOS/LVTTL interface levels. See Table 3C. |
| 19 | IREF | Input | | A fixed precision resistor (RREF = 475Ω) from this pin to ground provides a reference current used for differential current-mode QB0/nQB0 clock outputs. |
| 20, 21 | $\overline{QB0}$, QB0 | Output | | Differential output pair. HCSL interface levels. |
| 23, 24 | QB1, $\overline{QB1}$ | Output | | Differential output pair. HCSL interface levels. |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Function Tables

Table 3A. Output Enable Function Table

| Inputs | | Outputs | |
|--------|-----|-----------------|-----------------|
| OEA | OEB | QA[0:1]/QA[0:1] | QB[0:1]/QB[0:1] |
| 0 | 0 | Hi-Z | Hi-Z |
| 1 | 1 | Enabled | Enabled |

Table 3B. PLL Bandwidth Function Table

| Input | PLL Bandwidth |
|--------|-------------------|
| BW_SEL | |
| 0 | ~200kHz |
| Float | ~600kHz (default) |
| 1 | ~2MHz |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 82.3°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|-----------------|---------|----------|-------|
| V_{DD} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.12$ | 3.3 | V_{DD} | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | | 45 | mA |
| I_{DDA} | Analog Supply Current | | | | 12 | mA |
| I_{DDO} | Output Supply Current | | | | 80 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---------------------------------|--------------------------------|---------|------------------|---------|
| V_{IH} | Input High Voltage | OEA, OEB, MR, F_SELA, F_SELB | 2 | | $V_{DD} + 0.3$ | V |
| | | BW_SEL | $V_{DD} - 0.3$ | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | OEA, OEB, MR, F_SELA, F_SELB | -0.3 | | 0.8 | V |
| | | BW_SEL | -0.3 | | +0.3 | V |
| V_{IM} | Input Mid Voltage | BW_SEL | $V_{DD}/2 - 0.1$ | | $V_{DD}/2 + 0.1$ | V |
| I_{IH} | Input High Current | F_SELA, F_SELB, MR, BW_SEL | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | OEA, OEB | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | MR, F_SELA, F_SELB, | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| | | OEA, OEB, BW_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------------|------------------|-------------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | \overline{CLK} | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK | $V_{DD} = 3.465V,$ $V_{IN} = 0V$ | -5 | | μA |
| | | \overline{CLK} | $V_{DD} = 3.465V,$ $V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1 | | GND + 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: Common mode input voltage is defined as V_{IH} .Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 290 | 390 | 490 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.2 | 1.35 | 1.5 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

AC Electrical Characteristics

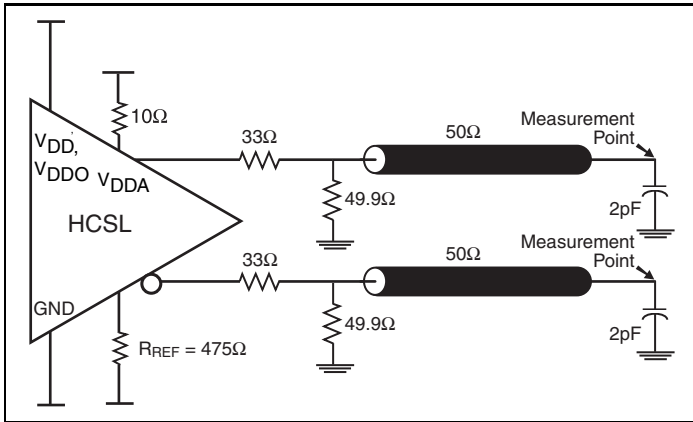
Table 5. 0.7V Differential AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Parameter | Symbol | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------------|---|-----------------------|-----------------------------------|---------|-------------------|-------|
| f_{MAX} | Output Frequency | | 98 | | 160 | MHz |
| $f_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 1 | | | | 35 | ps |
| $t_{sk(b)}$ | Bank Skew; NOTE 2 | | | | 30 | ps |
| V_{HIGH} | Output Voltage High | QBx/ \overline{QBx} | 530 | | 870 | ps |
| V_{LOW} | Output Voltage Low | QBx/ \overline{QBx} | -150 | | | ps |
| V_{OVS} | Max. Voltage, Overshoot | QBx/ \overline{QBx} | | | $V_{HIGH} + 0.35$ | V |
| V_{UDS} | Min. Voltage, Undershoot | QBx/ \overline{QBx} | -0.3 | | | V |
| V_{rb} | Ringback Voltage | QBx/ \overline{QBx} | | | 0.2 | V |
| V_{CROSS} | Absolute Crossing Voltage | QBx/ \overline{QBx} | @ 0.7V Swing | 250 | 550 | mV |
| ΔV_{CROSS} | Total Variation of V_{CROSS} over all edges | QBx/ \overline{QBx} | @ 0.7V Swing | | 140 | mV |
| t_R / t_F | Output Rise/Fall Time | QBx/ \overline{QBx} | measured between 0.175V to 0.525V | 175 | 700 | ps |
| | | QAx/ \overline{QAx} | 20% to 80% | 250 | 600 | ps |
| $\Delta t_R / \Delta t_F$ | Rise/Fall Time Variation | QBx/ \overline{QBx} | | | 125 | ps |
| t_{RFM} | Rise/Fall Matching | QBx/ \overline{QBx} | | | 20 | % |
| odc | Output Duty Cycle | | 48 | | 52 | % |

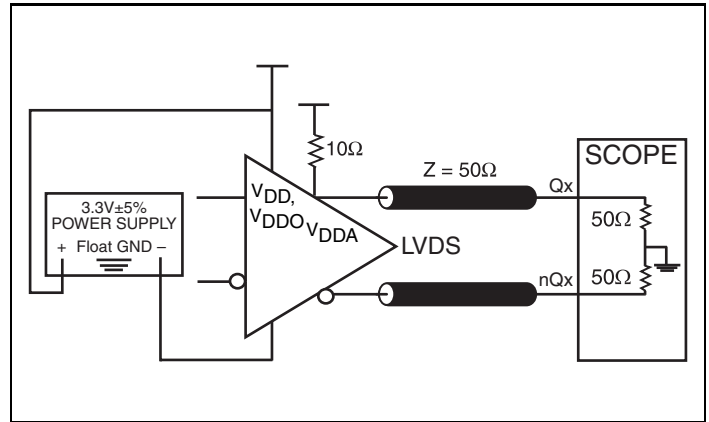
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

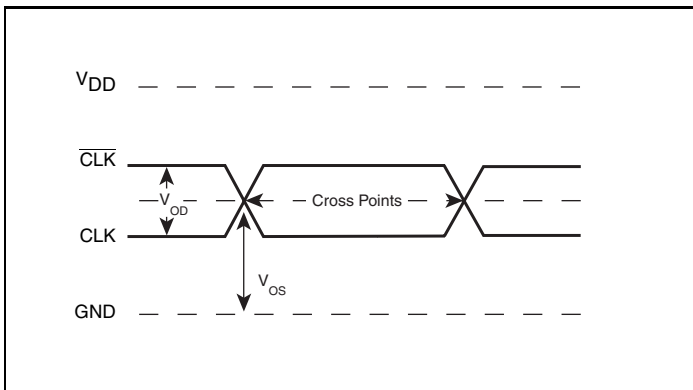
Parameter Measurement Information



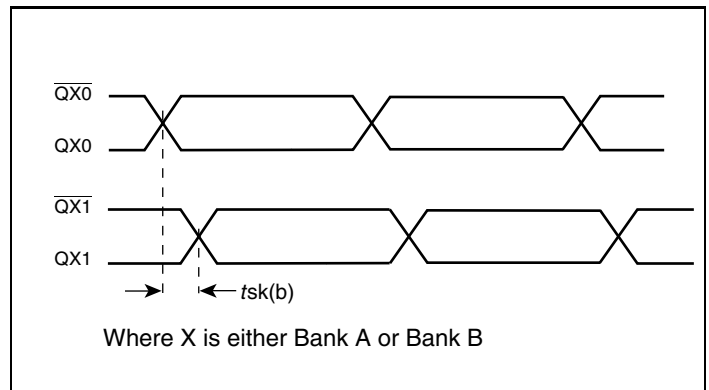
3.3V HCSL Output Load AC Test Circuit



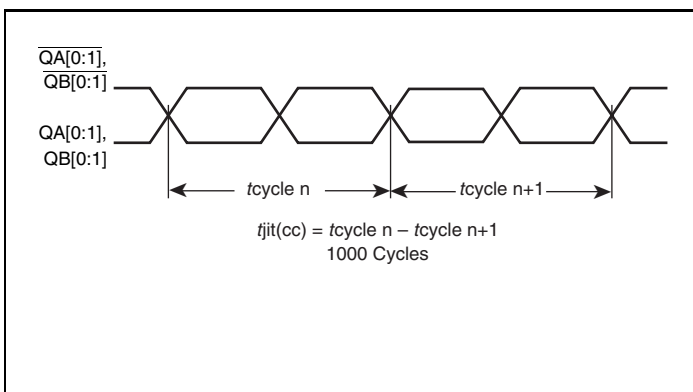
3.3V LVDS Output Load AC Test Circuit



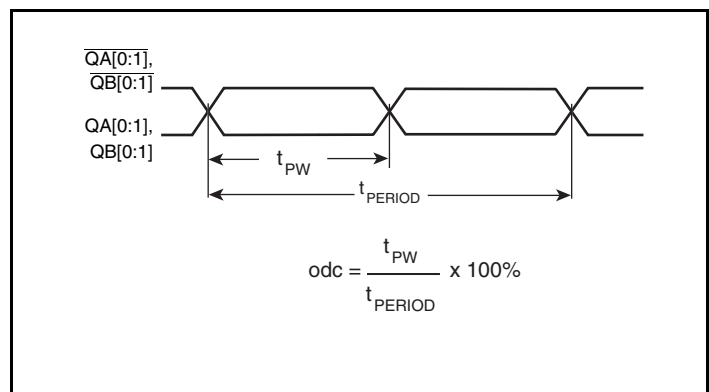
Differential Input Level



Bank Skew

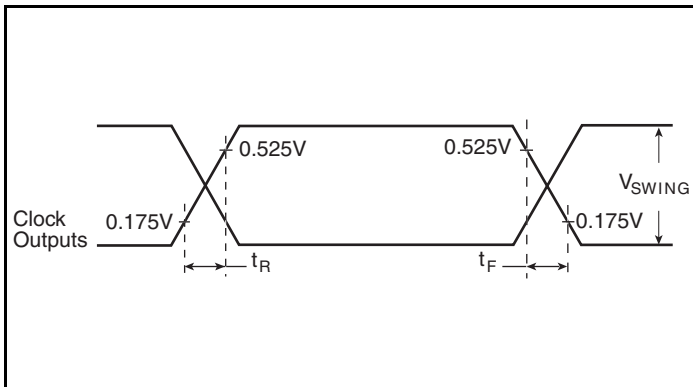


Cycle-to-Cycle Jitter

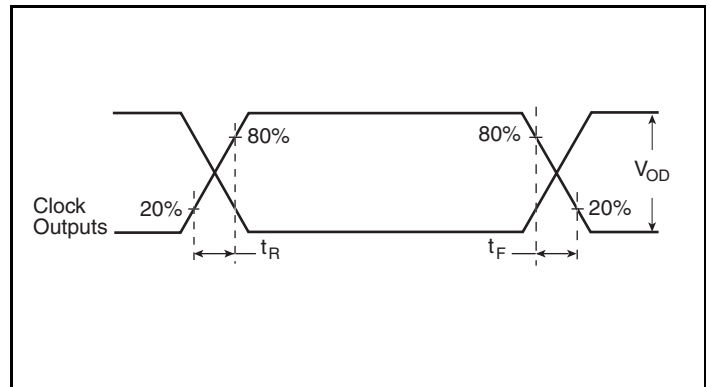


Output Duty Cycle/Pulse Width/Period

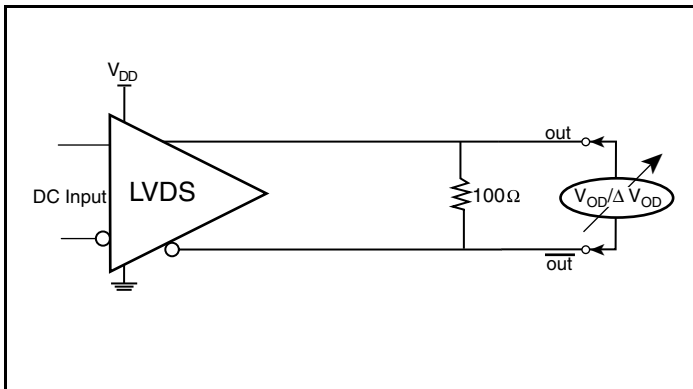
Parameter Measurement Information, continued



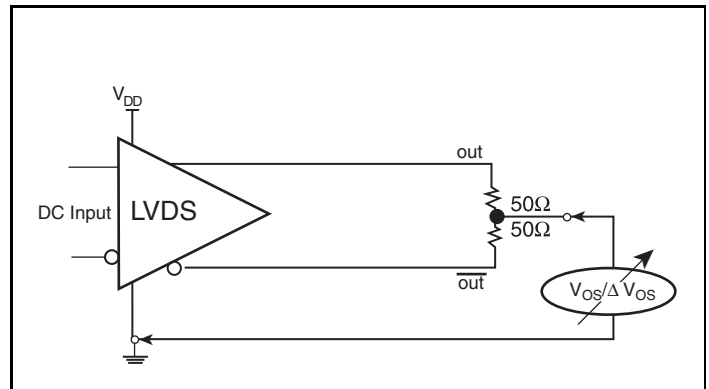
HCSL Output Rise/Fall Time



LVDS Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8741004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $0.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} pin.

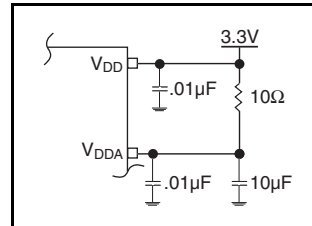


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio of

$R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3\text{V}$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

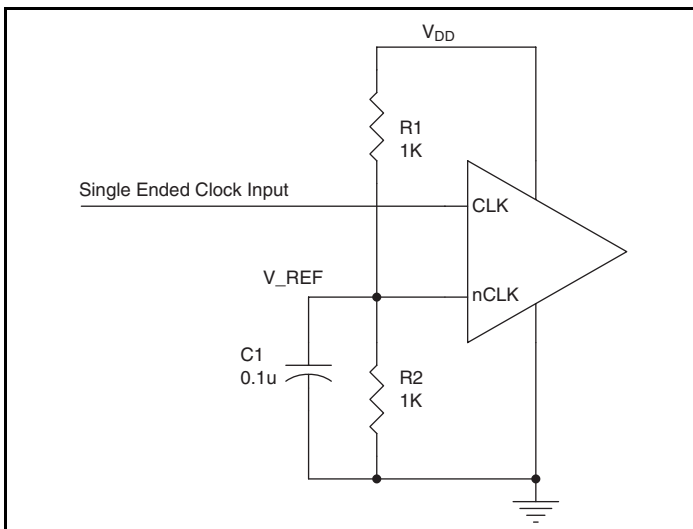


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK/ $\overline{\text{CLK}}$ accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/ $\overline{\text{CLK}}$ input driven by the most common driver types. The input interfaces suggested here are

examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

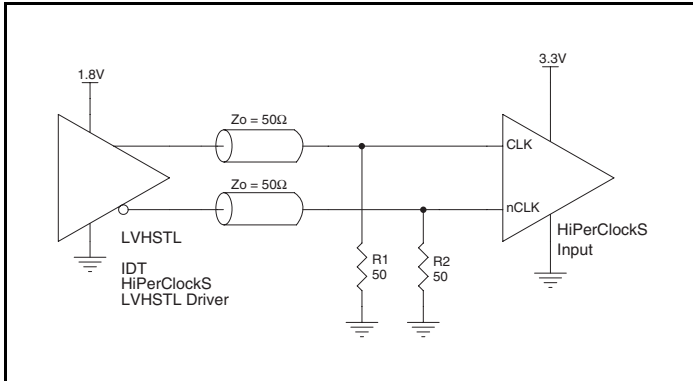


Figure 3A. HiPerClockS CLK/ $\overline{\text{CLK}}$ Input Driven by an IDT HiPerClockS LVHSTL Driver

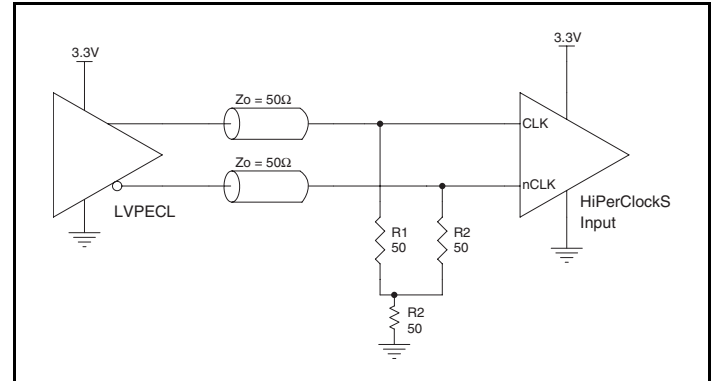


Figure 3B. HiPerClockS CLK/ $\overline{\text{CLK}}$ Input Driven by a 3.3V LVPECL Driver

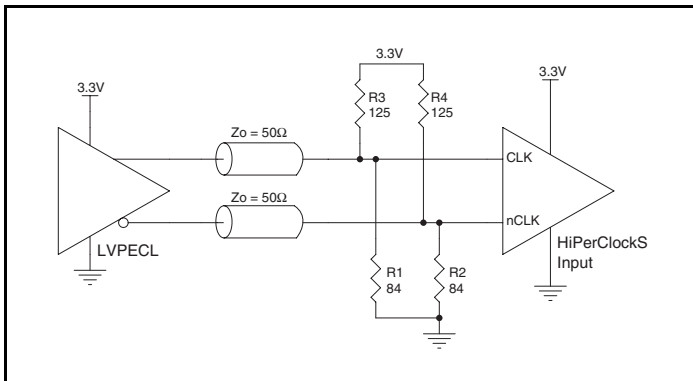


Figure 3C. HiPerClockS CLK/ $\overline{\text{CLK}}$ Input Driven by a 3.3V LVPECL Driver

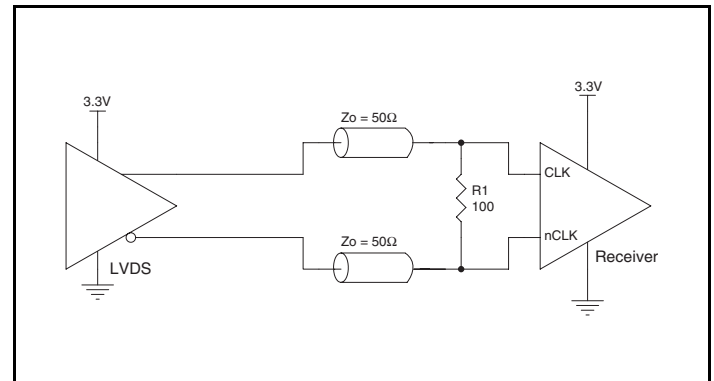


Figure 3D. HiPerClockS CLK/ $\overline{\text{CLK}}$ Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100 Ω differential transmission line environment, LVDS drivers require a matched load termination of 100 Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

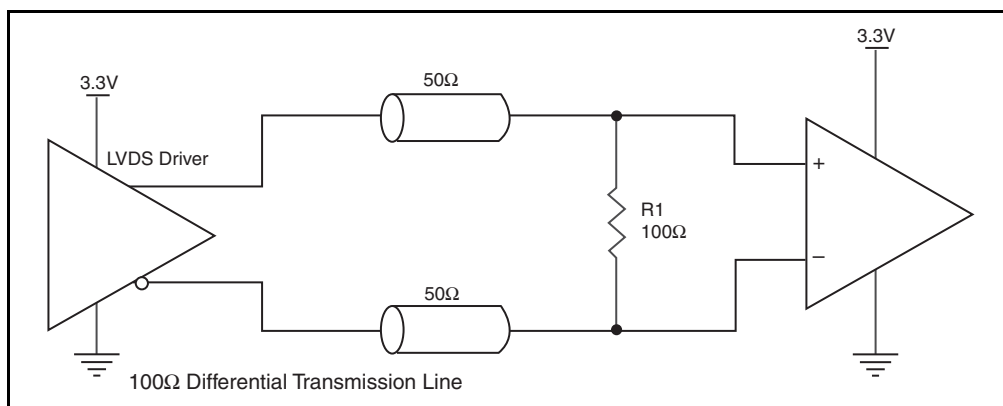


Figure 4. Typical LVDS Driver Termination

Recommended Termination

Figure 5A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

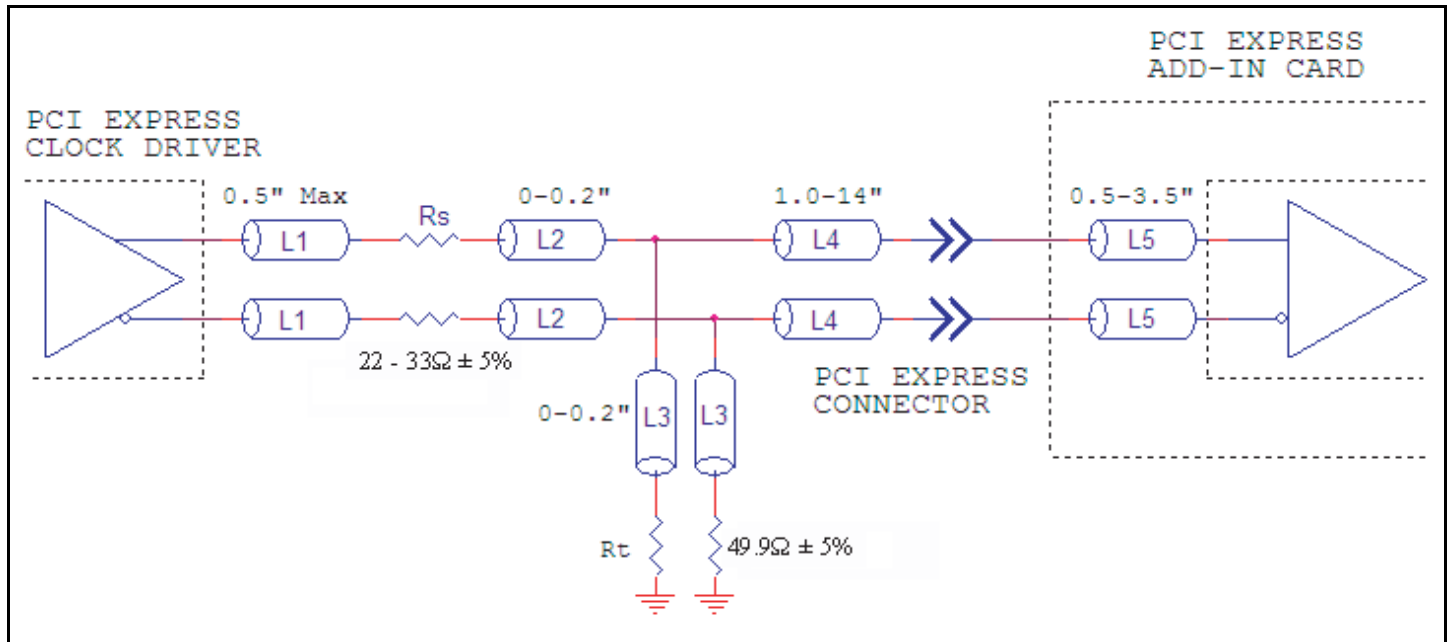


Figure 5A. Recommended Termination

Figure 5B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

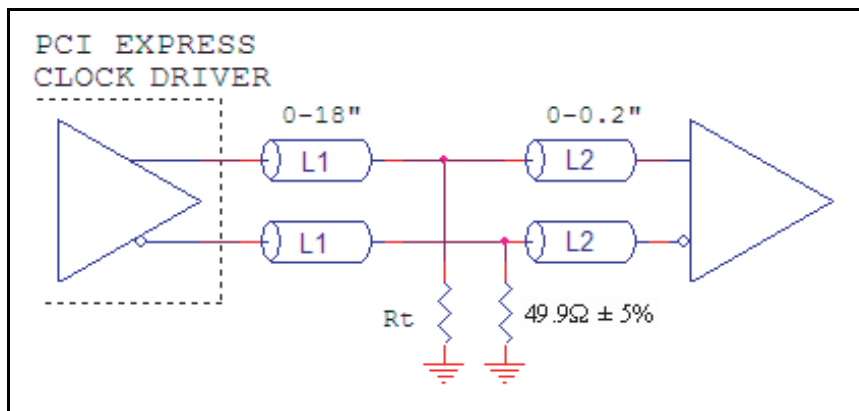


Figure 5B. Recommended Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8741004. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS741004 is the sum of the core power plus the **analog power** plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (45mA + 12mA) = \mathbf{197.5mW}$
- Power (LVDS_output)_{MAX} = $V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 80mA = \mathbf{227.2mW}$
- Power (HCSL_output)_{MAX} = $45.65mW * 2 = \mathbf{91.3mW}$

Total Power_{MAX} = (3.465V, with all outputs switching) = $197.5mW + 277.2mW + 91.3mW = \mathbf{556mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.556\text{W} * 82.3^\circ\text{C}/\text{W} = 115.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

| θ_{JA} Vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 82.3°C/W | 78.0°C/W | 75.9°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6*.

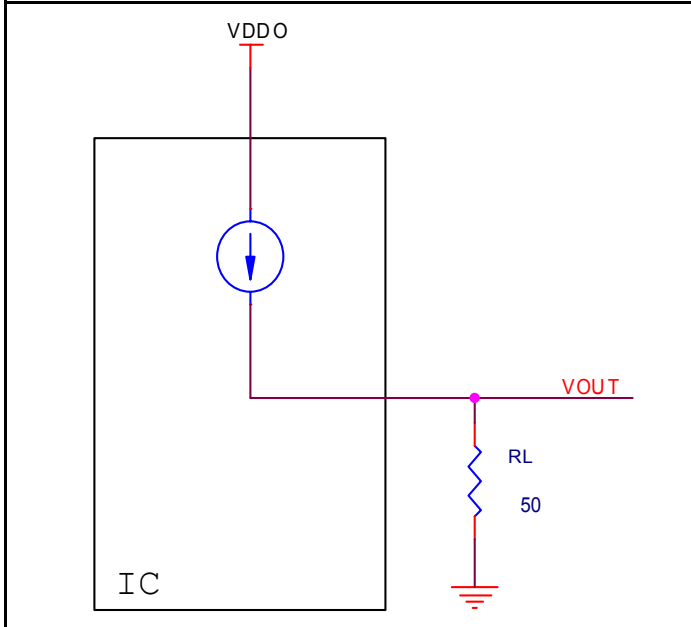


Figure 6. LVHSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load and a termination voltage of $V_{CCO} - 2V$.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MAX} / R_L) * (V_{DD_MAX} - V_{OH_MAX})$$

$$Pd_L = (V_{OL_MIN} / R_L) * (V_{DD_MAX} - V_{OL_MIN})$$

$$Pd_H = (0.85V / 50\Omega) * (3.465V - 0.87V) = \mathbf{44.1mW}$$

$$Pd_L = (0.15V / 50\Omega) * 0.15V = \mathbf{0.45mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{45mW}$$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 82.3°C/W | 78.0°C/W | 75.9°C/W |

Transistor Count

The transistor count for ICS8741004 is: 1318

Package Outline and Package Dimension

Package Outline - G Suffix for 24 Lead TSSOP

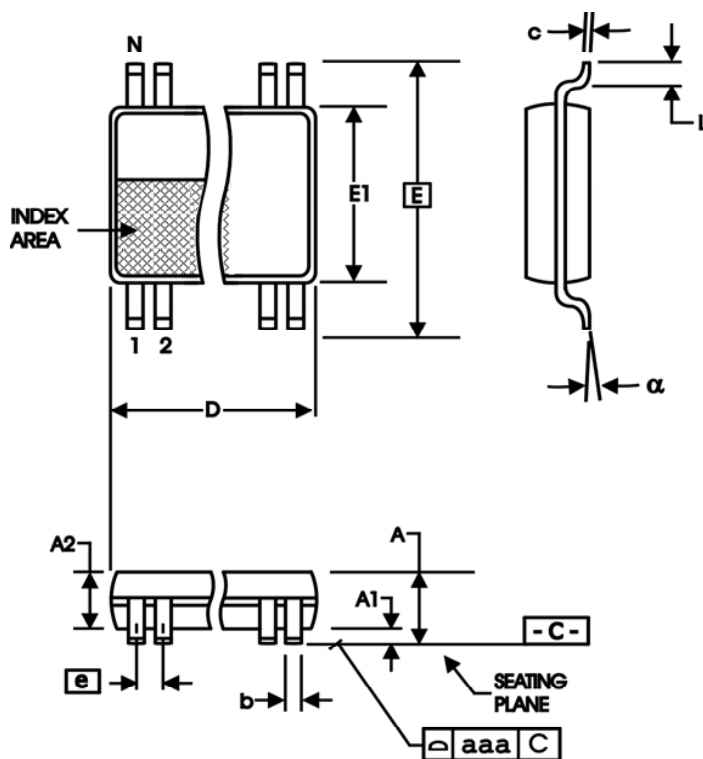


Table 8. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 24 | |
| A | | 1.20 |
| A1 | 0.5 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 7.70 | 7.90 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------------|---------------------------|--------------------|-------------|
| 8741004AG | ICS8741004AG | 24 Lead TSSOP | Tray | 0°C to 70°C |
| 8741004AGT | ICS8741004AG | 24 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |
| 8741004AGLF | ICS8741004AGLF | "Lead-Free" 24 Lead TSSOP | Tray | 0°C to 70°C |
| 8741004AGLFT | ICS8741004AGLF | "Lead-Free" 24 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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