



# LOW SKEW, 1-TO-10 HSTL FANOUT BUFFER

ICS83210

## GENERAL DESCRIPTION

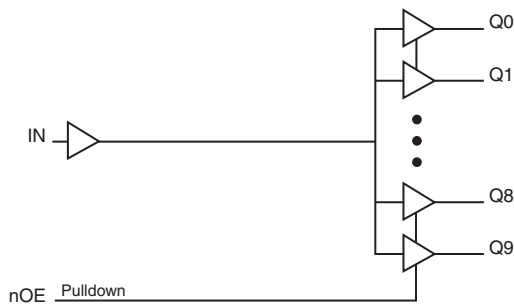


The ICS83210 is a low skew, 1-to-10 HSTL Fanout Buffer and a member of the HiPerClockS™ Family of High Performance Clock Solutions from IDT. The class II HSTL outputs are balanced push-pull in design, capable of delivering 16mA into a 10pF load. This class allows both source series termination and symmetrically double parallel termination.

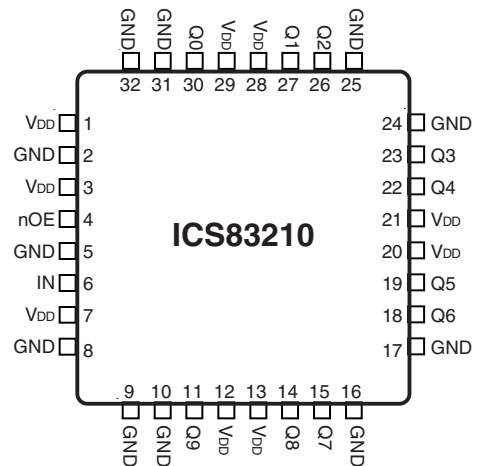
## FEATURES

- Ten single-ended HSTL outputs
- One single-ended HSTL clock input
- Maximum input frequency: 150MHz
- Output skew: 110ps (maximum)
- Part-to-part skew: 2ns (maximum)
- 1.5V power supply
- 0°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**32-Lead TQFP**  
 7mm x 7mm x 1.0mm package body  
**Y package**  
 Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 7, 12, 13, 20, 21, 28, 29	V <sub>DD</sub>	Power		Power supply pins.
2, 5, 8, 9, 10, 16, 17, 24, 25, 31, 32	GND	Power		Power supply ground.
4	nOE	Input	Pulldown	Output enable/disable input pin. When LOW, outputs Qx outputs are enabled. When HIGH, Qx outputs are disabled low. LVCMOS/LVTTL interface levels.
5	IN	Input		Single-ended reference clock input. HSTL interface levels.
11, 14, 15, 18, 19, 22, 23, 26, 27, 30	Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended HSTL clock outputs.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
C <sub>OUT</sub>	Output Pin Capacitance			4.5	6	pF
R <sub>OUT</sub>	Output Impedance			20		Ω

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	75.5°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 1.5V \pm 8\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		1.38	1.5	1.62	V
$I_{DD}$	Power Supply Current	Outputs Loaded @ 62.5MHz		215	250	mA
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = 0V$ , outputs disabled			1	mA

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 1.5V \pm 8\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	nOE	$0.7 \cdot V_{DD}$		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	nOE	-0.3		$0.3 \cdot V_{DD}$	V
$I_{IH}$	Input High Current	nOE			150	$\mu A$
$I_{IL}$	Input Low Current	nOE	-5			$\mu A$

TABLE 3C. HSTL DC CHARACTERISTICS,  $V_{DD} = 1.5V \pm 8\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	IN	0.85		1.8	V
$V_{IL}$	Input Low Voltage	IN				
$V_{OH}$	Output High Voltage; NOTE 1	$I_{OH} = -16mA$	1.0		$V_{DD} + 0.3$	V
$V_{OL}$	Output Low Voltage; NOTE 1	$I_{OL} = 16mA$	-0.3		0.4	V

NOTE 1: Outputs terminated with 50 $\Omega$  to ground.

TABLE 4. AC CHARACTERISTICS,  $V_{DD} = 1.5V \pm 8\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency				150	MHz
$t_{PLH}$	Propagation Delay, Low-to-High; NOTE 1		1.0		5.5	ns
$t_{PHL}$	Propagation Delay, High-to-Low NOTE 1		1.0		5.5	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				110	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				2	ns
$t_{EN}$	Output Enable Time				7	ns
$t_{DIS}$	Output Disable Time				7	ns
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	250		1.3	ns
odc	Output Duty Cycle	$F_{out} \leq 100MHz$	48		52	%
		$F_{out} > 100MHz$	45		55	%

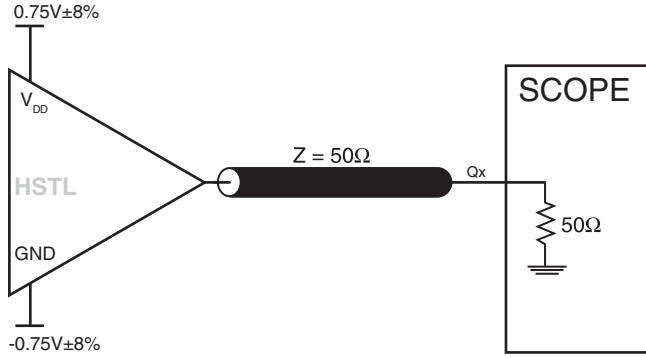
NOTE 1: Measured from the  $V_{DD}/2$  of the input to  $V_{DD}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

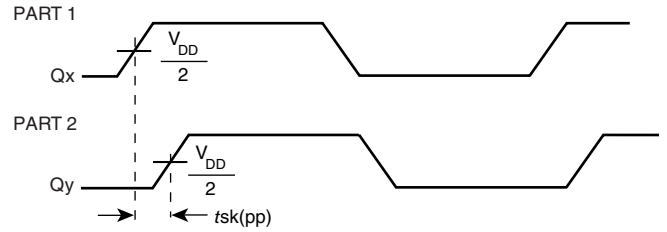
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

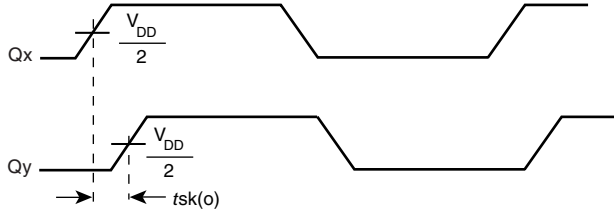
## PARAMETER MEASUREMENT INFORMATION



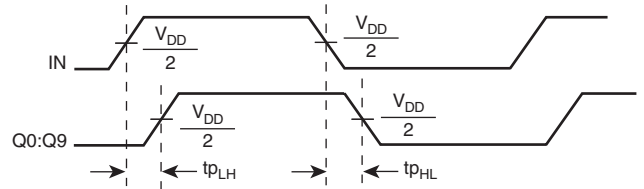
1.5V OUTPUT LOAD AC TEST CIRCUIT



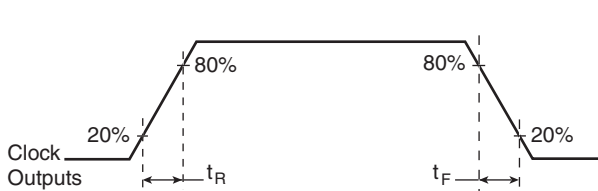
PART-TO-PART SKEW



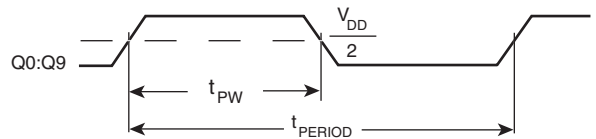
OUTPUT SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED OUTPUT PINS

#### OUTPUTS:

##### HSTL OUTPUTS

All unused HSTL outputs can be left floating. We recommend that there is no trace attached.

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## RELIABILITY INFORMATION

TABLE 5.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD TQFP

	$\theta_{JA}$ by Velocity (Meters per Second)		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	75.5°C/W	65.8°C/W	62.2°C/W

#### TRANSISTOR COUNT

The transistor count for ICS83210 is: 218

Pin compatible with CY2HH8110

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD TQFP

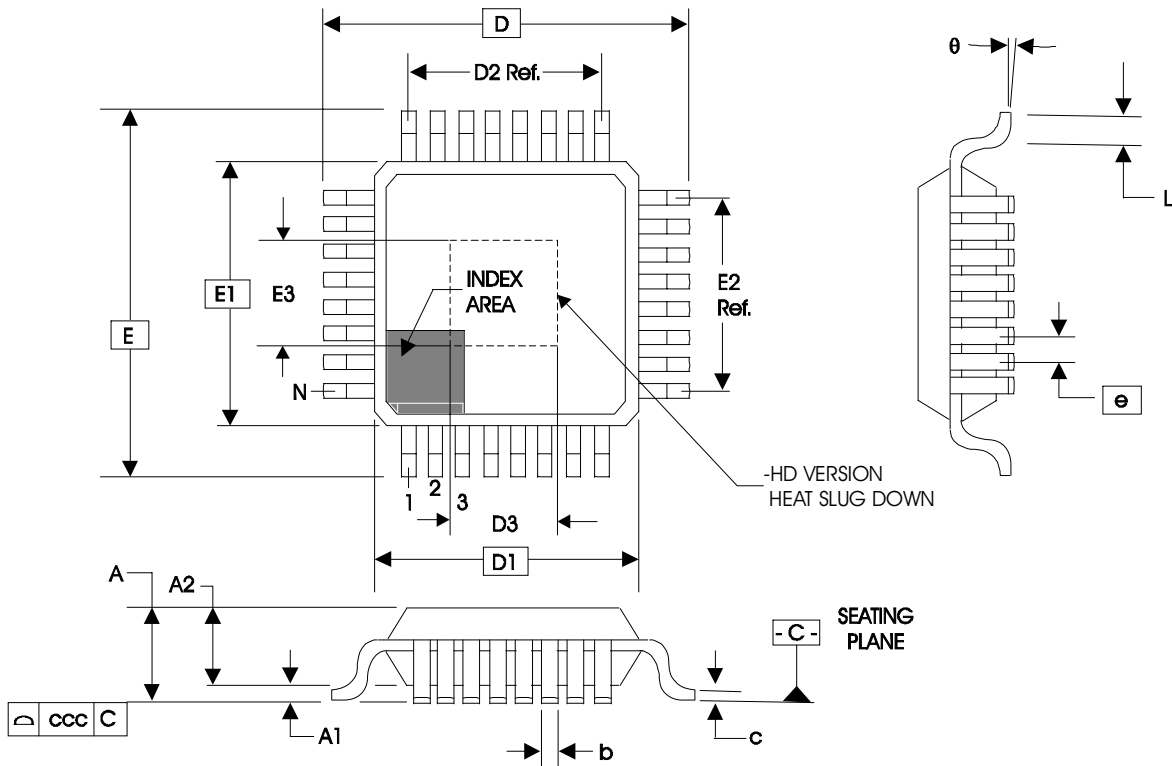


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83210AY	ICS83210AY	32 lead TQFP	tray	0°C to 85°C
ICS83210AYT	ICS83210AY	32 lead TQFP	1000 tape & reel	0°C to 85°C
ICS83210AYLF	ICS83210AYLF	32 lead "Lead-Free" TQFP	tray	0°C to 85°C
ICS83210AYLFT	ICS83210AYLF	32 lead "Lead-Free" TQFP	1000 tape & reel	0°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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