

AsahiKASEI
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AKD4628A-B
AK4628A Evaluation Board Rev.1

GENERAL DESCRIPTION

The AKD4628A-B is an evaluation board for the AK4628A, a single chip CODEC that includes two channels of ADC and eight channels of DAC. The AKD4628A-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector or BNC connector.

■ Ordering guide

AKD4628A-B --- AK4628A Evaluation Board
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this.) This control software can't operate on Windows NT.

FUNCTION

- On-board analog input buffer circuit
- Compatible with 2 types of interface
 - DIT (AK4103A)/DIR (AK4112B) with optical output/input and BNC input
 - Direct interface with AC3 decoder by 10pin header
- 10pin header for serial control interface

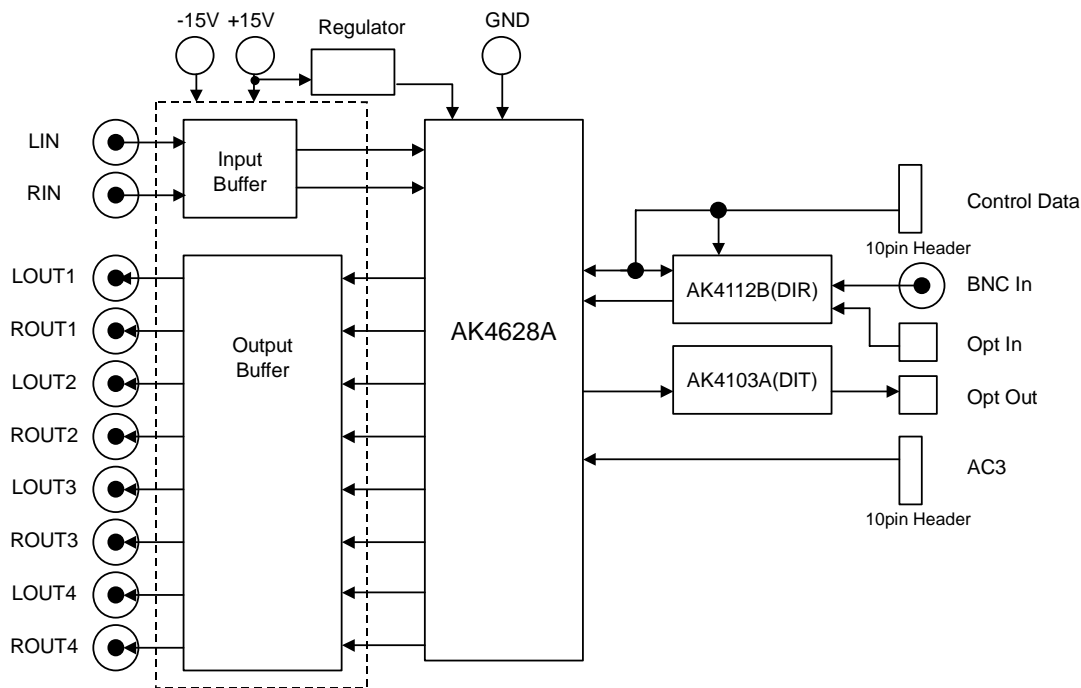


Fig 1. AKD4628A-B Block Diagram

*Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

(1) Set up the power supply lines.

| | | |
|--------|---------------|--------------|
| [+12V] | (Orange jack) | = +12 ~ +15V |
| [-12V] | (Blue jack) | = -12 ~ -15V |
| [AGND] | (Black jack) | = 0V |
| [DGND] | (Black jack) | = 0V |

Each supply line should be distributed from the power supply unit.

±12V are supplied to analog interface.

+12V is regulated to +5V and +3.3V by regulators (T1, T2).

+5V is supplied to digital interface, AK4628A and TVDD of AK4112B.

+3.3V is supplied to AVDD and DVDD of AK4112B and TVDD of AK4628A.

(2) Set up the evaluation mode and jumper pins. (See p.6.)

(3) Power on.

The AK4628A, AK4112B and AK4103A should be reset once bringing PDN (SW1) “L” upon power-up.

(4) Set up software.

The control mode of AK4628A and AK4112B is fixed to “serial”.

The AKD4628A-B can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (uP-I/F) with PC by 10-line flat cable packed with the AKD4628A-B.

Take care of the direction of connector. There is a mark at pin#1.

The pin layout of PORT1 is as Figure 2.

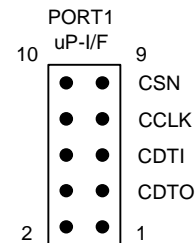


Figure 2. PORT1 pin layout

■ Evaluation mode

1) Evaluation of ADC

TOTX176 is used for digital output. Clock mode of the AK4112B should be set to PLL mode or X'tal mode.

2) Evaluation of DAC

TORX176 or BNC is used for digital input. Clock mode of the AK4112B should be set to PLL mode. "4112B" should be selected on JP4, 5, 6 and 7.

3) Loop back mode

Clock mode of the AK4112B should be set to PLL mode or X'tal mode. "4112B" should be selected on JP4,5,6 and 7.

4) Evaluation of DAC using DSP

"DSP" should be selected on JP4, 5, 6 and 7.

| Evaluation mode | AK4112B clock set-up | JP4, 5, 6, 7 | Used I/F |
|-----------------|---|--------------|---------------------------|
| ADC | CM1="0", CM0="0"(PLL mode) or CM1="0", CM0="1"(X'tal mode) | Don't care | TOTX176 optical output |
| DAC | CM1="0", CM0="0"(PLL mode) | "4112B" | |
| Loop back | CM1="0", CM0="1"(X'tal mode) | "4112B" | |
| Using DSP | CM1="0", CM0="0"(PLL mode) | "DSP" | PORT5 (10-pin Header) |

(Note.) 1. Software "akd4628a-b-ak4112b.exe" packed with the AKD4628A-B is used for set-up of the AK4112B.

2. CM1 and CM0 bits are D5 and D4 of Addr=00H, respectively

Table 2.Evaluation mode

■ DIP Switch set up. (See the datasheet of AK4628A and AK4103A)

1.DFS_4628A (SW2-1) set up of AK4628A Sampling speed (fs).

| DFS_4628A | Sampling Speed (fs) | | Default |
|-----------|---------------------|-------------|---------|
| OFF | Normal Speed Mode | 32kHz~48kHz | |
| ON | Double Speed Mode | 64kHz~96kHz | |

Table 3. Set up of Sampling Speed (fs)

2.V (SW2-2) set up of AK4103A Validity detect.

| V | Validity | Default |
|-----|----------|---------|
| OFF | Valid | |
| ON | Invalid | |

Table 4. Set up of Validity

3.FS3 (SW2-3), FS2 (SW2-4) set up of AK4103A Sampling frequency setting.

| FS3 | FS2 | Sampling frequency setting | Default |
|-----|-----|----------------------------|---------|
| OFF | OFF | 44.1kHz | |
| OFF | ON | 48kHz | |
| ON | OFF | Reserved | |
| ON | ON | 32kHz | |

Table 5. Set up of sampling frequency setting

4.CKS0 (SW2-5) set up of AK4103A System Clock.

| CKS1 | MCLK | fs | Default |
|------|-------|------------|---------|
| OFF | 256fs | 28k-108kHz | |
| ON | 512fs | 28k-54kz | |

Table 6.Set up of System Clock

5.DIF0 (SW2-6) set up of AK4103A Audio Serial Interface Format.

| DIF0 | Audio Serial Interface Format | LRCK | BICK | |
|------|-------------------------------|------|------------|---------|
| OFF | 24bit, Left justified | H/L | 48fs-128fs | Default |
| ON | 24bit, I ² S | L/H | 48fs-128fs | |

Table 7. Set up of Audio Serial Interface Format

■ Jumper pin set up

[JP1] (GND) --- Analog GND and Digital GND

[JP4, 5, 6, 7]

(SDTI1, 2, 3, 4) --- AK4628A SDTI1, 2, 3, 4 input source select

<DSP> : Serial Data is input from DSP via PORT4.

<4112A> : Serial Data is input from AK4112B SDTO. <default>

[JP3] (V/TX) --- AK4112B V/TX output select.

<V> : Validity. <default>

<TX> : Transmit channel (through data)

[JP2](OPT/COAX) --- The source of the biphasic signal input to the AK4112B

<OPT_IN> : Optical input to RX1 of AK4112B <default>

<RX2> : BNC input to RX1 of AK4112B

■ The function of the toggle SW.

[SW1]: Resets the AK4628A, AK4112B and AK4103A. Keep “H” during normal operation.

■ The indication content for LED.

[LE1] (DZF1) : Zero detection

[LE2] (DZF2_OVF) : Zero detection or Overflow Detection

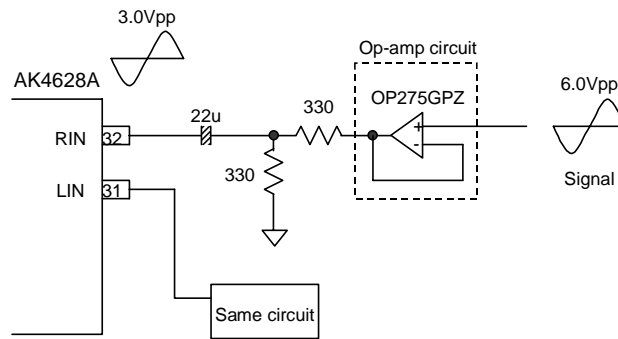
[LE3] (ERF) : AK4112B unlock and parity error output.

[LE4] (FS96) : AK4112B 96kHz sampling detect.

[LE5] (AUTO) : AK4112B AC-3/MPEG detect.

[LE6] (V) : AK4112B Validity detect

■ Analog input circuit



1) Gain

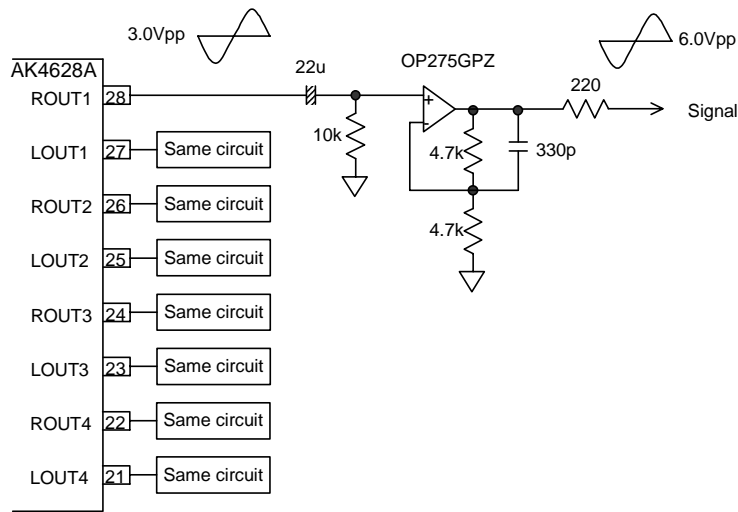
Gain of analog input circuit is

$$330 / (330 + 330) = -6.02 \text{dB}$$

Therefore input level for this board is

$$\begin{aligned} &+0.51 \text{dBV} (= 3.0 \text{Vpp}) + 6.02 \text{dB} \\ &= +6.53 \text{dBV} = 6.00 \text{Vpp} = 2.12 \text{Vrms} \end{aligned}$$

■ Analog output circuit



1st order LPF on this board

1) Frequency response of HPF

The HPF is implemented on board to cancel the DC offset of analog output of AK4628A.

Frequency response of 1st-order HPF

$$|\text{Amplitude}|^2 = 1 / \{1 + (fc/f)^2\}; fc = 1/2\pi RC = \mathbf{0.7Hz} @ R=10k, C=22u$$

| | |
|--------------------|-----------------|
| fin | 20Hz |
| Frequency Response | -0.006dB |

2) Gain, S/N and frequency response of op-amp circuit

1st-order filter with non-inverting amp is implemented on board to double the analog output level and attenuate out-of-band noise.

a) Gain

The gain is

$$1 + 4.7k/4.7k = +6.02dB.$$

Therefore the output level of this board is

$$\begin{aligned} &0.51dBV (=3.0Vpp) + 6.02dB \\ &= \mathbf{6.53dBV = 6.00Vpp = 2.12Vrms.} \end{aligned}$$

c) Frequency response of filter

Frequency response of the 1st-order filter

$$| \text{Amplitude} |^2 = K * \{ 1 + (f/fc_2)^2 \} / \{ 1 + (f/fc_1)^2 \};$$

$$K = 1 + 4.7k/4.7k = 2,$$

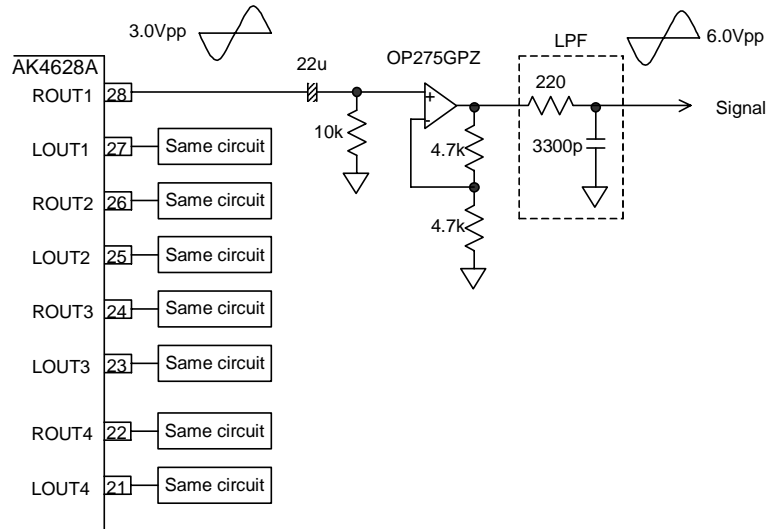
$$fc_1 = 1/2\pi RC = 102.7kHz @ R=4.7k, C=330p,$$

$$fc_2 = K * fc_1 = 205.3kHz$$

Frequency response referenced to output level of this board is as following table:

| fin | DC | 20kHz | 40kHz | 80kHz | 145kHz | ∞ |
|--------------------|-----|-----------------|-----------------|-----------------|--------|------|
| Frequency Response | 0dB | -0.121dB | -0.452dB | -1.448dB | -3dB | -6dB |

If the frequency response of filter influences the system, 1st-order LPF is also available as the following figure:



Example of LPF with flat response.

Frequency response of this LPF

$$| \text{Amplitude} |^2 = 1 / \{ 1 + (f/fc)^2 \};$$

$$fc = 1/2\pi RC = 219kHz @ R=220, C=3300p$$

Frequency response referenced to output level of this board is as following table:

| fin | DC | 20kHz | 40kHz | 80kHz | 219kHz | ∞ |
|--------------------|-----|-----------------|-----------------|-----------------|--------|------|
| Frequency Response | 0dB | -0.036dB | -0.142dB | -0.543dB | -3dB | -∞dB |

The total frequency response of this board is sum of the external filter and internal LPF of AK4628A.

These filters are effective to attenuate the high frequency noise since some measurement units is sensitive for out-of-band noise.

CONTROL SOFTWARE MANUAL

■ Set-up of evaluation board and control software

1. Set up the AKD4628A-B according to previous term.
2. Connect IBM-AT compatible PC with AKD4628A-B by 10-line type flat cable (packed with AKD4628A-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)
3. Insert the CD-ROM labeled "AKD4628A-B Evaluation Kit" into the CD-ROM drive.
4. Access the CD-ROM drive and double-click the icon of the control files as following to set up the control program.
 "akd4628a-b-ak4628a.exe" – AK4628A control program
 "akd4628a-b-ak4112b.exe" – AK4112B control program
5. Then please evaluate according to the follows.

(Note) This board is used AK4112B as "DIR". This software must set up when Evaluation of DAC using DSP and Clock Mode selected X'tal.(See P3. (4)).

This evaluation board and the control software packed with this do not correspond to I²C control.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

- | | |
|---------------------|---|
| 1. [Port Reset]: | Set up the USB interface board (AKDUSBIF-A) when using the board. |
| 2. [Write default]: | Initialize the register of the AK4628A, AK4112B. |
| 3. [All Write]: | Write all registers that are currently displayed. |
| 4. [Function1]: | Dialog to write data by keyboard operation. |
| 5. [Function2]: | Dialog to write data by keyboard operation. |
| 6. [Function3]: | The sequence of register setting can be set and executed. |
| 7. [Function4]: | The sequence that is created on [Function3] can be assigned to buttons and executed. |
| 8. [Function5]: | The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. |
| 9. [SAVE]: | Save the current register setting. |
| 10. [OPEN]: | Write the saved values to all register. |
| 11. [Write]: | Dialog to write data by mouse operation. |

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "L". If not, "0" or "1".

If you want to write the input data to the AK4628A, AK4112B, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.

Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4628A, AK4112B, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate DATT

There are dialogs corresponding to register of 03h and 04h.

Address Box: Input registers address in 2 figures of hexadecimal.

Start Data Box: Input starts data in 2 figures of hexadecimal.

End Data Box: Input end data in 2 figures of hexadecimal.

Interval Box: Data is written to the AK4628A, AK4112B by this interval.

Step Box: Data changes by this step.

Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.

[Example] Start Data = 00, End Data = 09

Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.

[Example] Start Data = 00, End Data = 09

Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4628A, AK4112B, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is “.akr”.

<Operation flow>

- (1) Click [SAVE] Button.
- (2) Set the file name and click [SAVE] Button. The extension of file name is “.akr”.

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4628A, AK4112B. The file type is the same as [SAVE].

<Operation flow>

- (1) Click [OPEN] Button.
- (2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

- (1) Click [F3] Button.
- (2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.
- (3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval= "-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

| | Address | Data | Interval | | Address | Data | Interval | | | | | | |
|----|---------|------|----------|---|---------|------|----------|----|---|---|---|---|----|
| 1 | -1 | H | 0 | H | 0 | ms | 16 | -1 | H | 0 | H | 0 | ms |
| 2 | -1 | H | 0 | H | 0 | ms | 17 | -1 | H | 0 | H | 0 | ms |
| 3 | -1 | H | 0 | H | 0 | ms | 18 | -1 | H | 0 | H | 0 | ms |
| 4 | -1 | H | 0 | H | 0 | ms | 19 | -1 | H | 0 | H | 0 | ms |
| 5 | -1 | H | 0 | H | 0 | ms | 20 | -1 | H | 0 | H | 0 | ms |
| 6 | -1 | H | 0 | H | 0 | ms | 21 | -1 | H | 0 | H | 0 | ms |
| 7 | -1 | H | 0 | H | 0 | ms | 22 | -1 | H | 0 | H | 0 | ms |
| 8 | -1 | H | 0 | H | 0 | ms | 23 | -1 | H | 0 | H | 0 | ms |
| 9 | -1 | H | 0 | H | 0 | ms | 24 | -1 | H | 0 | H | 0 | ms |
| 10 | -1 | H | 0 | H | 0 | ms | 25 | -1 | H | 0 | H | 0 | ms |
| 11 | -1 | H | 0 | H | 0 | ms | | | | | | | |
| 12 | -1 | H | 0 | H | 0 | ms | | | | | | | |
| 13 | -1 | H | 0 | H | 0 | ms | | | | | | | |
| 14 | -1 | H | 0 | H | 0 | ms | | | | | | | |
| 15 | -1 | H | 0 | H | 0 | ms | | | | | | | |

Start Step

START Help

Save OPEN Close

Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

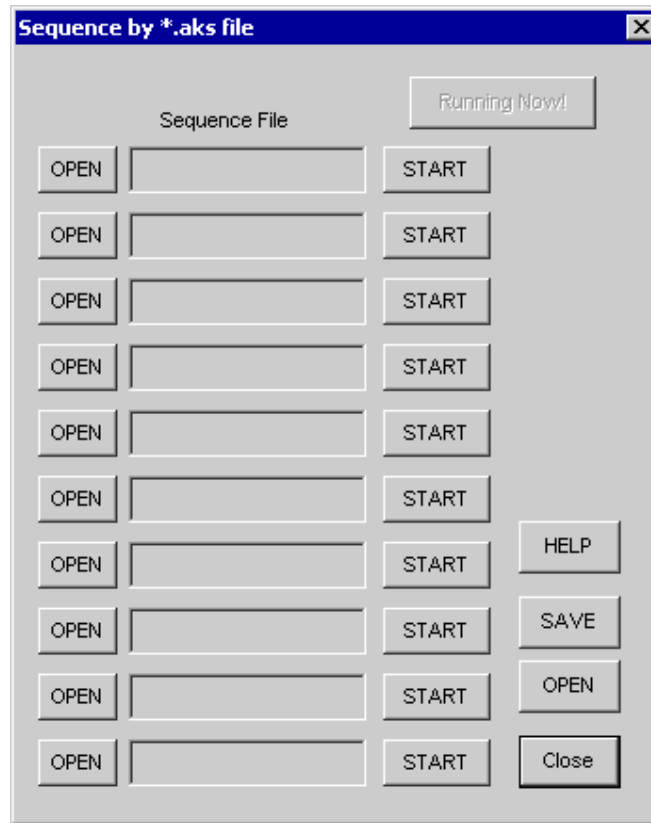


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 3. (In case that the selected sequence file name is “DAC_Stereo_ON.aks”)

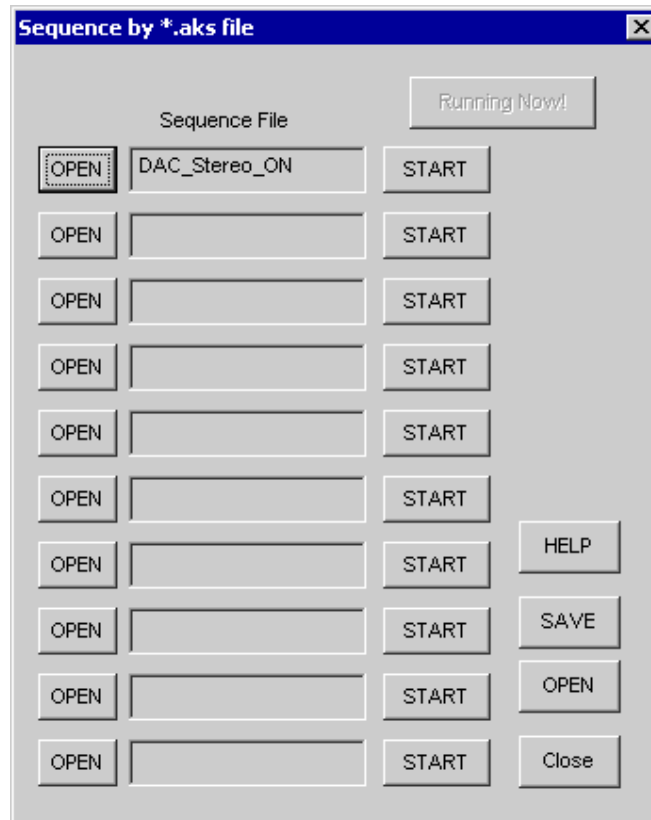


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The file name is “*.ak4”.

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 4 opens.

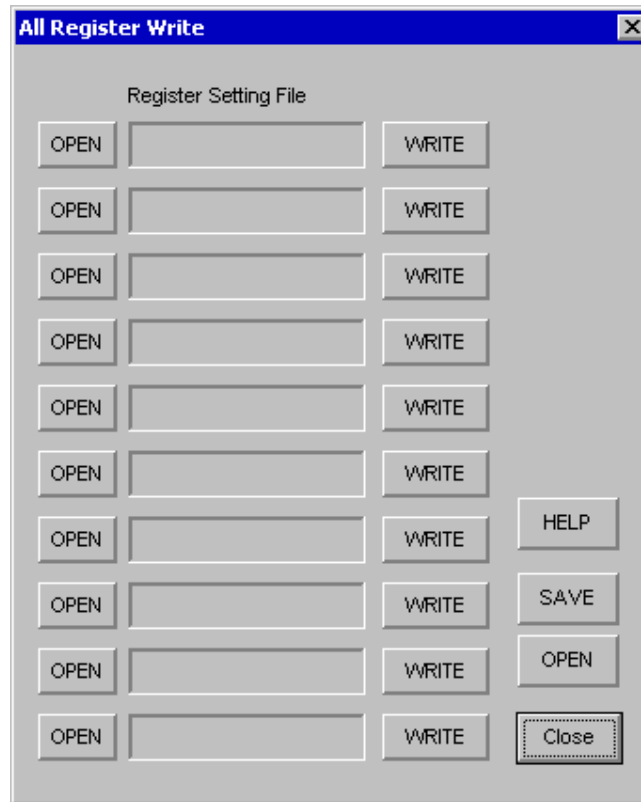


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

- (1) Click [OPEN] button and select the register setting file (*.akr).
- (2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".

[OPEN] : The name assign of register setting file(*.ak5) saved by [SAVE] is loaded.

7-3. Note

- (1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.
- (2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

| |
|----------------------------|
| MEASUREMENT RESULTS |
|----------------------------|

1) ADC part

[Measurement condition]

- Measurement unit: Audio Precision, System two, Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz(fs=48kHz), 10Hz~48kHz(fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=DVDD= TVDD=5V
- Interface : DIT(AK4103)
- Temperature : Room

fs=48kHz

| Parameter | Input signal | Measurement filter | Lch | Rch |
|-----------|--------------|--------------------|---------|---------|
| S/(N+D) | 1kHz, -0.5dB | 20kLPF | 95.6dB | 95.7dB |
| DR | 1kHz, -60dB | 20kLPF | 99.3dB | 99.0dB |
| | | 20kLPF+A-weighted | 101.8dB | 101.2dB |
| S/N | No signal | 20kLPF | 99.5dB | 99.4dB |
| | | 20kLPF+A-weighted | 101.8dB | 101.2dB |

fs=96kHz

| Parameter | Input signal | Measurement filter | Lch | Rch |
|-----------|--------------|--------------------|--------|--------|
| S/(N+D) | 1kHz, -0.5dB | fs/2 | 91.7dB | 92.2dB |
| DR | 1kHz, -60dB | fs/2 | 96.3dB | 95.9dB |
| | | fs/2+A-weighted | 99.0dB | 98.1dB |
| S/N | No signal | fs/2 | 96.3dB | 95.9dB |
| | | fs/2+A-weighted | 99.1dB | 98.1dB |

2) DAC part

[Measurement condition]

- Measurement unit: Audio Precision, System two, Cascade(fs=48kHz, 96kHz)
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~22kHz (fs=48kHz), 10Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=DVDD= TVDD=5V
- Interface : DIR(AK4112B)
- Temperature : Room

fs=48kHz

| Parameter | Input signal | Measurement filter | Lch | Rch |
|-----------|--------------|--------------------|---------|---------|
| S/(N+D) | 1kHz, 0dB | 20kLPF | 97.7dB | 97.4dB |
| DR | 1kHz, -60dB | 20kLPF | 102.6dB | 102.6dB |
| | | 22kLPF+A-weighted | 105.7dB | 105.5dB |
| S/N | No signal | 20kLPF | 102.5dB | 102.5dB |
| | | 22kLPF+A-weighted | 105.9dB | 105.9dB |

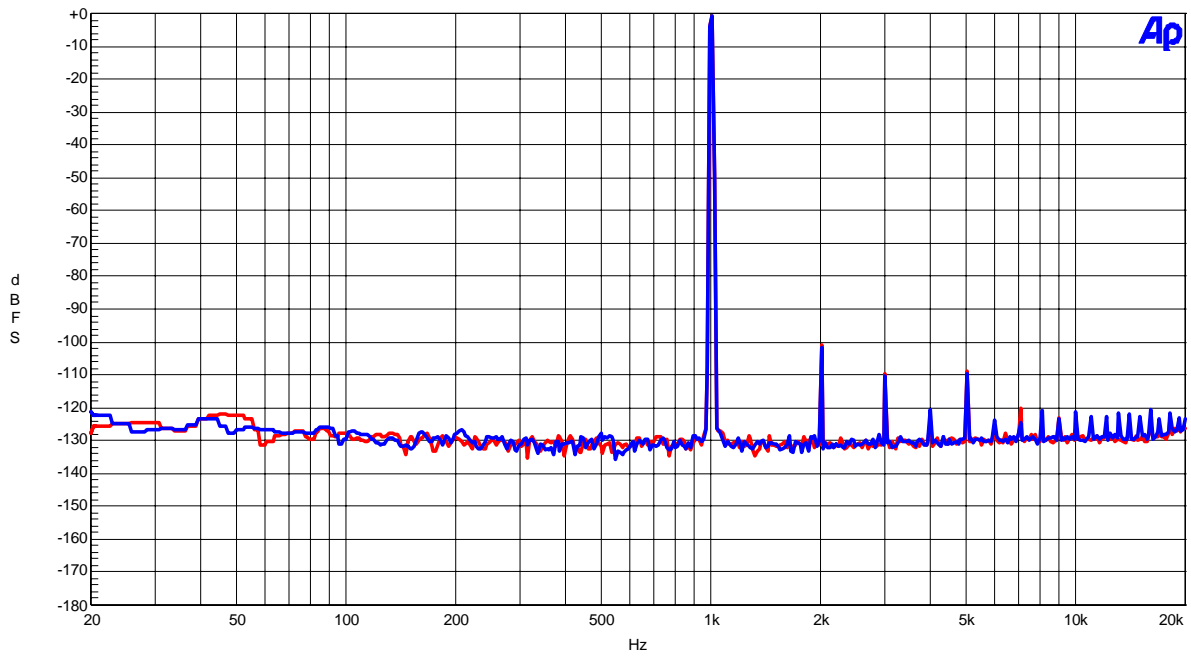
fs=96kHz

| Parameter | Input signal | Measurement filter | Lch | Rch |
|-----------|--------------|--------------------|---------|---------|
| S/(N+D) | 1kHz, 0dB | 40kHzLPF | 92.7dB | 92.7dB |
| DR | 1kHz, -60dB | 40kHzLPF | 100.3dB | 100.3dB |
| | | 40kHz +A-weighted | 105.7dB | 105.9dB |
| S/N | No signal | 40kHz | 100.7dB | 100.8dB |
| | | 40kHz +A-weighted | 106.1dB | 106.3dB |

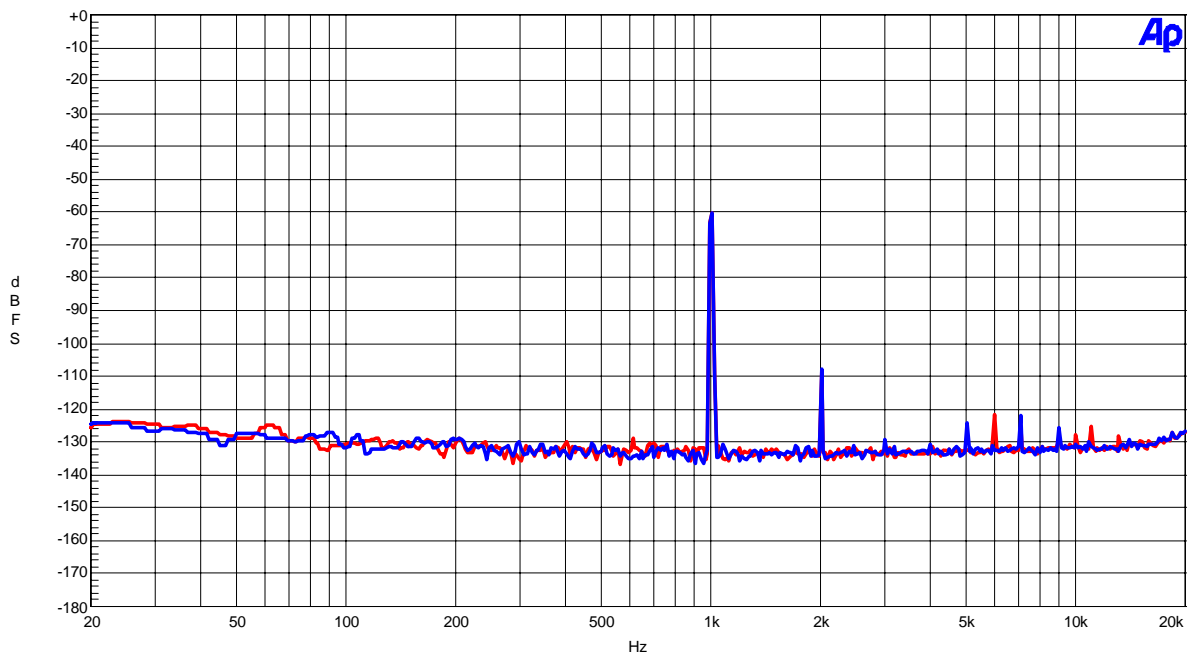
1.ADC

(ADC fs=48kHz)

AKM

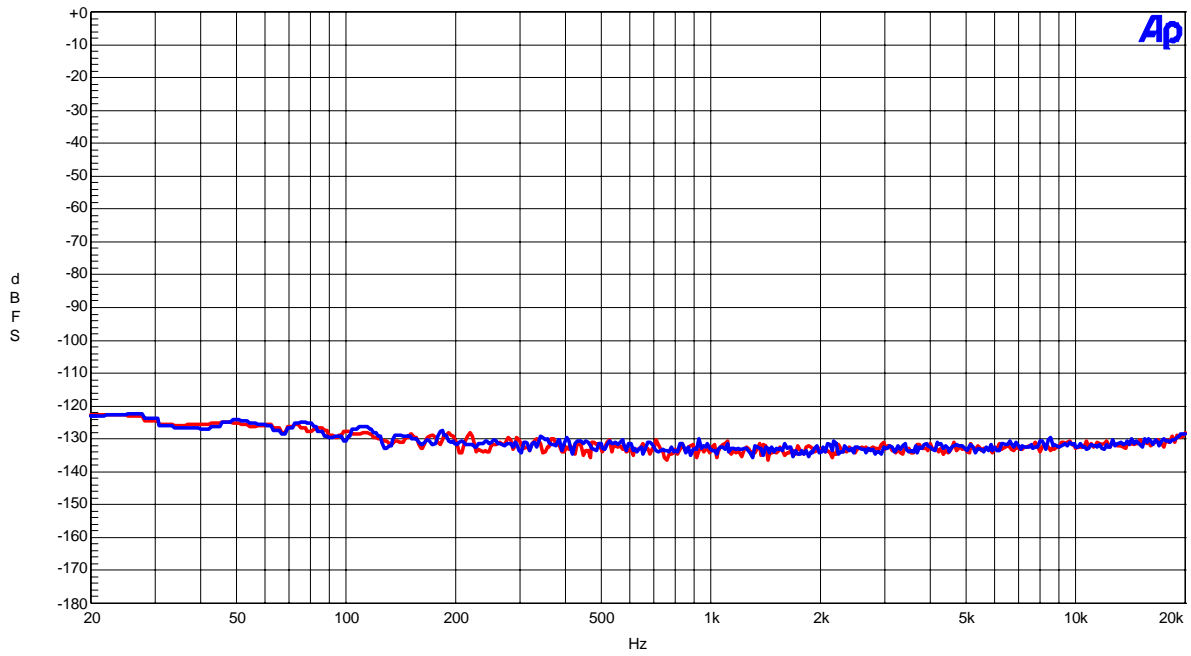
AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, -0.5dB_r input, fin=1kHzFFT (Input=-0.5dB_r, fin=1kHz)

AKM

AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, -60dB_r input, fin=1kHzFFT (Input=-60dB_r, fin=1kHz)

(ADC fs=48kHz)

AKM

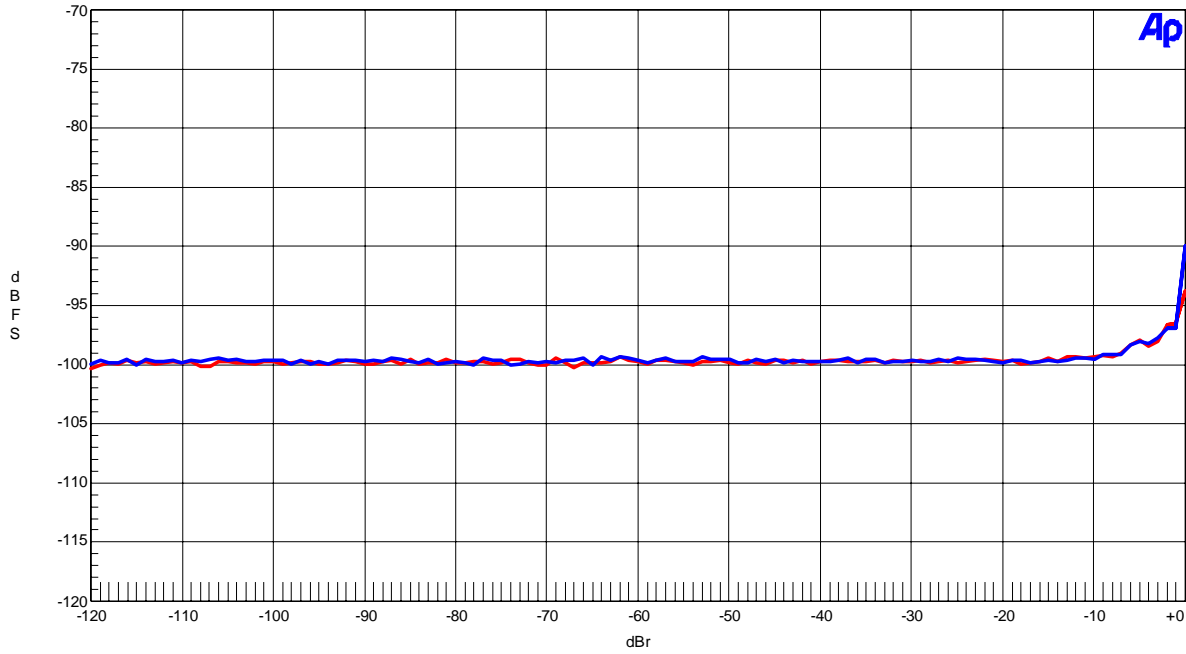
AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, No signal input, fin=1kHz

FFT (noise floor)

(ADC fs=48kHz)

AKM

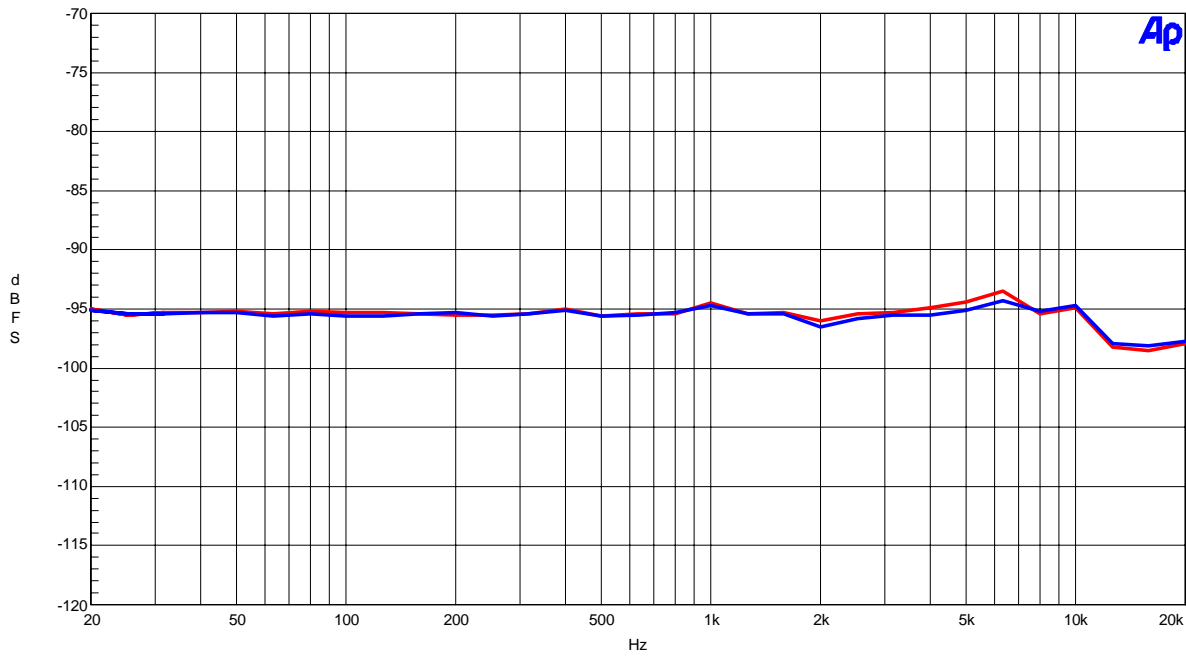
AK4628A THD+N vs. Input Level
 AVDD=DVDD=5V, fs=96kHz, fin=1kHz



THD + N vs Amplitude (fin=1kHz)

AKM

AK4628A THD+N vs. Input Frequency
 AVDD=DVDD=5V, -0.5dBr input, fs=48kHz

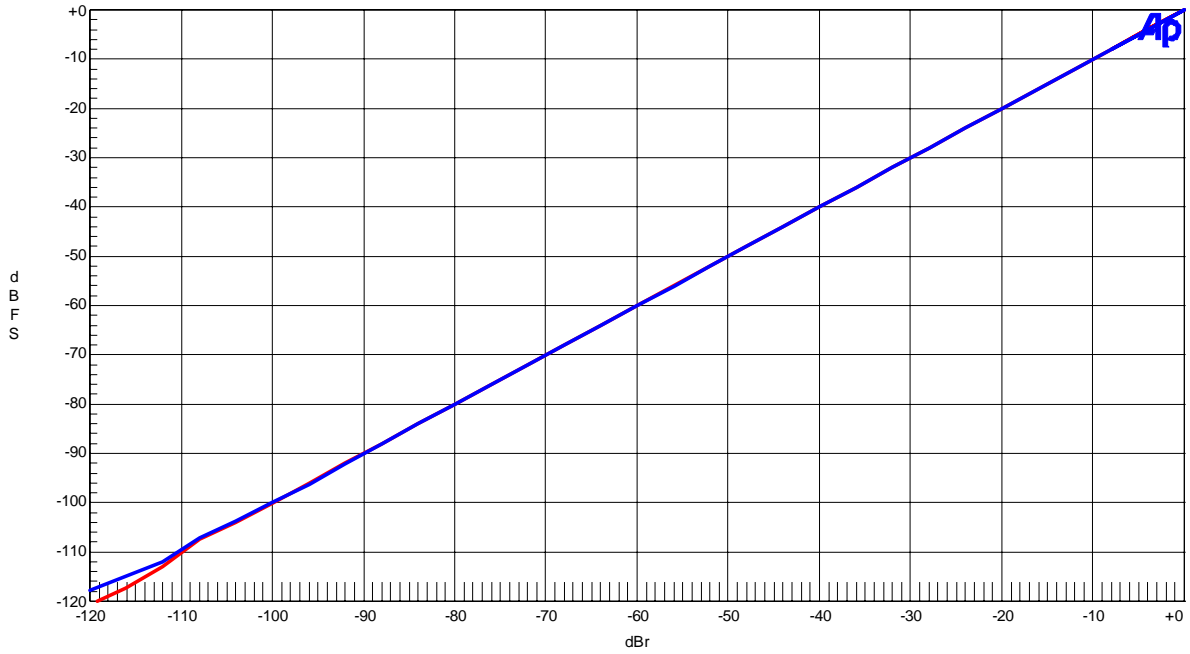


THD + N vs Input Frequency (Input=-0.5dBr)

(ADC fs=48kHz)

AKM

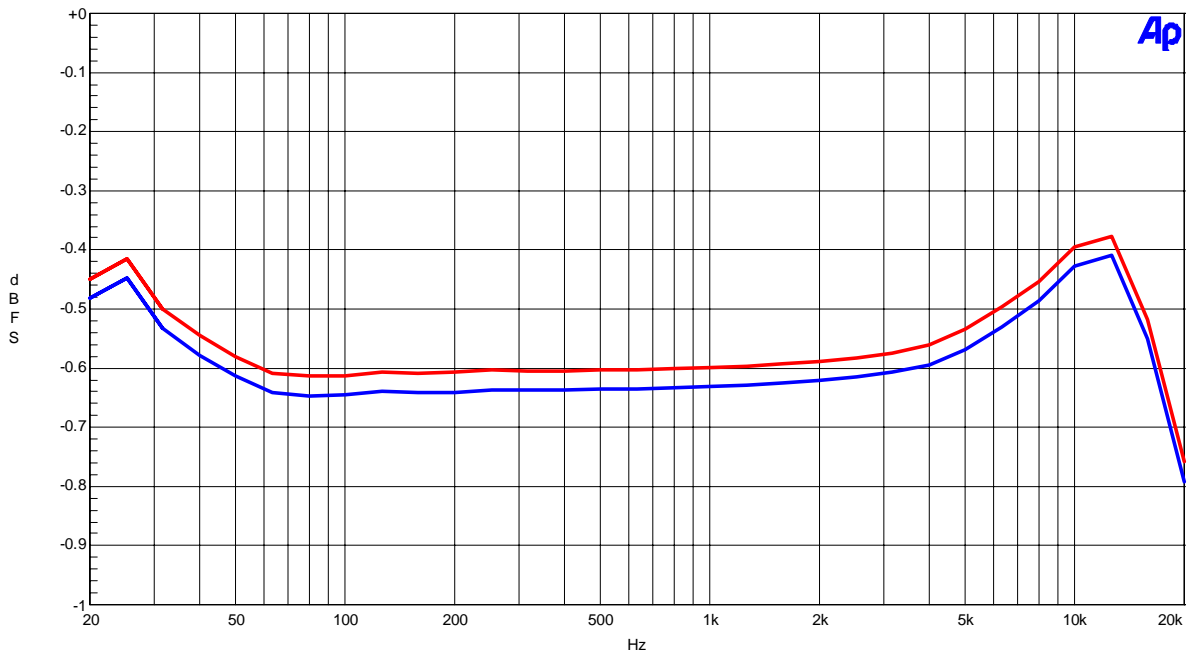
AK4628A Linearity
AVDD=DVDD=5V, fs=48kHz, fin=1kHz



Linearity(fin=1kHz)

AKM

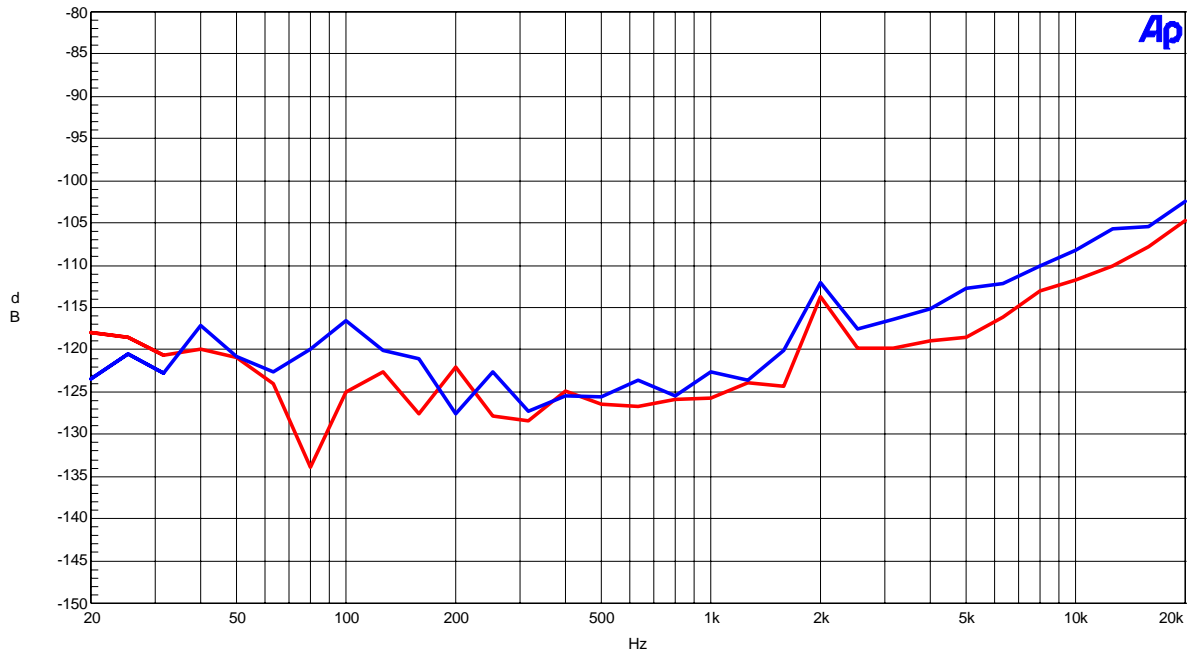
AK4628A Frequency Response
AVDD=DVDD=5V, -0.5dBr input, fs=48kHz



Frequency Response(Input Level=-0.5dBr)
(including input RC filter)

(ADC fs=48kHz)

AKM

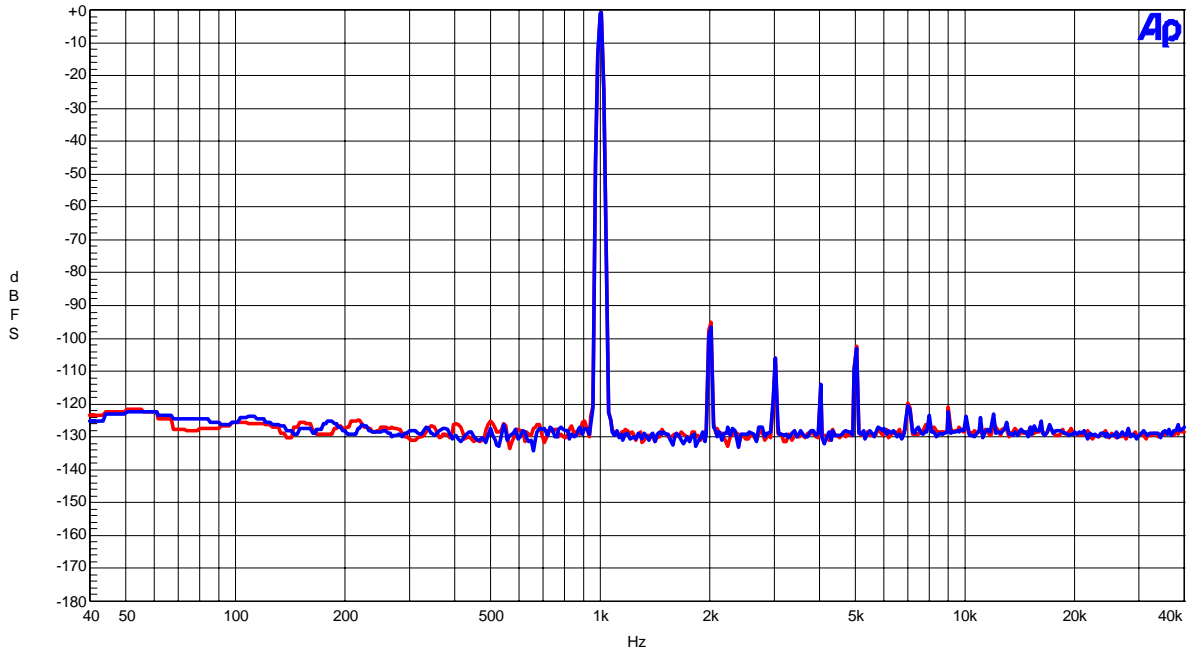
AK4628A Crosstalk
DVDD=AVDD=5V, -0.5dBm input, fs=48kHz

Crosstalk (Blue= Rch, Red = Lch)

(ADC fs=96kHz)

AKM

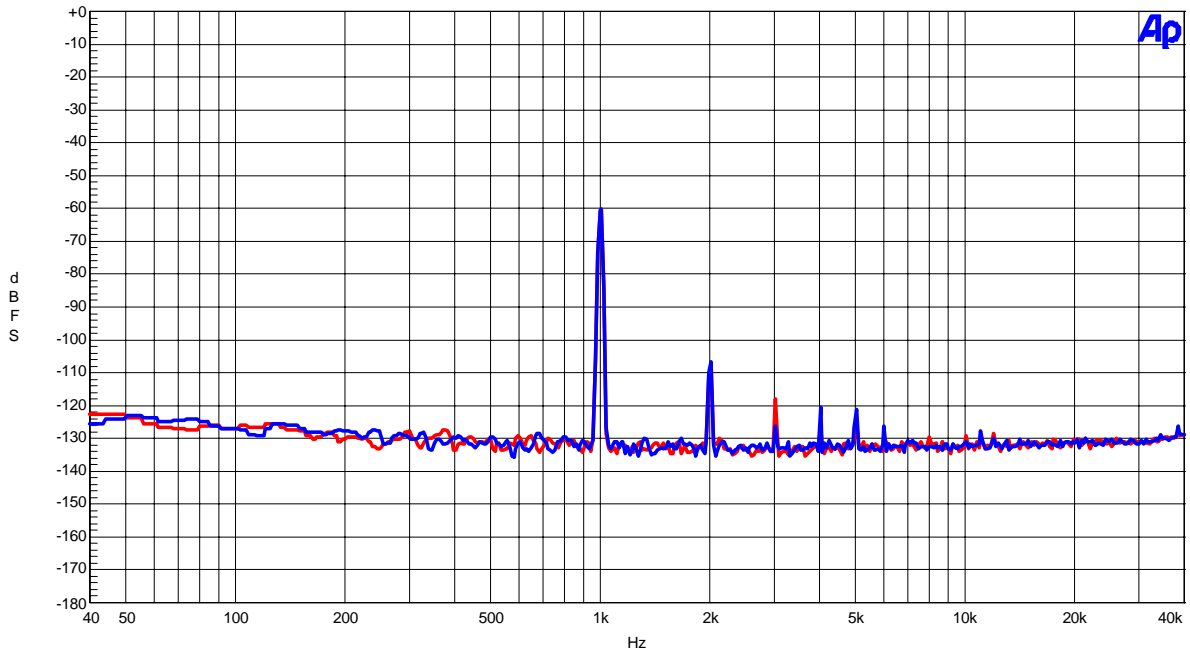
AK4628A FFT
 AVDD=DVDD=5V, fs=96kHz, -0.5dB_r input, fin=1kHz



FFT(Input=-0.5dB_r, fin=1kHz)

AKM

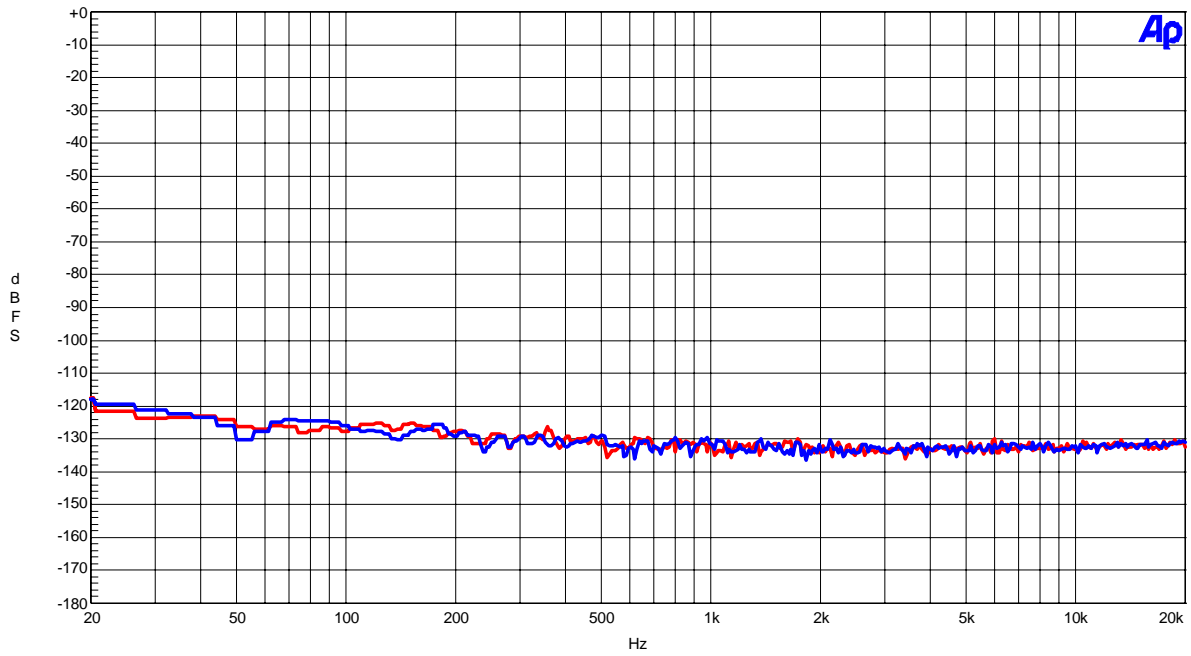
AK4628A FFT
 AVDD=DVDD=5V, fs=96kHz, -60dB_r input, fin=1kHz



FFT(Input=-60dB_r, fin=1kHz)

(ADC fs=96kHz)

AKM

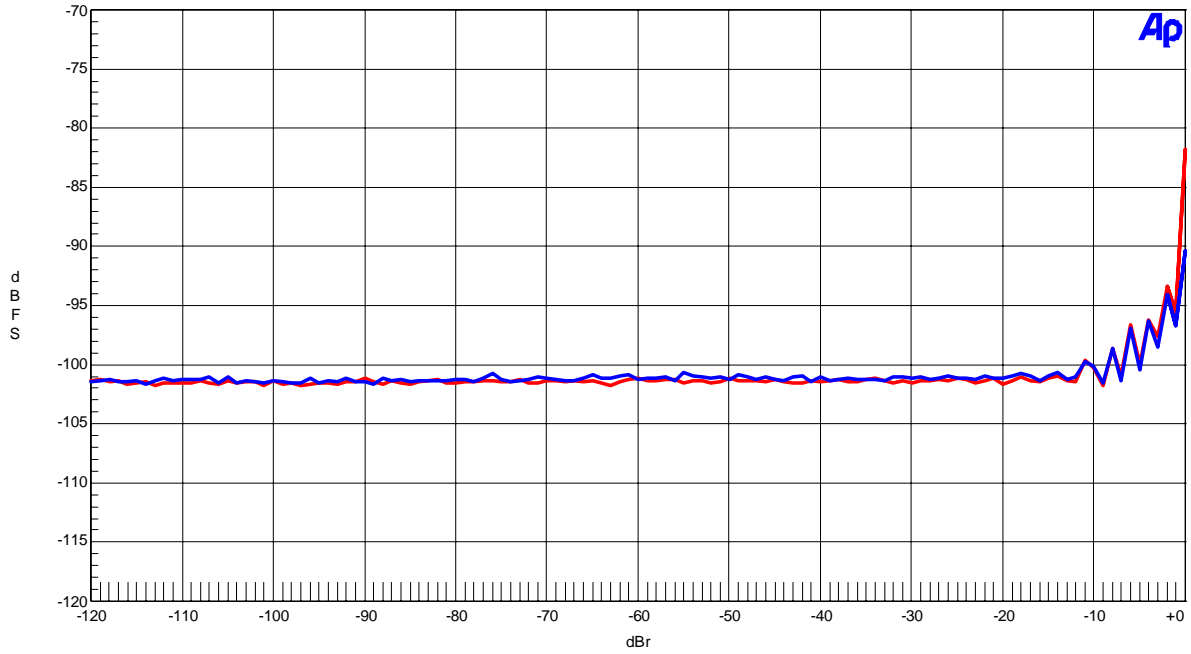
AK4628A FFT
AVDD=DVDD=5V, fs=96kHz, No signal input, fin=1kHz

FFT(Noise floor)

(ADC fs=96kHz)

AKM

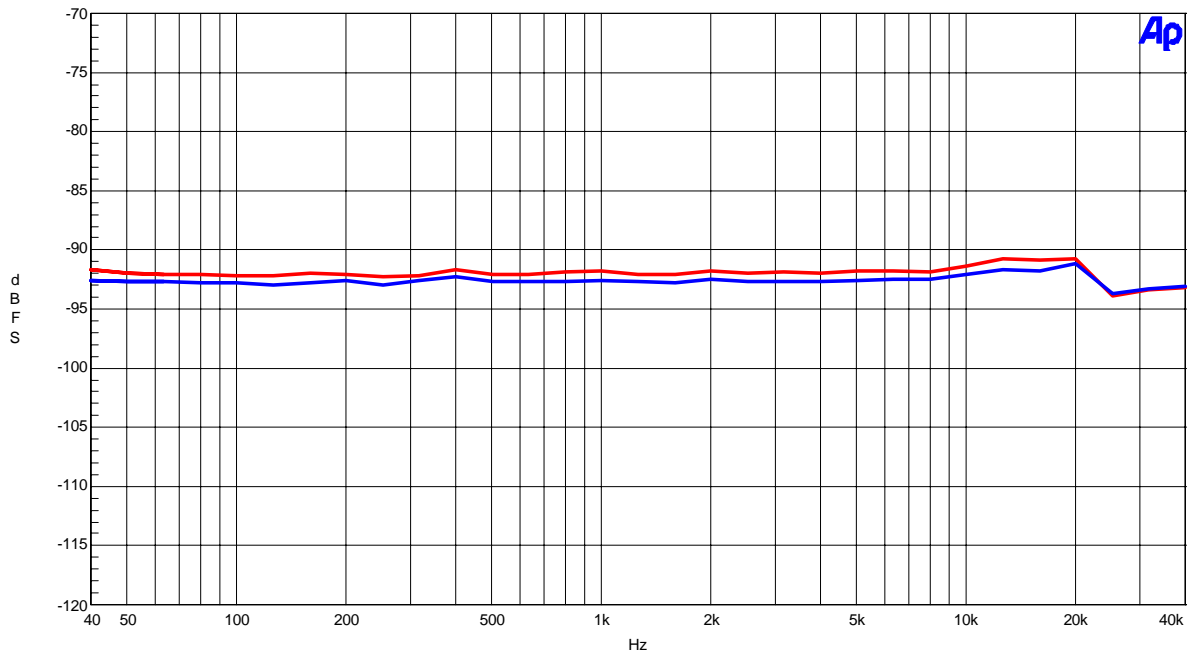
AK4628A THD+N vs. Input Level
 AVDD=DVDD=5V, fs=96kHz, fin=1kHz



THD + N vs Amplitude(fin=1kHz)

AKM

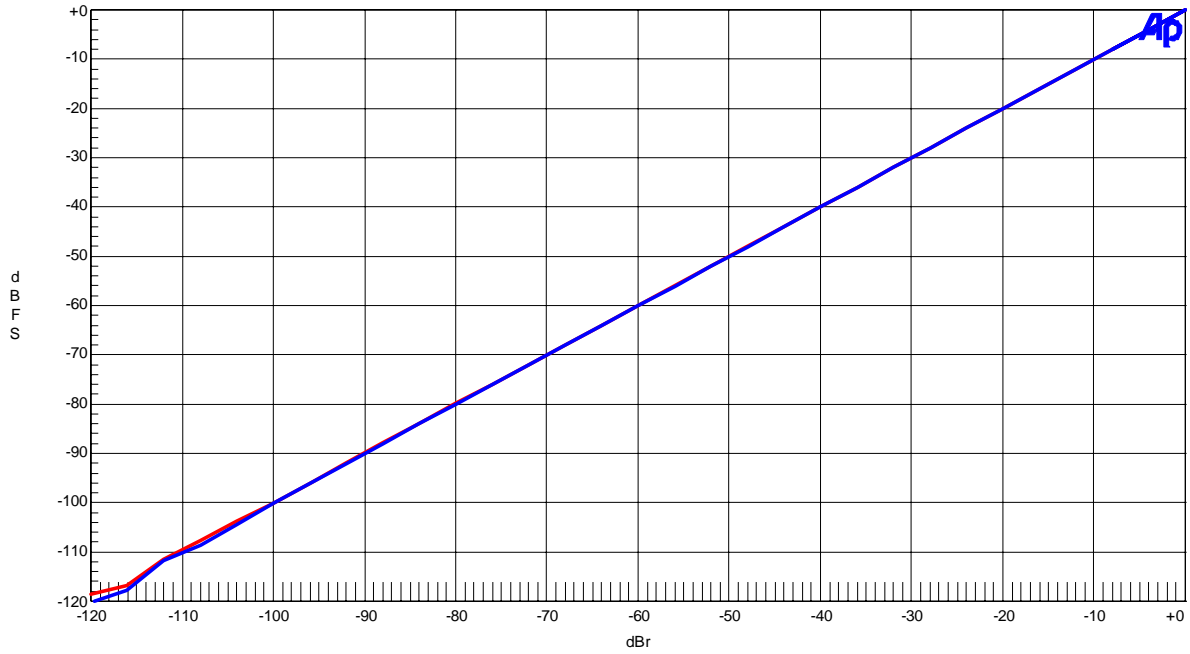
AK4628A THD+N vs. Input Frequency
 AVDD=DVDD=5V, -0.5dBr input, fs=96kHz



THD + N vs Input Frequency(Input Level=-0.5dBr)

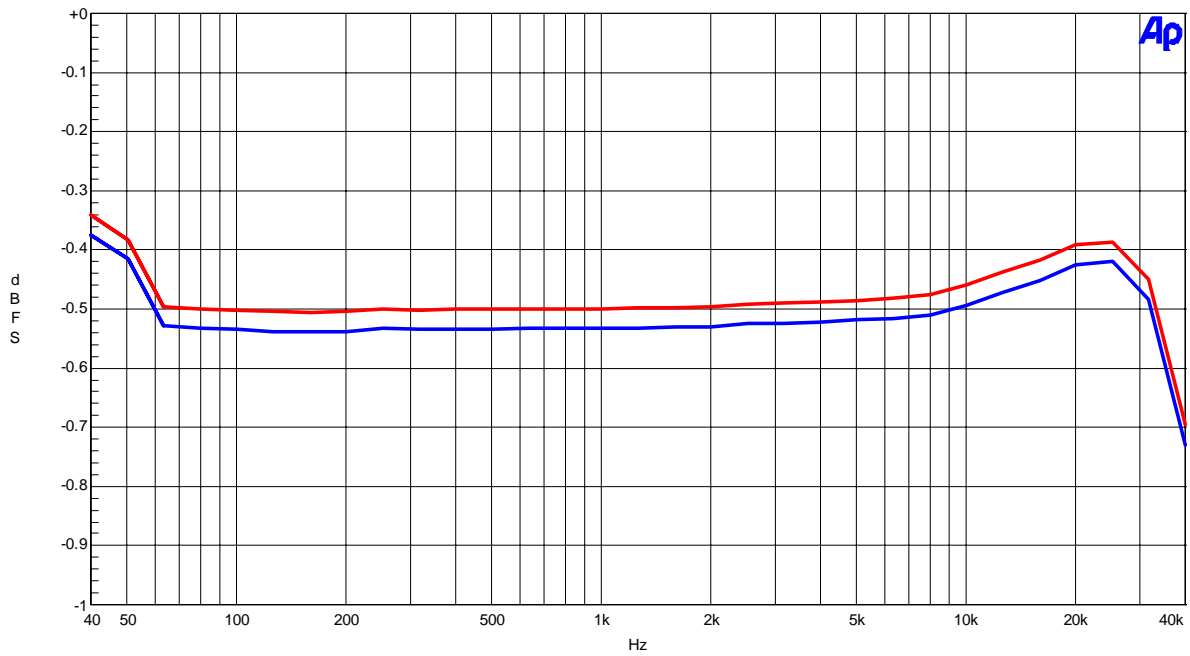
(ADC fs=96kHz)

AKM

AK4628A Linearity
AVDD=DVDD=5V, fs=96kHz, fin=1kHz

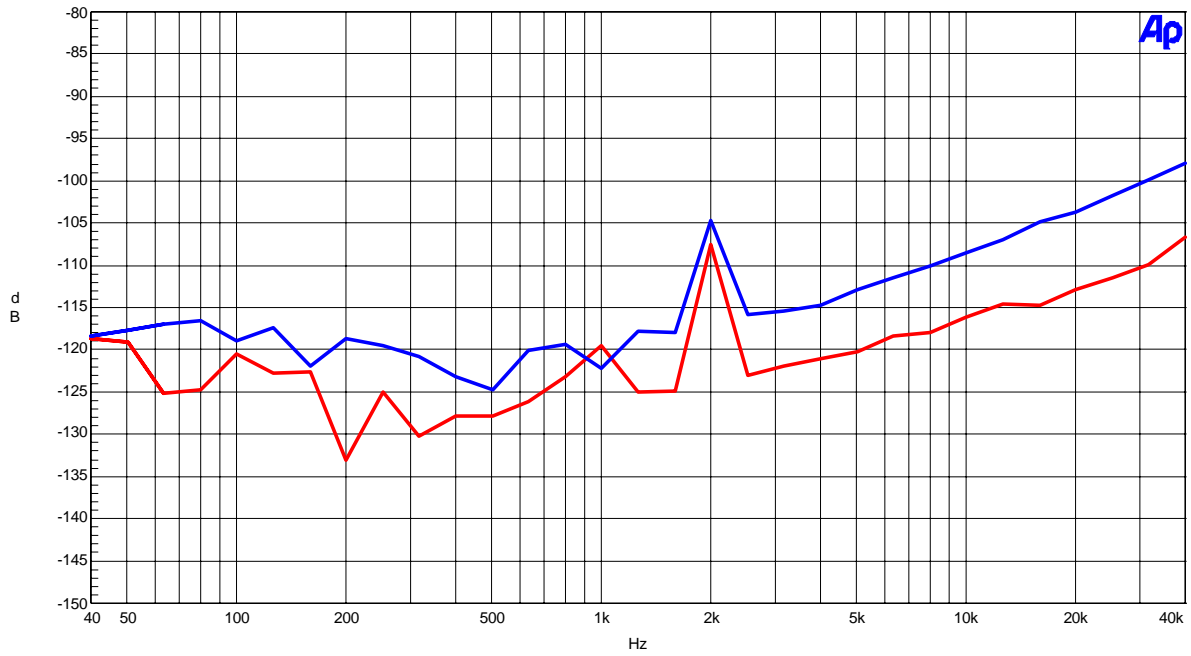
Linearity(fin=1kHz)

AKM

AK4628A Frequency Response
AVDD=DVDD=5V, -0.5dBr input, fs=96kHzFrequency Response(Input Level=-0.5dBr)
(including input RC filter)

(ADC fs=96kHz)

AKM

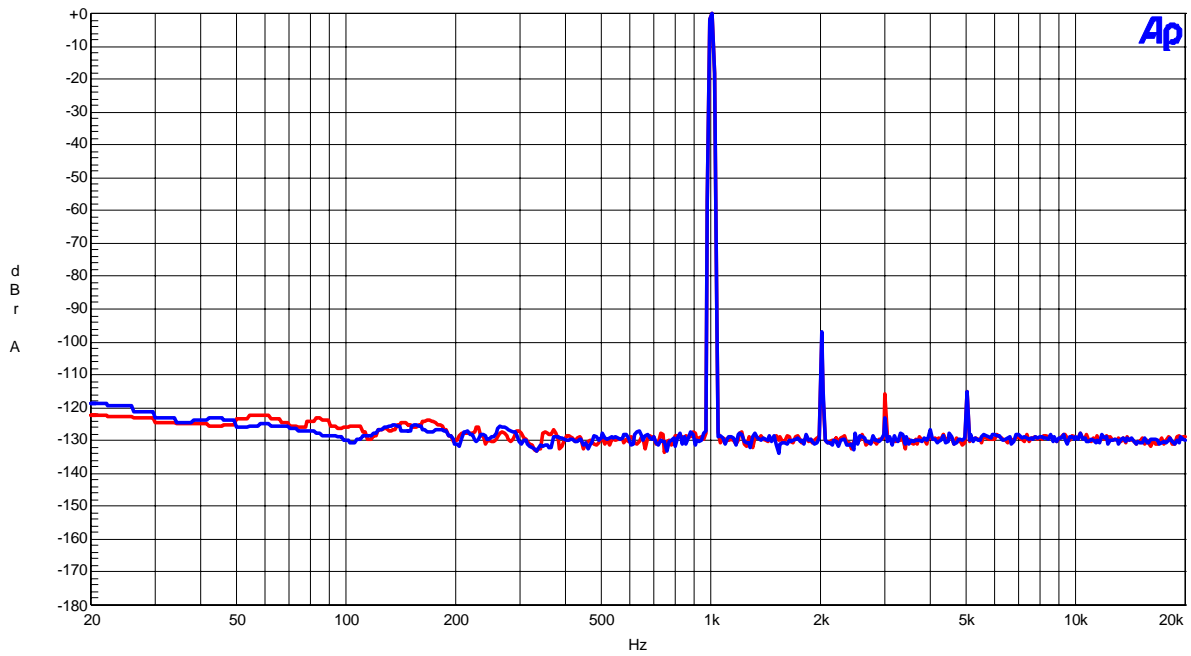
AK4628A Crosstalk
DVDD=AVDD=5V, -0.5dB_r input, fs=96kHz

Crosstalk (Blue= Rch, Red = Lch)

2.DAC

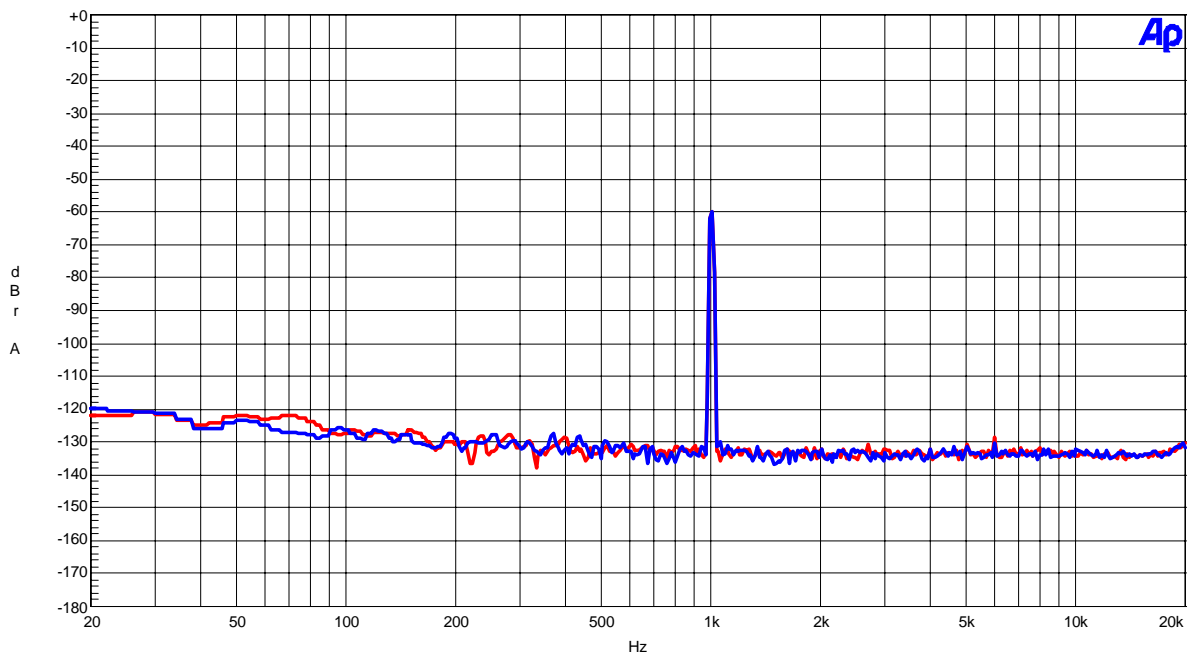
(DAC fs=48kHz)

AKM

AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, MCLK=512, 0dBFS input, fin=1kHz

FFT (Input=0dBFS, fin=1kHz)

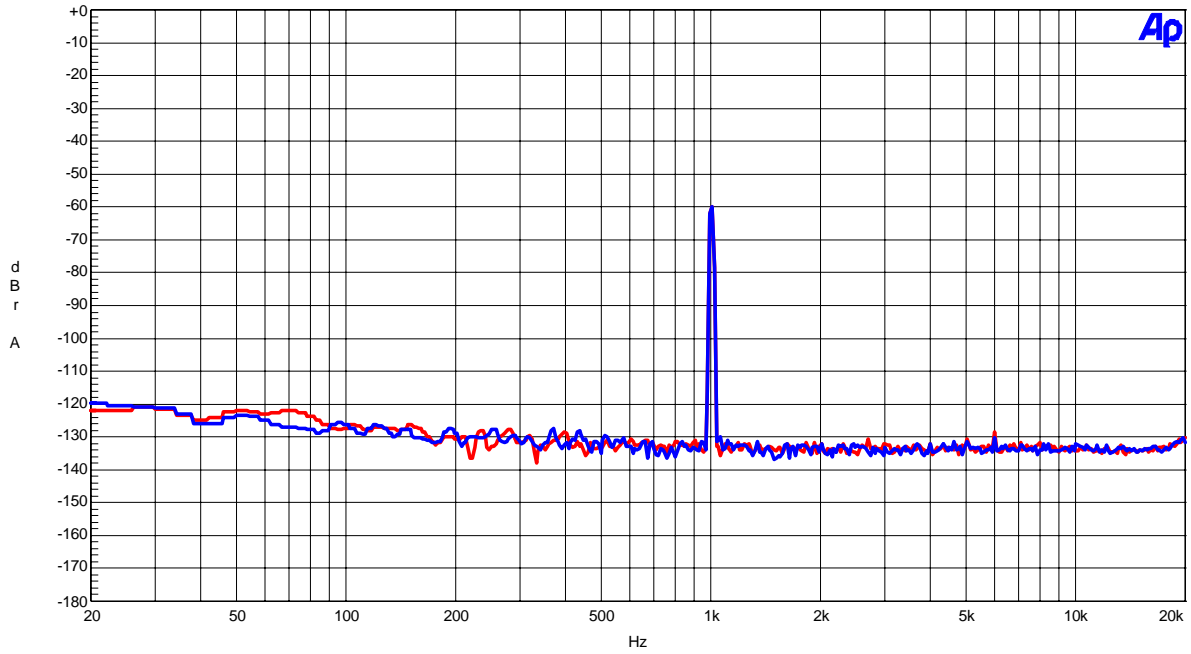
AKM

AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, MCLK=512, -60dBFS input, fin=1kHz

FFT (Input=-60dBFS, fin=1kHz)

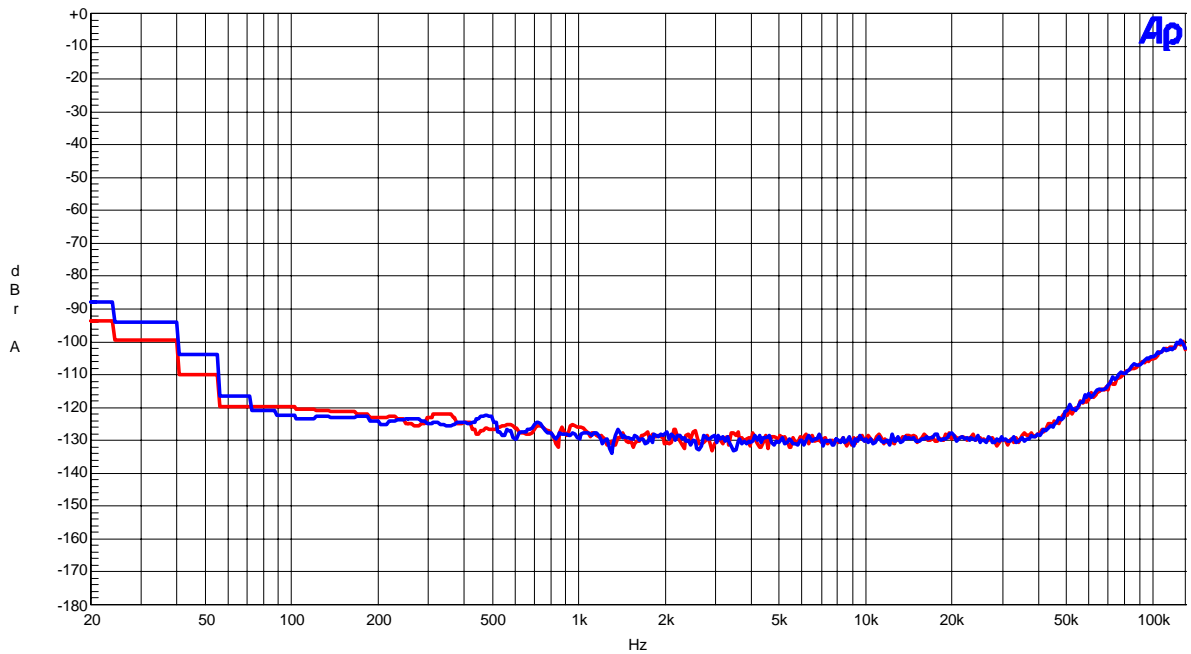
(DAC fs=48kHz)

AKM

AK4628A FFT
AVDD=DVDD=5V, fs=48kHz, fin=No signal

FFT (Noise floor)

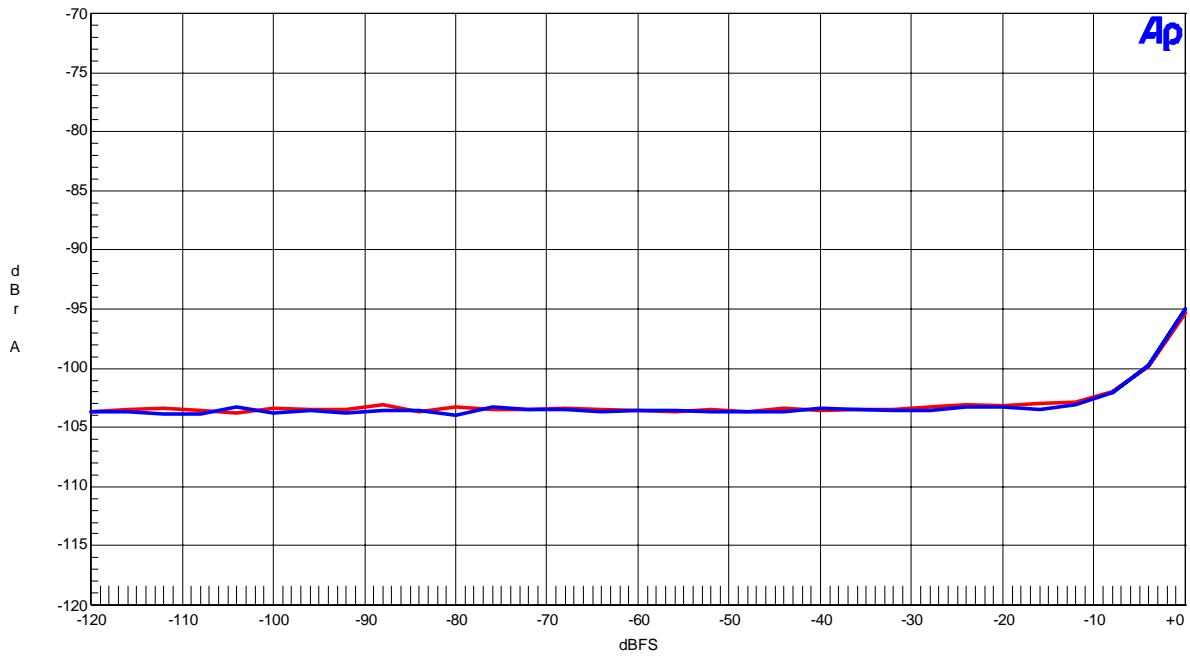
AKM

AK4628A FFT Out-of-band noise
AVDD=DVDD=5V, fs=48kHz, MCLK=512fs, fin=No signal

FFT (Out-of-band noise)

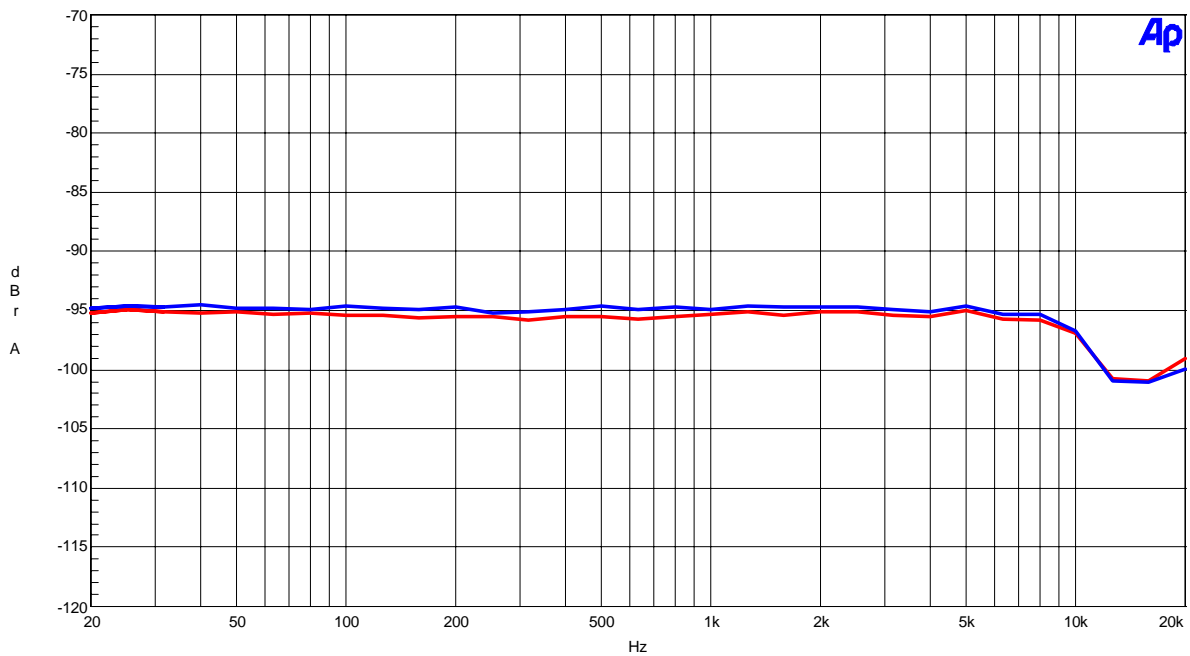
(DAC fs=48kHz)

AKM

AK4628A THD+N vs. Input Level
AVDD=DVDD=5V, fs=48kHz, MCLK=512fs, fin=1kHz

THD + N vs Amplitude(fin=1kHz)

AKM

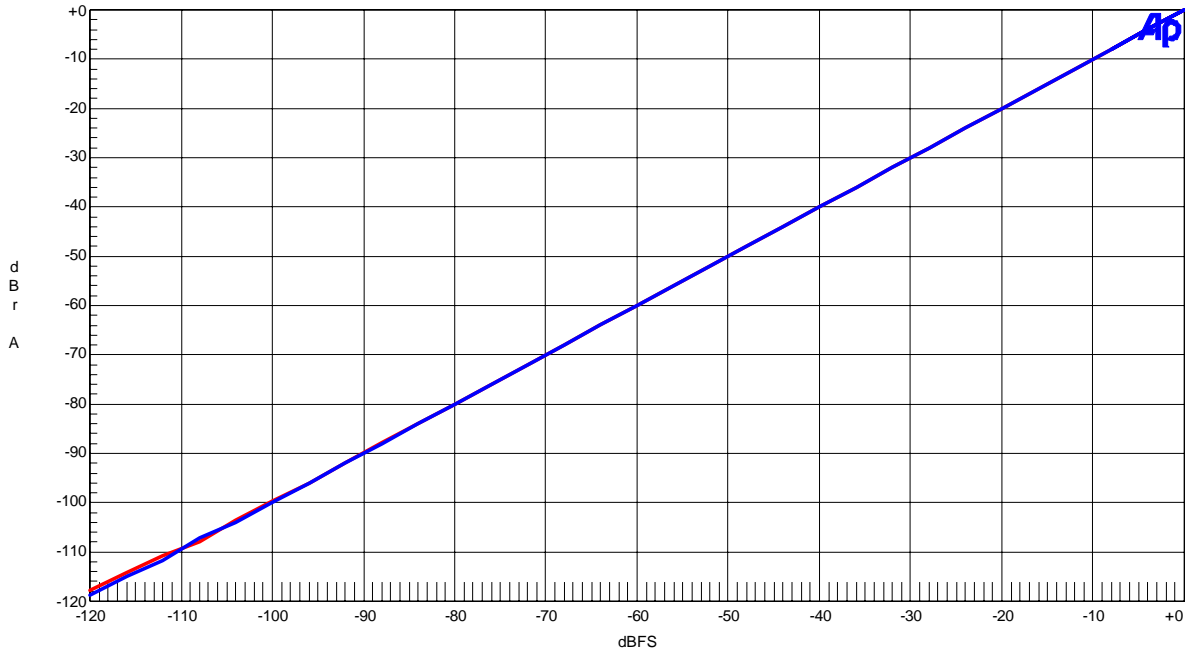
AK4628A THD+N vs. Input Frequency
AVDD=DVDD=5V, fs=48kHz, MCLK=512fs, 0dBFS input

THD + N vs Input Frequency (Input=0dBFS)

(DAC fs=48kHz)

AKM

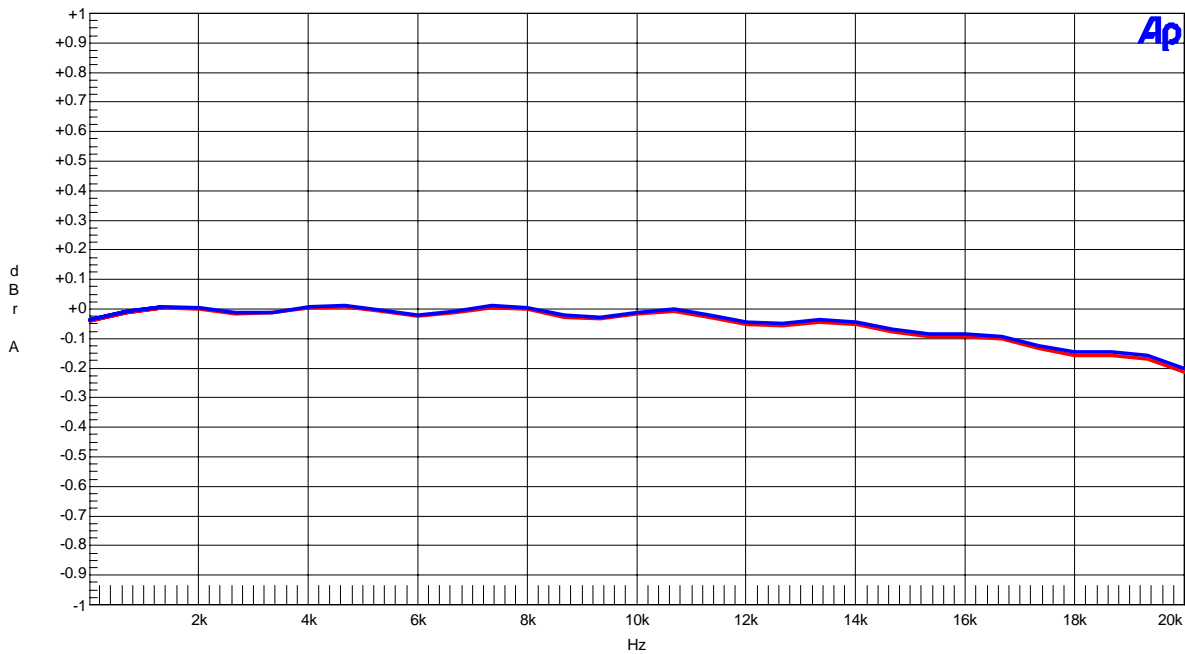
AK4628A Linearity
 AVDD=DVDD=5V, fs=48kHz, MCLK=512fs, fin=1kHz



Linearity(fin=1kHz)

AKM

AK4628A Frequency Response
 AVDD=DVDD=5V, fs=48kHz, MCLK=512fs, 0dBFS input

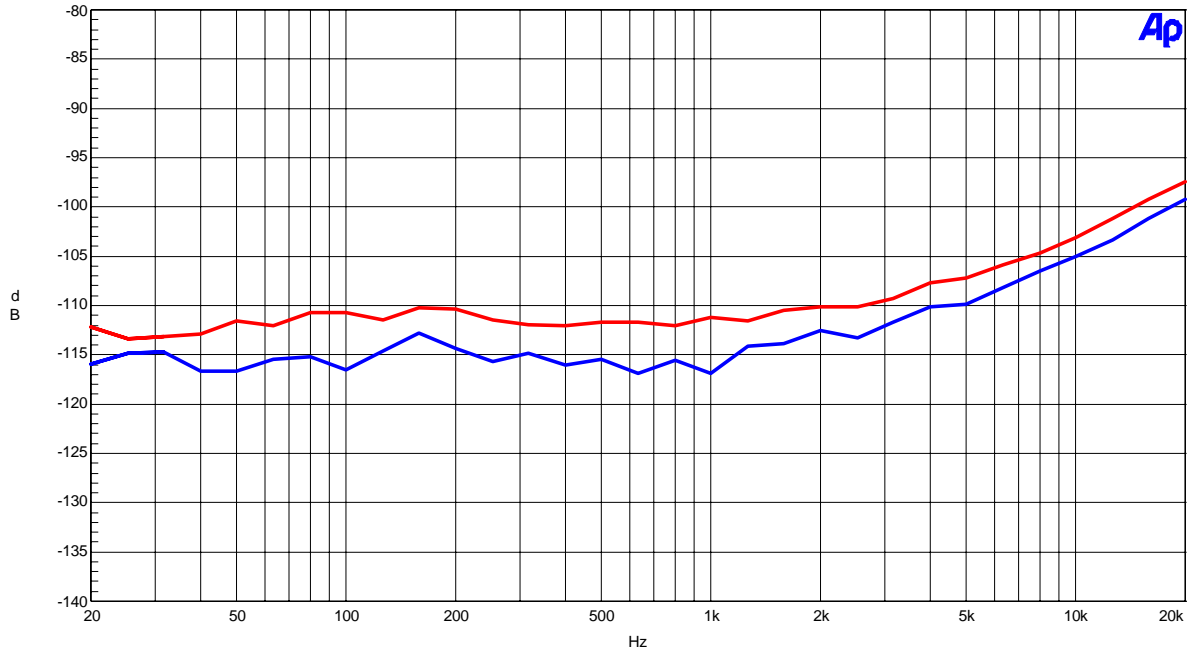


Frequency Response(Input Level=0dBFS)
 (including external RC filter)

(DAC fs=48kHz)

AKM

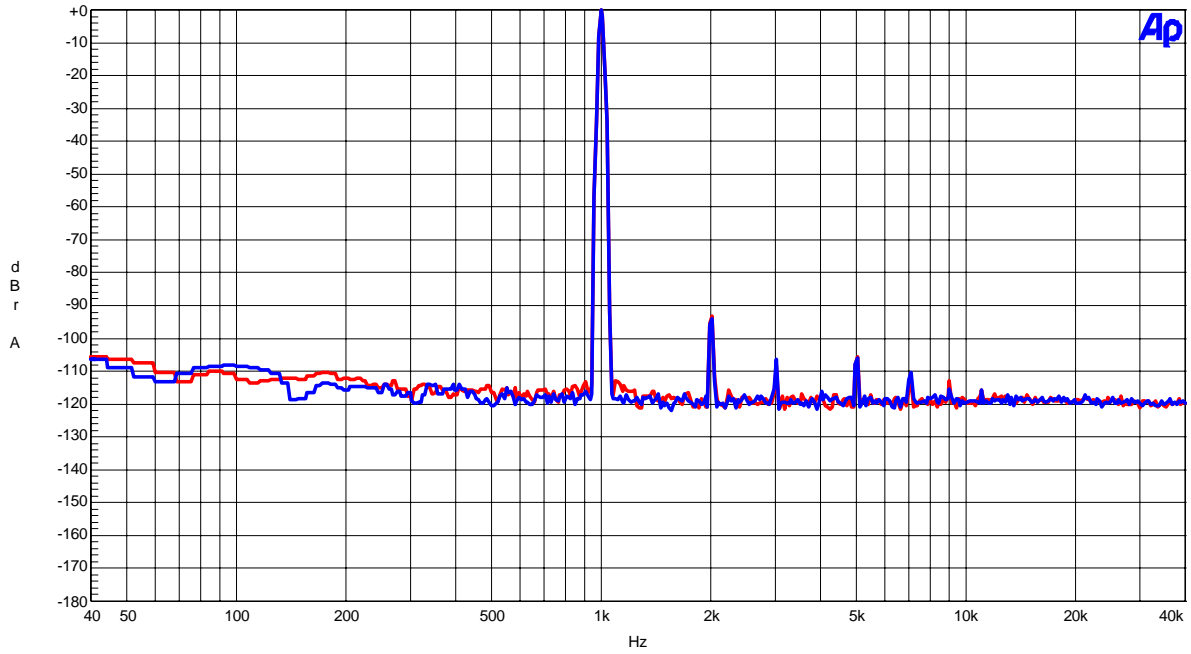
AK4628A Crosstalk (Red=Lch, Blue=Rch)
 AVDD=DVDD=5V, fs=8kHz, MCLK=512fs, 0dBFS input



Crosstalk(Red=Rch, Blue=Lch)

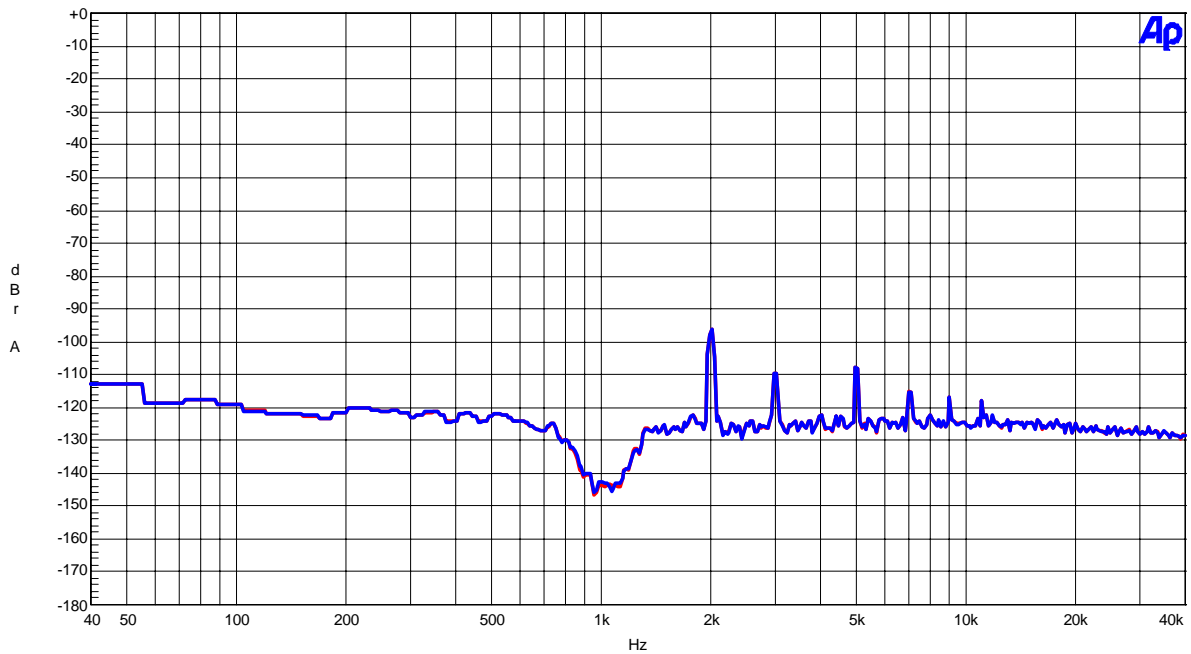
(DAC fs=96kHz)

AKM

AK4628 FFT
AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input, fin=1kHz

FFT (Input=0dBFS, fin=1kHz)

AKM

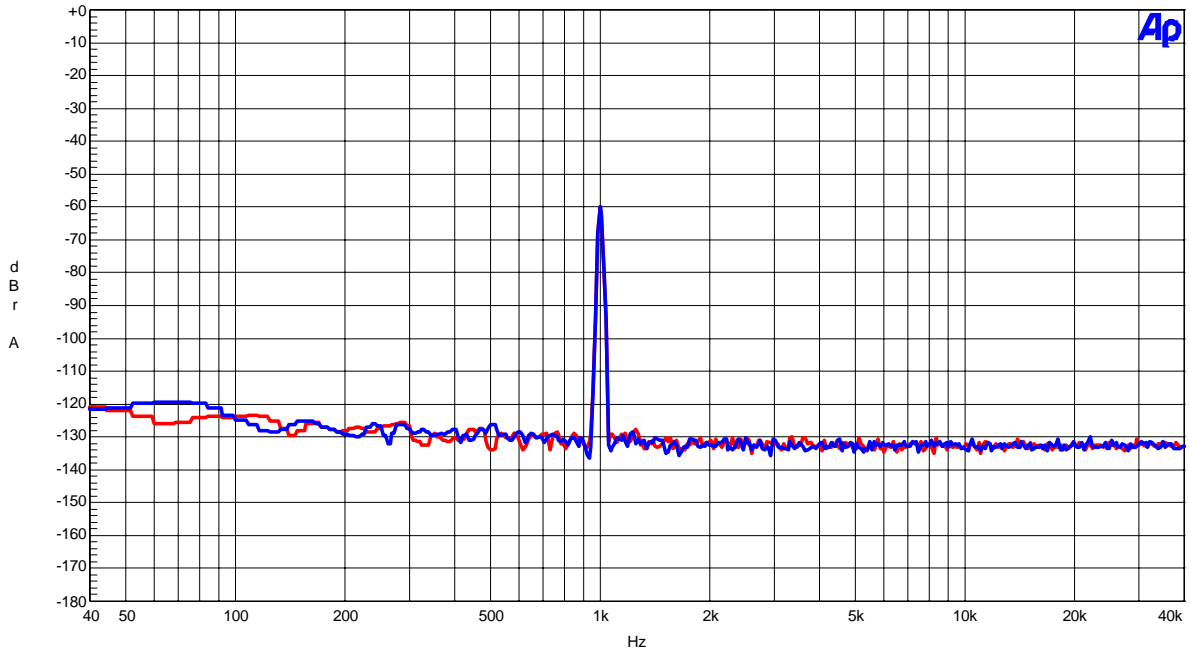
AK4628A FFT
fs=96kHz, MCLK=256fs, fin=1kHz, 0dBFS input, Notch=ON

FFT (Input=0dBFS, fin=1kHz, Notch)

(DAC fs=96kHz)

AKM

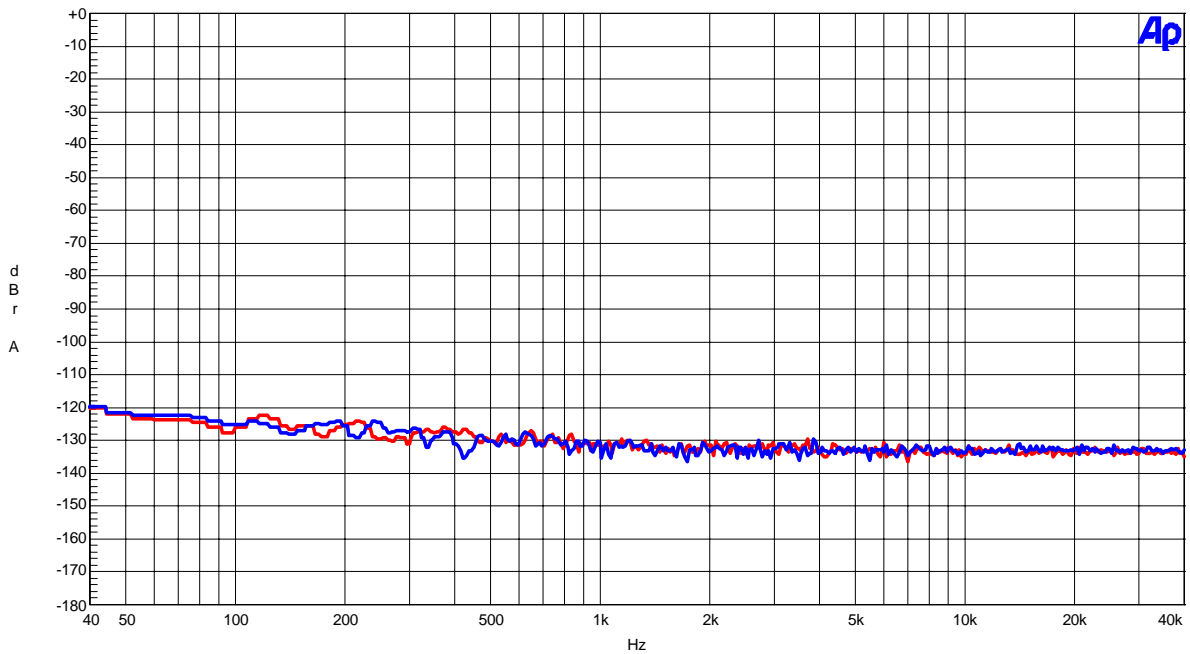
AK4628A FFT
 AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input, fin=1kHz



FFT (Input=-60dBFS,fin=1kHz)

AKM

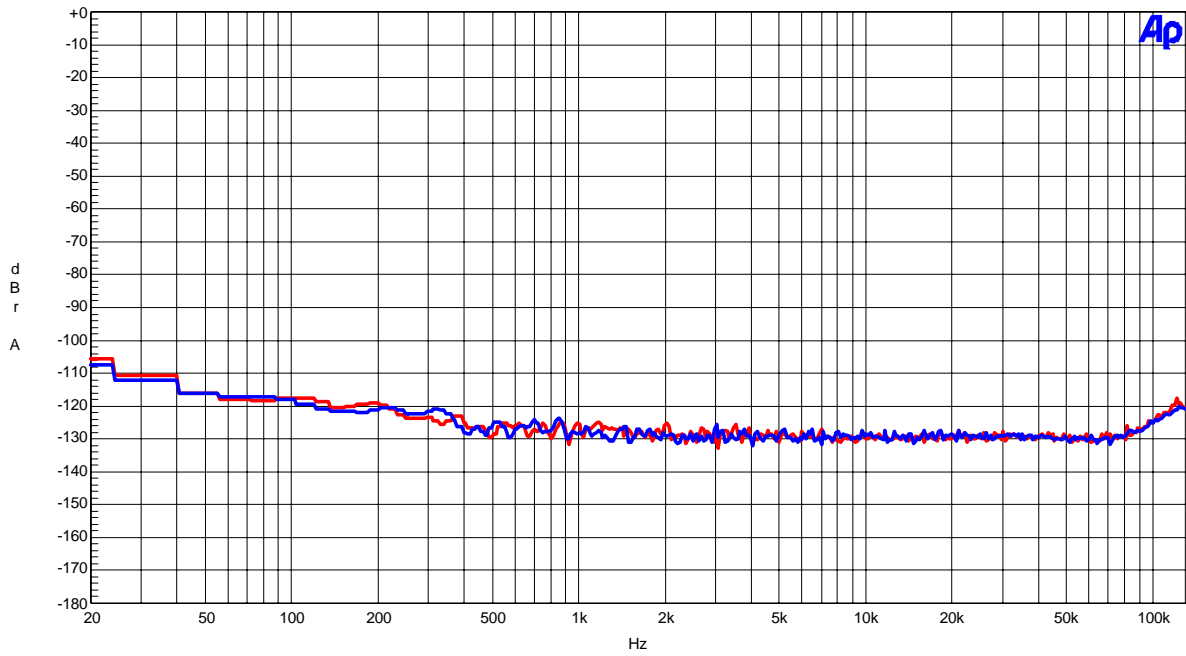
AK4628A FFT
 AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, fin=No signal input



FFT (Noise floor)

(DAC fs=96kHz)

AKM

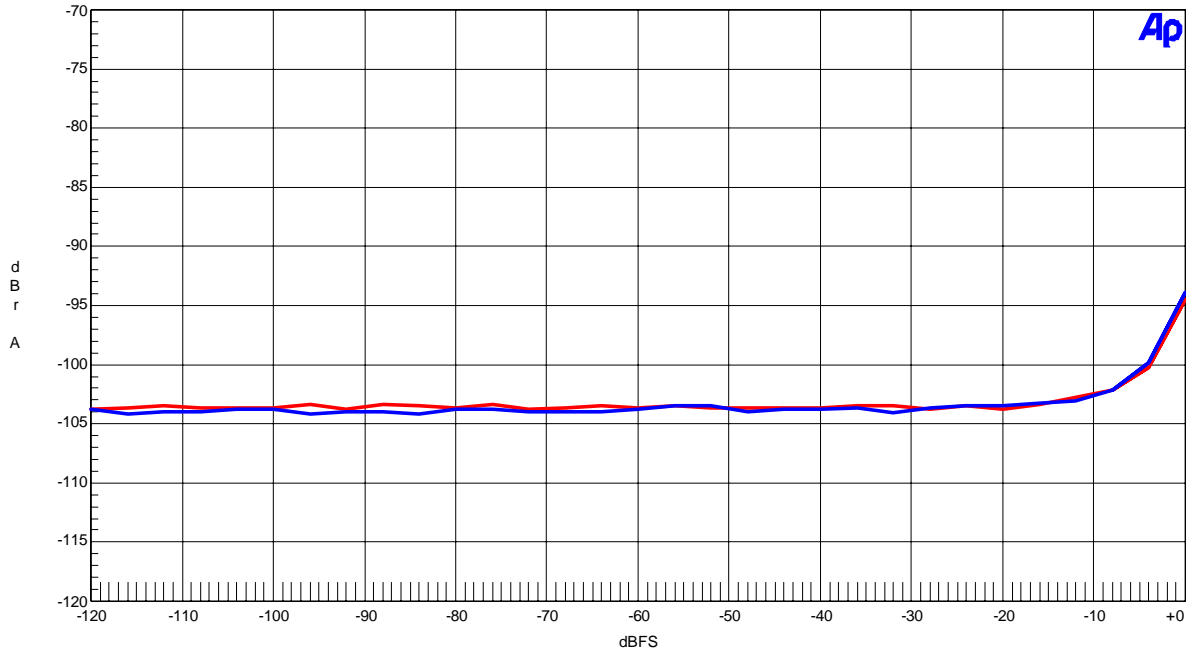
AK4626A FFT Out-of-band noise
AVDD=DVDD=5V, fs=44.1kHz, MCLK=512fs, fin=No signal

FFT (Out-of-band noise)

(DAC fs=96kHz)

AKM

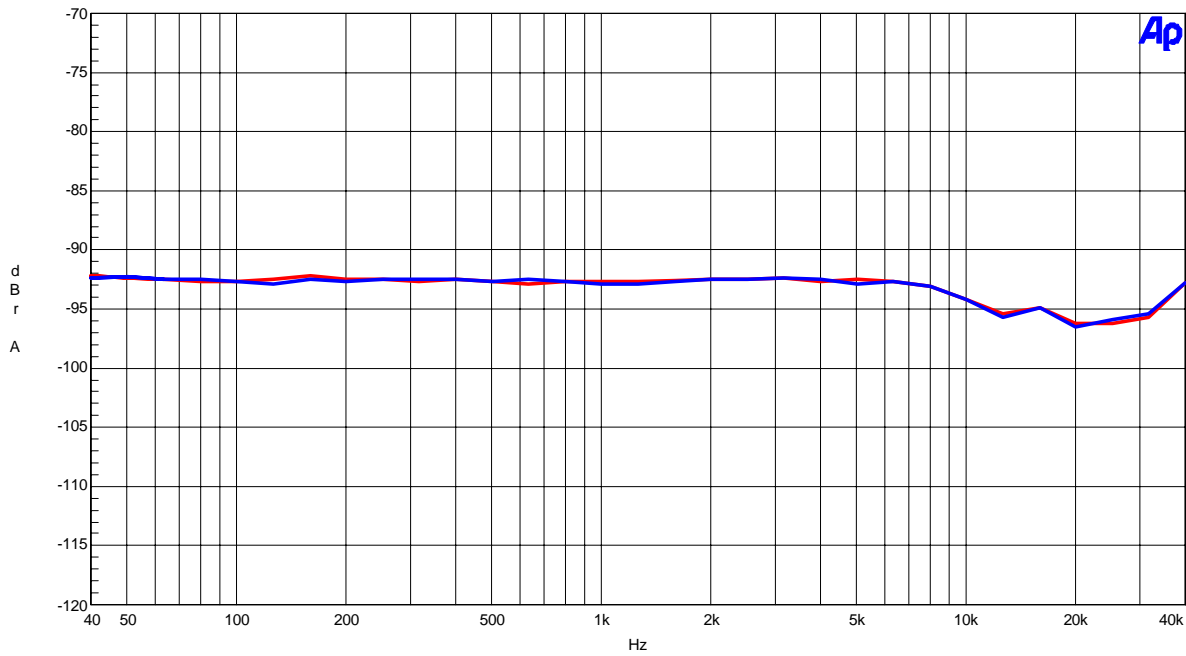
AK4626A THD+N vs. Input Level
 AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, fin=1kHz



THD + N vs Amplitude (fin=1kHz)

AKM

AK4628A THD+N vs. Input Frequency
 VDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input

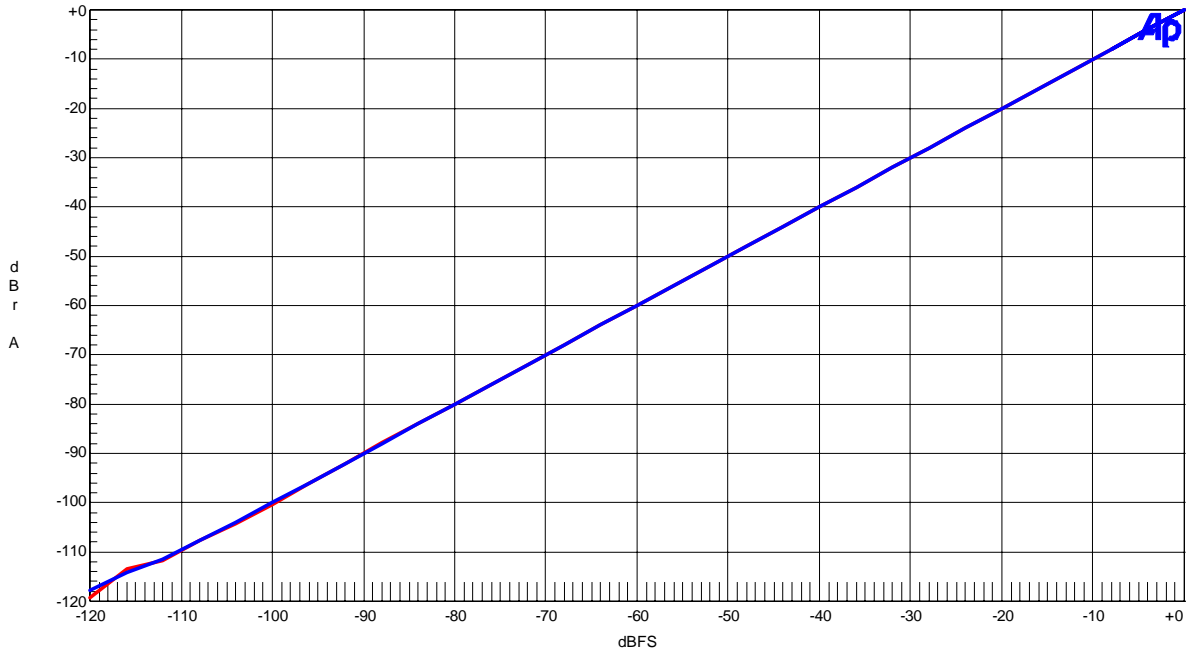


THD + N vs Input Frequency (Input=0dBFS)

(DAC fs=96kHz)

AKM

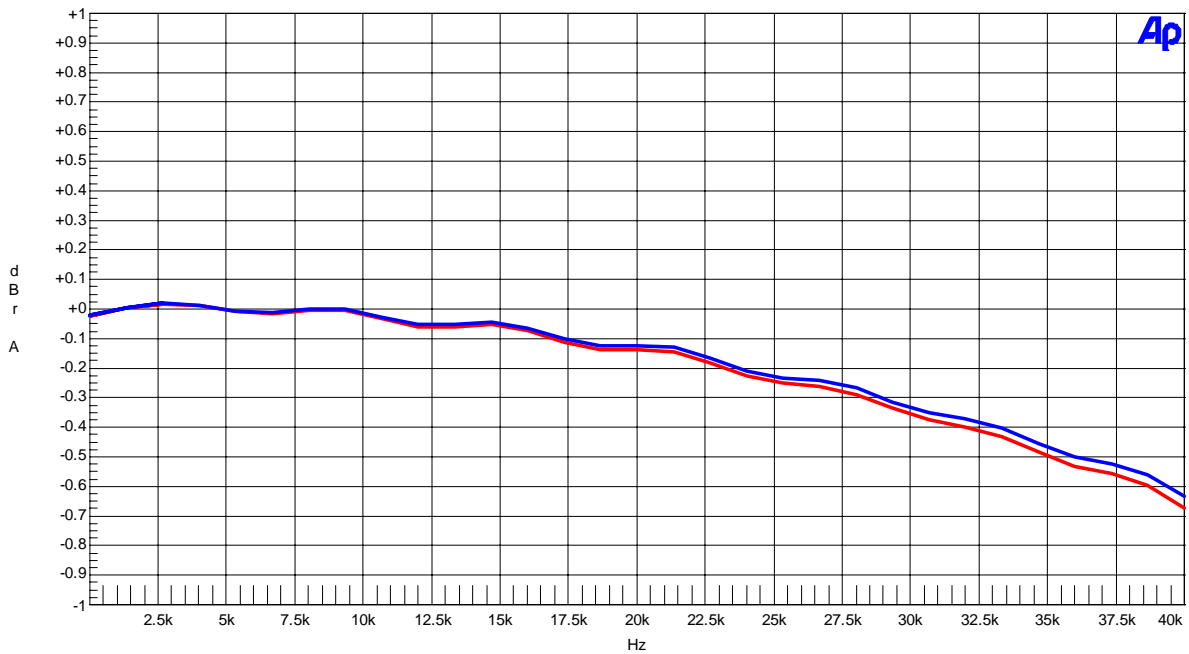
AK4628A Linearity
 AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, fin=1kHz



Linearity(fin=1kHz)

AKM

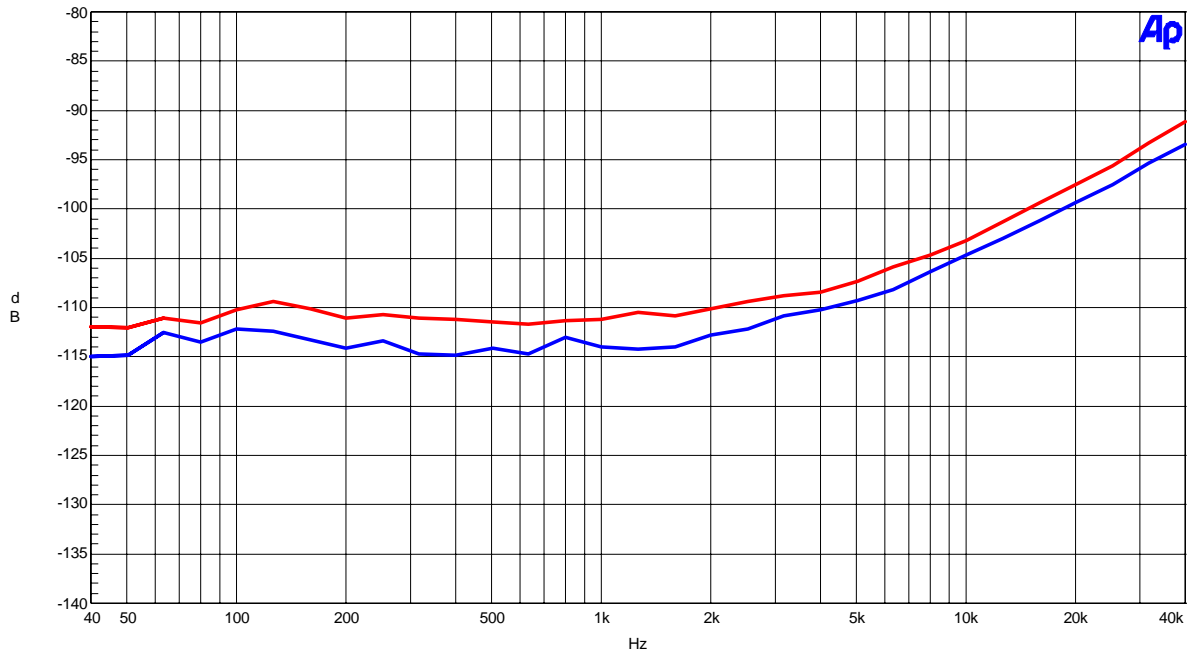
AK4628A Frequency Response
 AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input



Frequency Response(Input Level=0dBFS)
 (including external RC filter)

(DAC fs=96kHz)

AKM

AK4628A Crosstalk (Red=Lch, Blue=Rch)
AVDD=DVDD=5V, fs=96kHz, MCLK=256fs, 0dBFS input

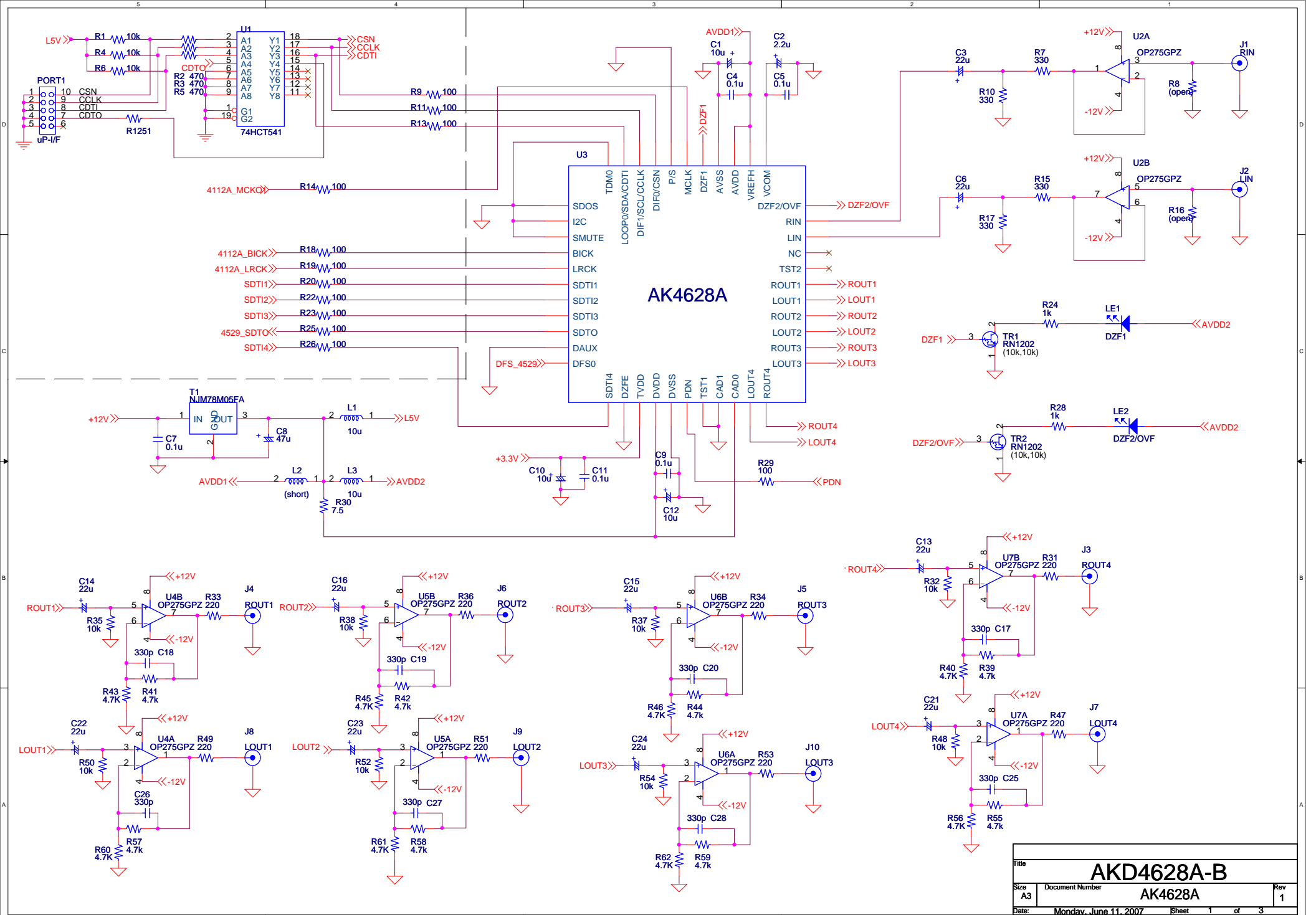
Crosstalk (Red=Rch, Blue=Lch)

| |
|-------------------------|
| Revision History |
|-------------------------|

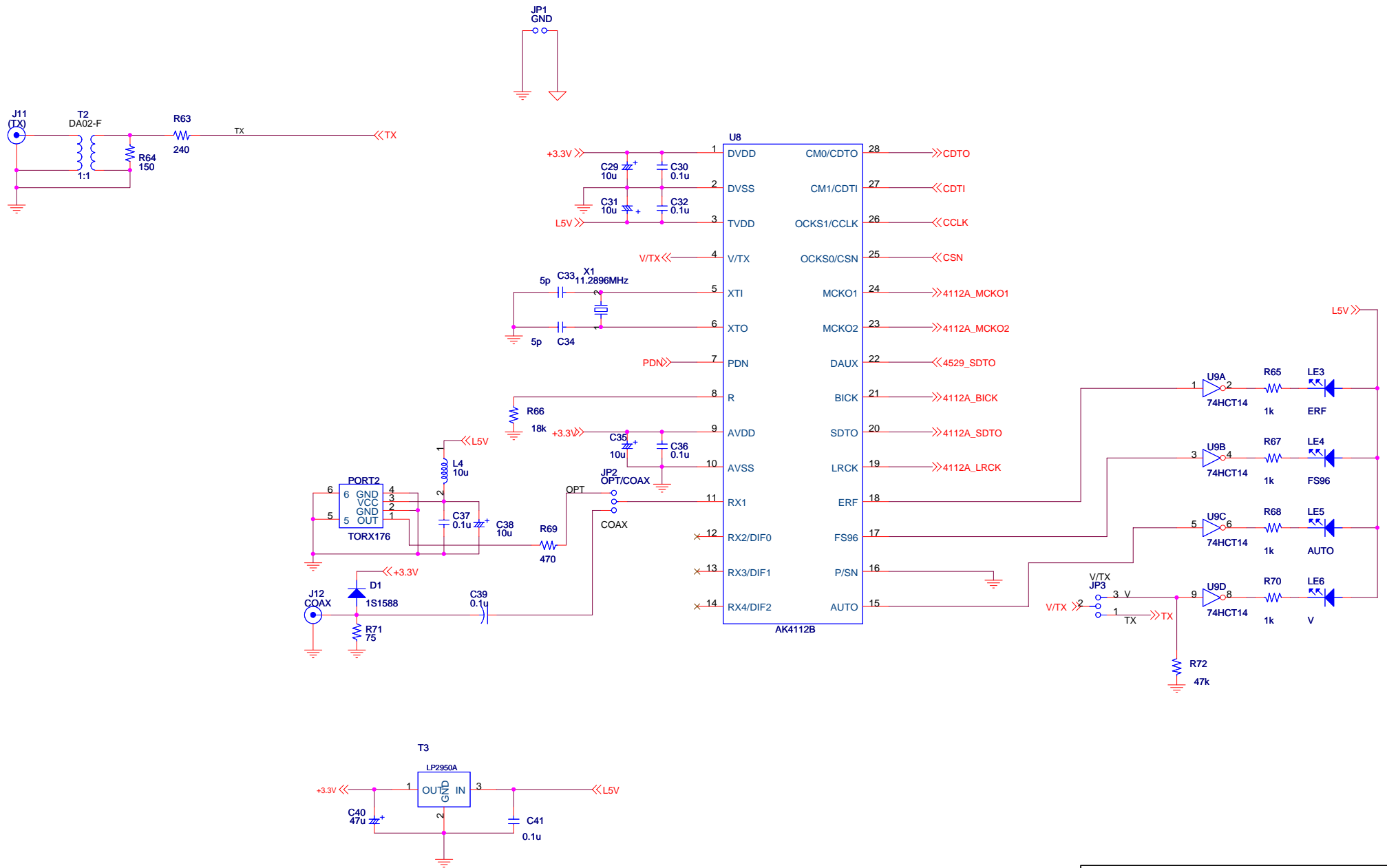
| Date (YY/MM/DD) | Manual Revision | Board Revision | Reason | Contents |
|--------------------|--------------------|-------------------|----------------|---|
| 06/08/29 | KM084900 | 0 | First Edition | |
| 07/07/03 | KM084901 | 1 | Circuit Change | U2, U4, U5, U6, U7: OPamp Change: NJM4580→OP275GPZ |

IMPORTANT NOTICE

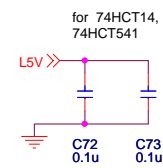
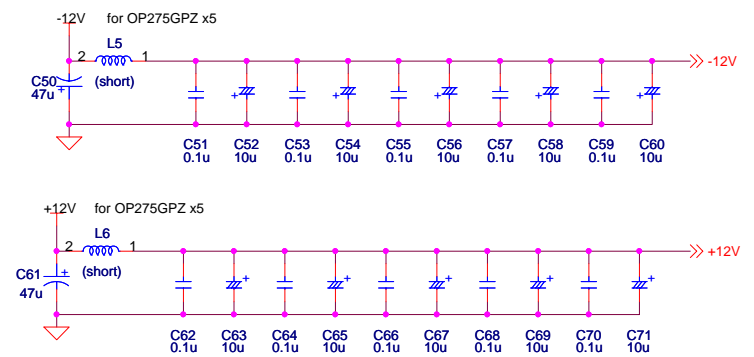
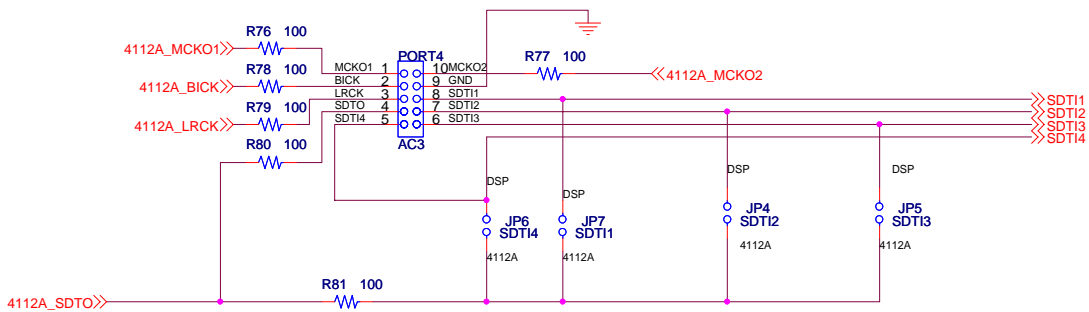
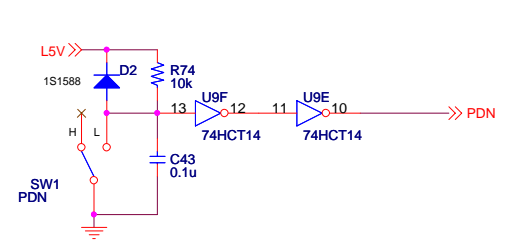
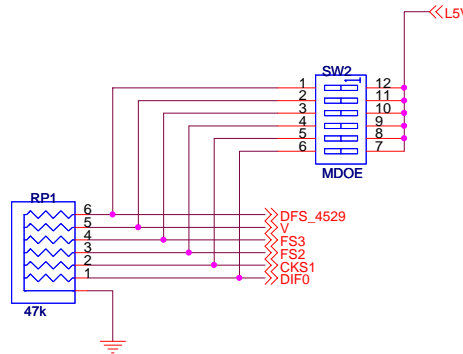
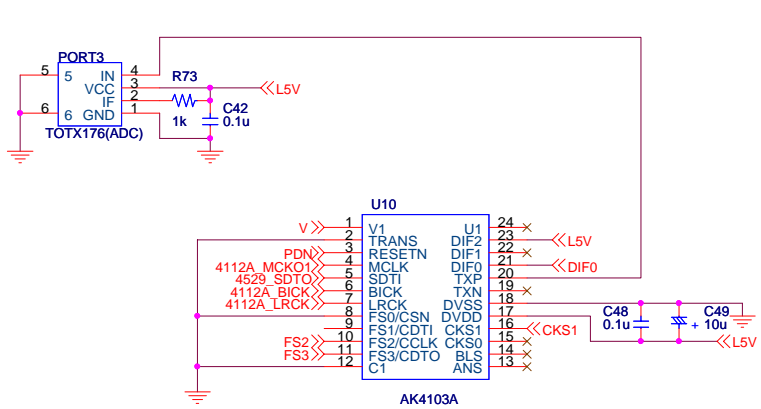
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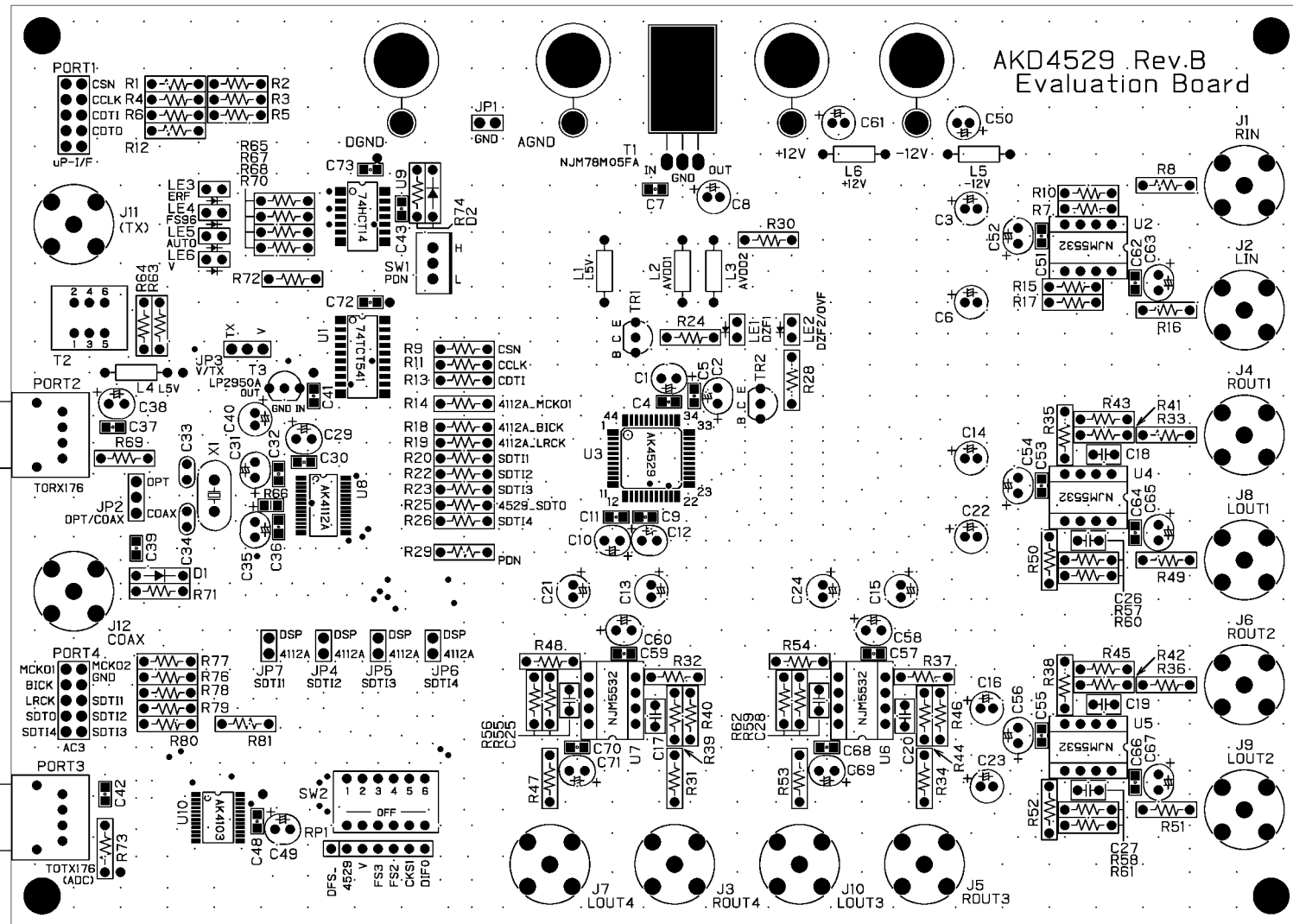
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| Title | | | AKD4628A-B | | |
| Size | Document Number | AK4628A | | | Rev |
| A3 | | | | | 1 |
| Date: | Monday, June 11, 2007 | Sheet | 1 | of | 3 |



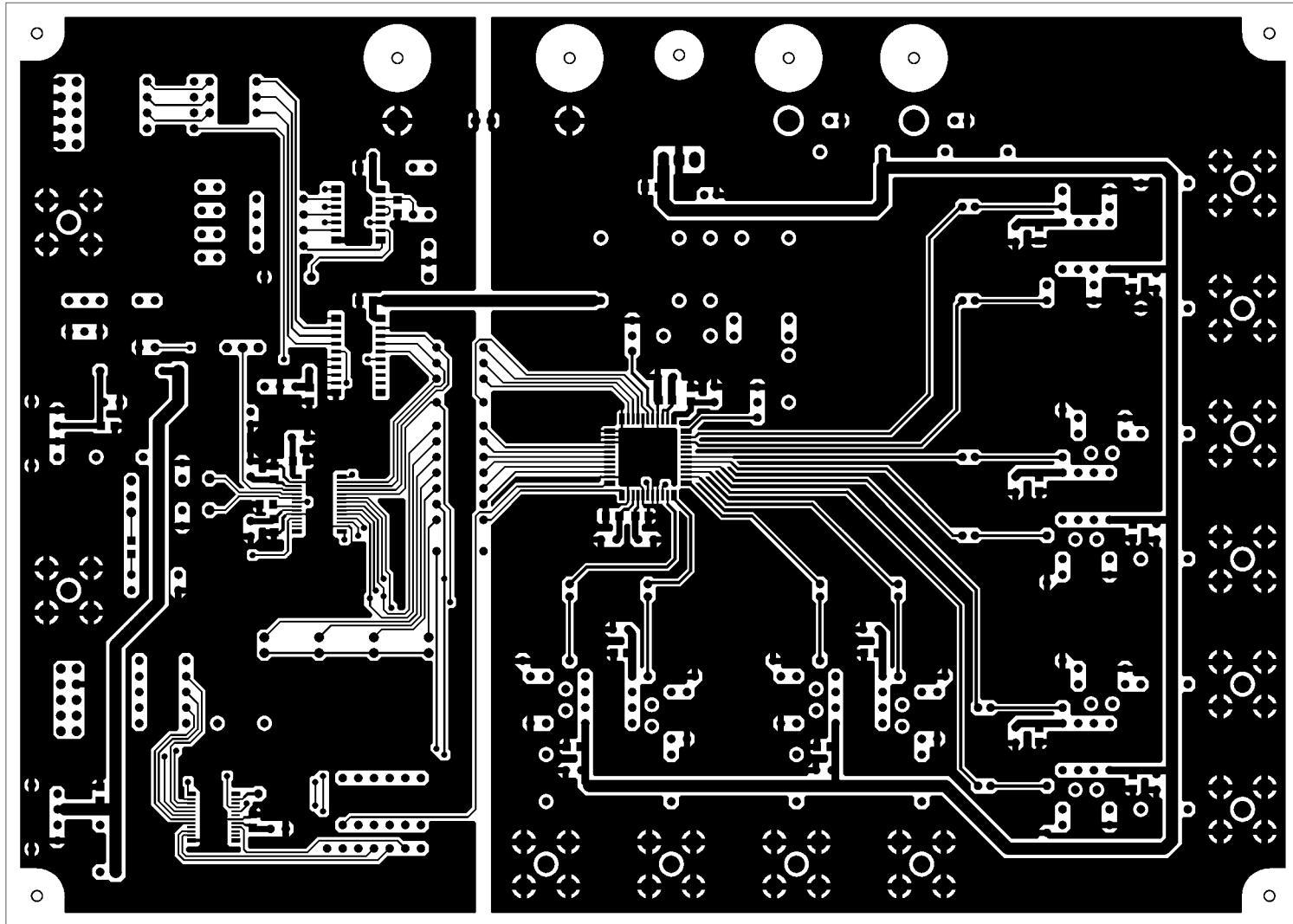
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| Title | | | AKD4628A-B | | |
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| A3 | | | | | 1 |
| Date: | Monday, June 11, 2007 | Sheet | 2 | of | 3 |



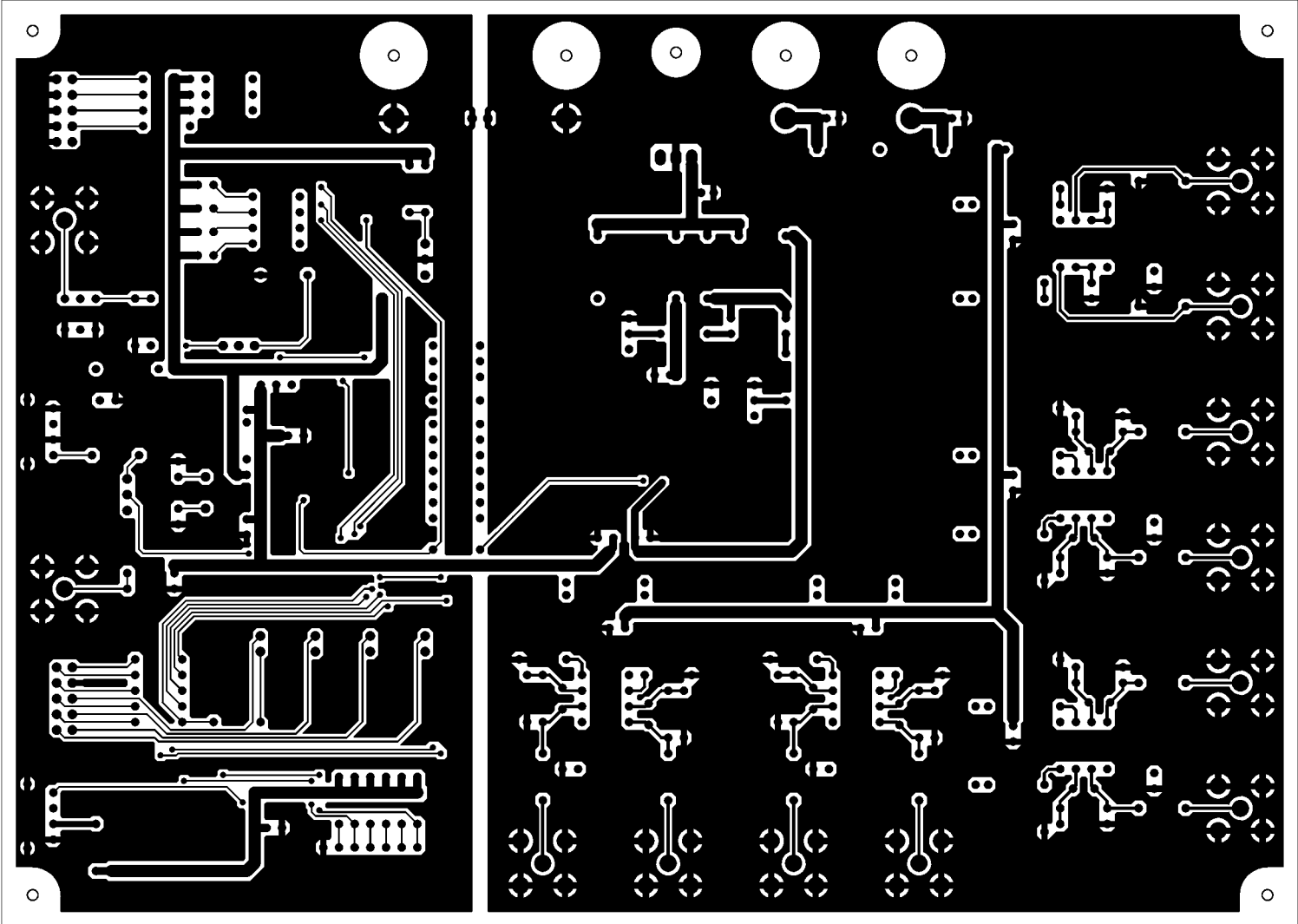
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| Size | Document Number | Interface | | | Rev |
| A3 | | | | | 1 |
| Date: | Monday, June 11, 2007 | Sheet | 3 | of | 3 |



AKD4529 Rev.B L1 SR SILK



AKD4529 Rev.B L1



AKD4258 Rev.B LS