Isolated Half-Bridge Driver with Integrated High-Side Supply

Preliminary Technical Data

ADuM5230

FEATURES

Integrated, isolated high-side supply
150mW of secondary side power
Isolated high-side and low-side outputs
100mA output source current, 300mA output sink current
High common-mode transient immunity: > 25 kV/µs
High temperature operation: 105°C
Adjustable Power Level
Wide body 16-lead SOIC package
Safety and regulatory approvals (pending):
UL recognition: 2500 V rms for 1 minute per UL1577

APPLICATIONS

MOSFET/IGBT gate drive
Plasma display modules
Motor drives
Power Supplies
Solar Panel Inverters

GENERAL DESCRIPTION

The ADuM5230[1] is an isolated half-bridge gate driver that employs Analog Devices' *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining CMOS and micro-transformer technologies, this isolation component contains an integrated dc-to-dc converter providing an isolated high-side supply. This eliminates the cost, space, and performance difficulties associated with external supply configurations such as a bootstrap circuitry. This high-side isolated supply powers not only the ADuM5230 high-side output but also any external buffer circuitry used with the ADuM5230.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM5230 offers the benefit of true, galvanic isolation between the input and each output. Each output can operate up to±700 V_P relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side may be as high as 700 V_P.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329; and other pending patents.

FUNCTIONAL BLOCK DIAGRAM

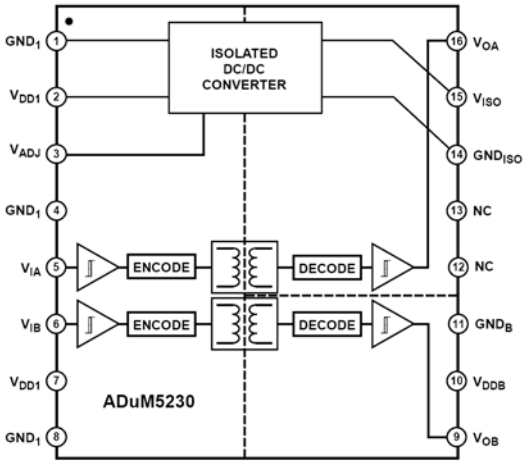


Figure 1.

Pr F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 12.0 ≤ V_{DDB} ≤ 18.0 V. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5.0 V, V_{DDB} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1(Q)}$			125	mA	I_{ISO} = 0mA, dc signal inputs, V_{ADJ} = Open
Channel B Supply Current, Quiescent	$I_{DDB(Q)}$			2	mA	
Channel A Output Supply Voltage	V_{ISO}	12	15	18	V	
At 100 kHz Switching Frequency						
Maximum Channel A Output Supply Current	$I_{ISO(max, 100)}$	10			mA	C_L = 200 pF
Input Supply Current	I_{DD1}			200	mA	I_{ISO} = $I_{ISO(max, 100)}$
Channel B Supply Current	I_{DDB}			1.8	mA	C_L = 200 pF
At 1000 kHz Switching Frequency						
Maximum Channel A Output Supply Current	$I_{ISO(max, 1000)}$	7.5			mA	C_L = 200 pF
Input Supply Current	I_{DD1}			200	mA	I_{ISO} = $I_{ISO(max, 1000)}$
Channel B Supply Current	I_{DDB}			7.5	mA	C_L = 200 pF
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB} ≤ 5.5V
Logic High Input Volatge	V_{ATH}, V_{BTH}	0.7 × V_{DD1}			V	
Logic Low Input Voltage	V_{ATL}, V_{BTL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{ISO} − 0.1, V_{DDB} − 0.1		V_{ISO}, V_{DDB}	V	I_{OA}, I_{OB} = −1 mA
Logic Low Output Voltages	V_{OAL},V_{OBL}			0.1	V	I_{OA}, I_{OB} = 1 mA
Undervoltage Lockout, V_{ISO} and V_{DDB} Supply						
Positive-Going Threshold	V_{DDBUV+}	8.0		10.1		
Negative-Going Threshold	$V_{DDBUV–}$	7.4		9.0		
Hysteresis	V_{DDBUVH}	0.3				
Undervoltage Lockout, V_{DD1} Supply						
Positive-Going Threshold	V_{DD1UV+}	3.5		4.2		
Negative-Going Threshold	$V_{DD1UV–}$	3.0		3.9		
Hysteresis	V_{DD1UVH}	0.25				
Output Short-Circuit Pulsed Current, Sourcing[1]	I_{OA}, I_{OB}	100			mA	
Output Short-Circuit Pulsed Current, Sinking[1]	I_{OA}, I_{OB}	300			mA	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 200 pF
Maximum Switching Frequency[3]		1000			kHz	C_L = 200 pF
Propagation Delay[4]	t_{PHL}, t_{PLH}			100	ns	C_L = 200 pF
Change vs. Temperature			100		ps/°C	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising or Falling Matching Edge Polarity[5]	t_{M2}			8	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising vs. Falling Opposite Edge Polarity[6]	t_{M1}			10	ns	C_L = 200 pF
Part-to-Part Matching, Rising or Falling Edges[7]				55	ns	C_L = 200 pF
Part-to-Part Matching, Rising vs. Falling Edges[8]				63	ns	C_L = 200 pF
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time (10% to 90%)	t_R			25	ns	C_L = 200 pF, I_{ISO} = 13. 5, 100 kHz switching frequency
Output Fall Time (10% to 90%)	t_F			10	ns	C_L = 200 pF, I_{ISO} = 13. 5, 100 kHz switching frequency

[1] Short-circuit duration <1 second. Average output current must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed. Operation below the minimum pulse width is strongly discouraged since in some instances pulse stretching to 1uS can occur.
[3] The maximum switching frequency is the maximum signal frequency at which the specified timing and power conversion parameters are guaranteed. Operation above the maximum frequency is strongly discouraged.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] "Channel-to-channel matching, rising or falling matching edge polarity" is the magnitude of the propagation delay difference between two channels of the same part when both inputs are either both rising or falling edges. The loads on each channel are equal.
[6] "Channel-to-channel matching, rising vs. falling opposite edge polarity" is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and one input is a falling edge. The loads on each channel are equal.
[7] Part-to-part matching, rising or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.
[8] Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		48		°C/W	

[1] The device is considered a 2-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.

REGULATORY INFORMATION

The ADuM5230 will be approved by the organization listed in Table 3.

Table 3.

UL[1] (pending)
Recognized under 1577 component recognition program, File E214100

[1] In accordance with UL1577, each ADuM5230 is proof-tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through the insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	4.5	5.5	V
Channel B Supply Voltage[1]	V_{DDB}	12	18	V
Input Signal Rise and Fall Times			1	ms
Minimum V_{DD1} power on slew rate[2]	T_{SLEW}	400		V/mS

[1] All voltages are relative to their respective ground.
[2] The ADuM5230 power supply may fail to properly initialize if V_{DD1} is applied too slowly

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Input Supply Voltage[1] (V_{DD1})	−0.5 V to +7.0 V
Channel B Supply Voltage[1] (V_{DDB})	−0.5 V to +27 V
Input Voltage[1] (V_{IA}, V_{IB})	−0.5 V to V_{DDI} + 0.5 V
Output Voltage[1] (V_{OA}, V_{OB})	−0.5 V to V_{ISO} + 0.5 V, −0.5 V to V_{DDB} + 0.5 V
Input-Output Voltage[2]	−700 V_{PEAK} to +700 V_{PEAK}
Output Differential Voltage[3]	700 V_{PEAK}
Output DC Current (I_{OA}, I_{OB})	−20 mA to +20 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] Input-to-output voltage is defined as GND_A − GND_1 or GND_B − GND_1.
[3] Output differential voltage is defined as GND_A − GND_B.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

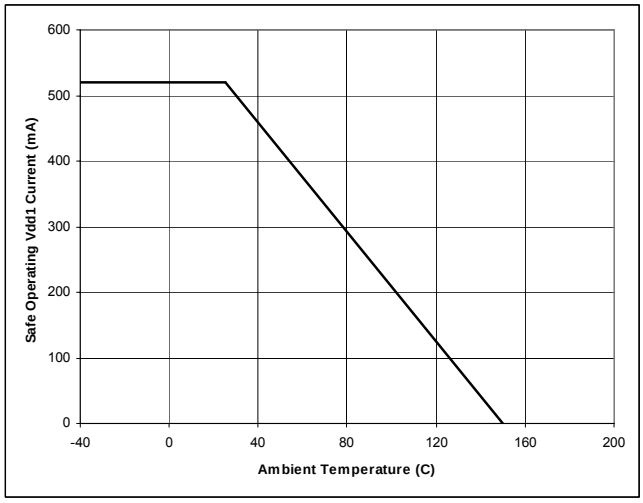


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

Table 7. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

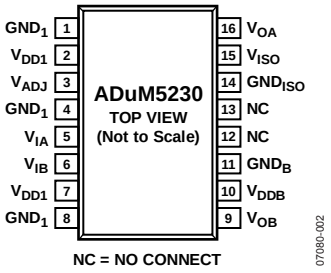


Figure 3. Pin Configuration

.Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND_1	Ground Reference for Input Logic Signals.
2	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V.
3	V_{ADJ}	Adjusts Internal DC-to-DC Converter Duty Cycle (Normally Left Unconnected).
4	GND_1	Ground Reference for Input Logic Signals.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V.
8	GND_1	Ground Reference for Input Logic Signals.
9	V_{OB}	Output B Signal.
10	V_{DDB}	Output B Supply Voltage, 12 V to 18 V.
11	GND_B	Ground Reference for Output B Signal.
12	NC	No Connect.
13	NC	No Connect.
14	GND_{ISO}	Ground Reference for Output A Signal and Isolated Output Supply Voltage.
15	V_{ISO}	Isolated Output Supply Voltage.
16	V_{OA}	Output A Signal.

Table 9. Truth Table (Positive Logic)

V_{IA}/V_{IB} Input	V_{DD1} State	V_{OA}/V_{OB} Output	Notes
H	Powered	H	
L	Powered	L	
X	Unpowered	L	Output returns to input state within 1 µs of V_{DDI} power restoration.
X	Powered	L	

TYPICAL PERFOMANCE CHARACTERISTICS

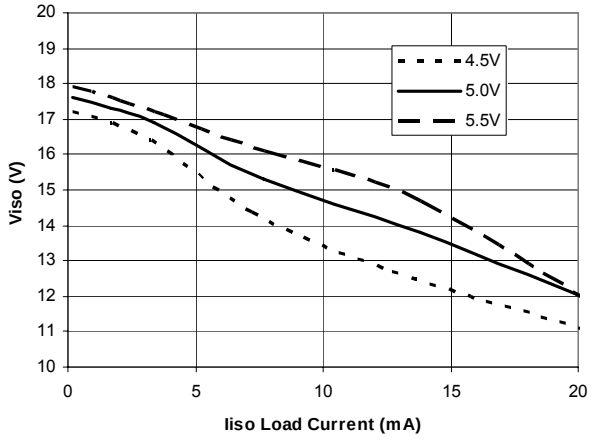


Figure 4. Typical V_{ISO} Supply Voltage vs. I_{ISO}, external load

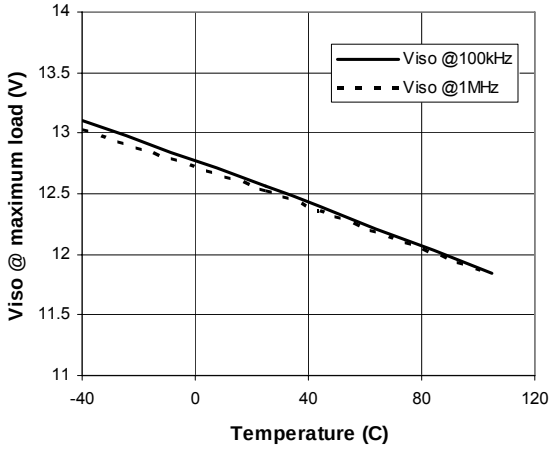


Figure 7. Typical VISO output voltage at maximum combined load over temperature

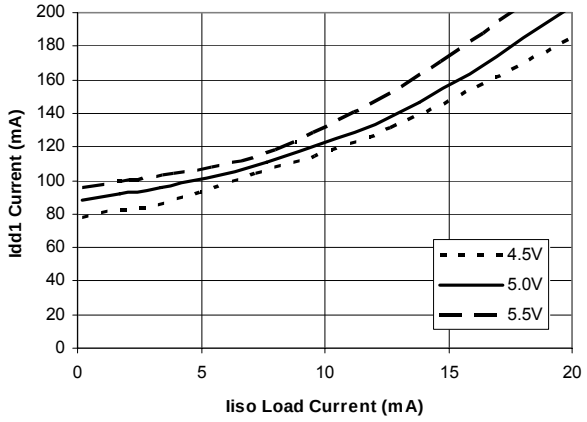


Figure 5. Typical V_{DD1} supply Current vs.V_{ISO} external load

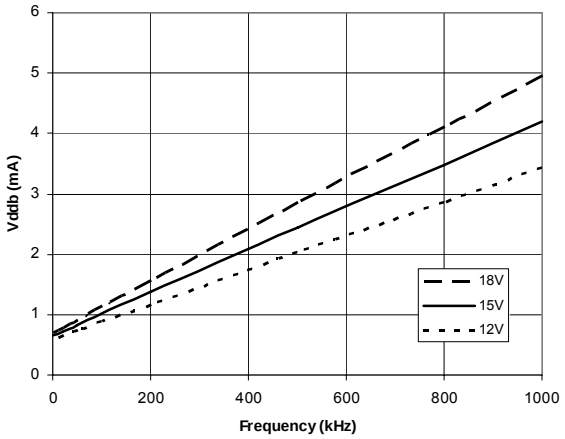


Figure 8. Typical V_{OX} output power consumption, CL = 200pF

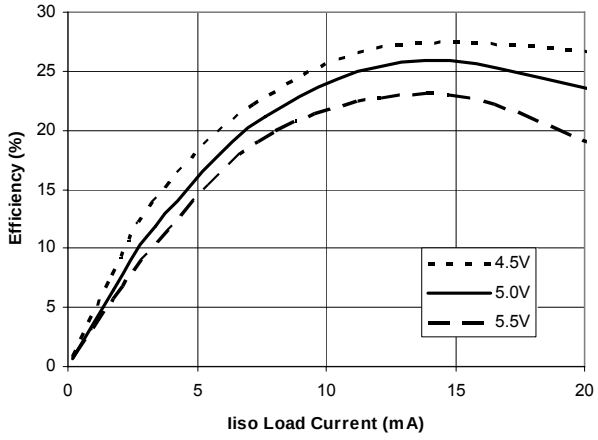


Figure 6. Typical V_{ISO} supply Efficiency vs. external load

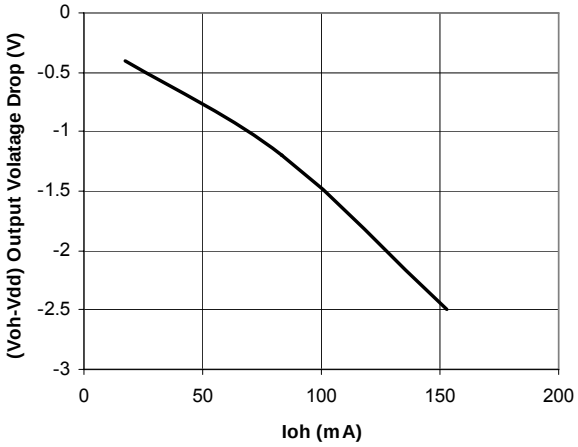


Figure 9. Typical V_{OH} vs. I_{OH}(V_{DD1}=5V, V_{DDB}, V_{ISO} = 12-18V)

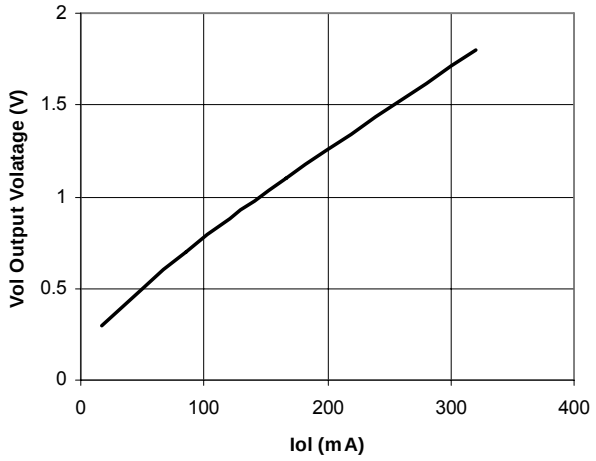


Figure 10. Typical V_{OL} vs. I_{OL}(V_{DD1}=5V, V_{DDB}, V_{ISO} = 12-18V)

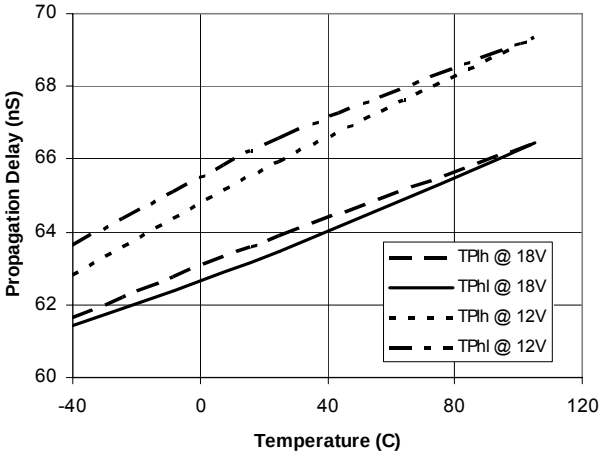


Figure 11. Typical VISO supply Efficiency vs. load

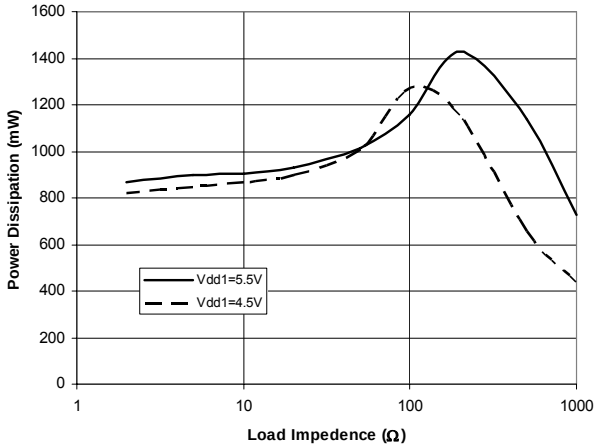


Figure 12. Power Dissipation vs. Load Impedance for Fault Conditions

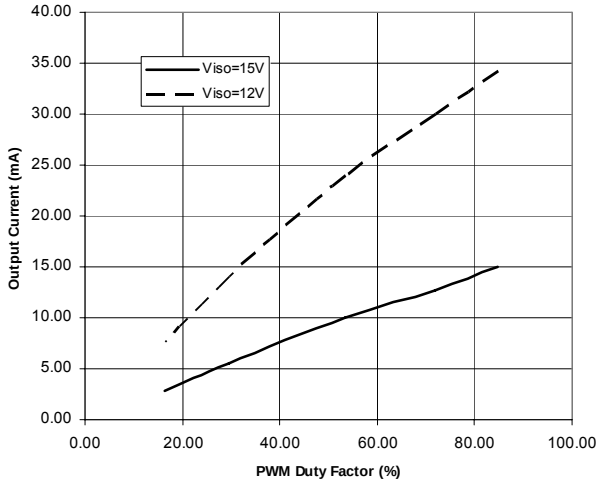


Figure 13. Current Available at the Output vs. PWM Duty Factor for V_{DD1}=5V

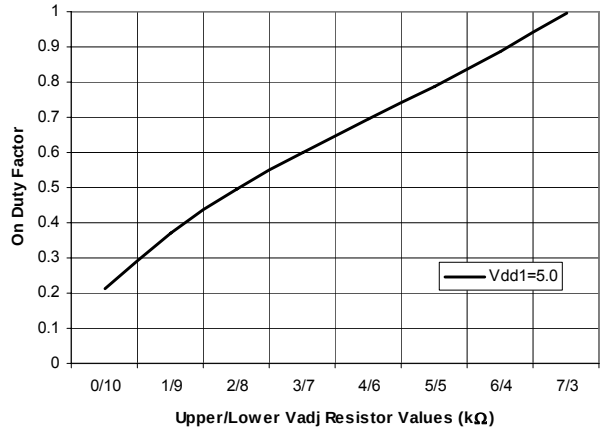


Figure 14. Upper / Lower V_{ADJ} Voltage Divider Resistor Values to Determine PWM Duty Factor for V_{DD1}=5V

APPLICATION INFORMATION

THEORY OF OPERATION

The DC/DC converter section of the ADuM5230 works on principles that are common to most modern power supply designs. It is implemented as an open loop PWM controller, which sets the power level being transferred to the secondary. V_{DD1} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. On the secondary side power is rectified to a DC voltage. The voltage is then clamped to approximately 18V and provided to the secondary side V_{OA} data channel and to the V_{ISO} pin for external use. The output voltage is unregulated and varies with load.

The PWM duty cycle is set by internal bias elements, but can be controlled externally through the V_{ADJ} pin with and external resistor network. This feature allows the user to boost the available power at the secondary, or reduce excess power if it is not required for the application. Please refer to the Power Consumption section.

Under voltage lockouts are provided on the V_{DD1}, V_{DDB}, and V_{ISO} supply lines to interlock the data channels from low supply voltages.

PC BOARD LAYOUT

The ADuM5230 digital isolator with a 150mW *iso*Power integrated DC/DC converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (Figure 15). The power supply section of the ADuM5230 uses a very high oscillator frequency to efficiently pass power through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance high frequency capacitor, ripple suppression and proper regulation require a large value capacitor. These are most conveniently connected between Pins 1 and 2 for V_{DD1} and between Pins 15 and 14 for V_{ISO}. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0. 1 µF, and 10µF. It is strongly recommended that a very low inductance ceramic or equivalent capacitor be used for the smaller value. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing with noise suppression and stiffening capacitors is recommended between Pins 1 and 2, a bypass capacitor is recommended between pins 7 and 8. Bypassing with noise suppression and stiffening capacitors is recommended between Pins 14 and 15.

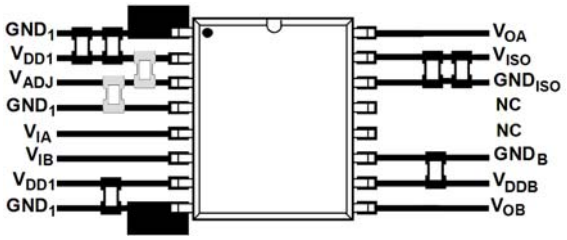


Figure 15. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, specified in Table 6 leading to latch-up and/or permanent damage.

The ADuM5230 is a power device that dissipates about 1W of power when fully loaded and running at maximum speed. Since it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device will be used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 15 shows enlarged pads for pins 1 and 8. Multiple vias should be implemented from the pad to the ground plane. This will significantly reduce the temperatures inside of the chip. The dimensions of the expanded pads are left to discretion of the designer and the available board space.

THERMAL ANALYSIS

The ADuM5230 parts consist of several internal die, attached to a three lead frames with three die attach paddles. For the purposes of thermal analysis it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} from Table 2. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4 layer board with fine width traces and still air. Under normal operating conditions the ADuM5230 will operate at full load across the full temperature range without derating the output current. However, following the recommendations in the PC Board Layout section will decrease the thermal resistance to the PCB allowing increased thermal margin it high ambient temperatures.

Under output short circuit conditions as shown in Figure 12, the package power dissipation is within safe operating limits, however, if the load is in the 100ohm range, power dissipation is high enough to cause thermal damage if the ambient temperature is above 80C. Care should be taken to avoid excessive non-short loads if the part is to be operated at high temperatures.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

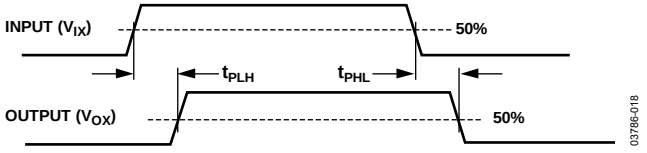


Figure 16. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM5230 component.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 9) by the watchdog timer circuit.

The limitation on the ADuM5230's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM5230 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 17.

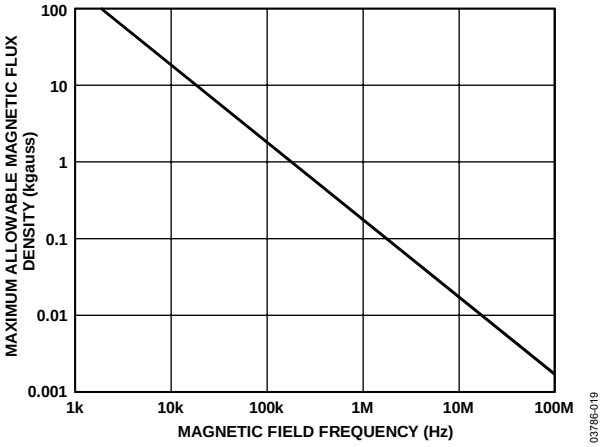


Figure 17. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM5230 transformers. Figure 18 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM5230 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM5230 to affect the component's operation.

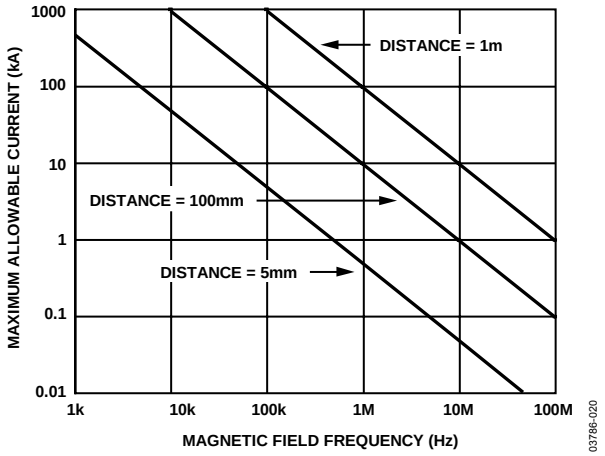


Figure 18. Maximum Allowable Current for Various Current-to-ADuM5230 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The power converter in the ADuM5230 provides 13mA of power to the secondary by default. Output power is shared between the output data channel V_{OA} and V_{ISO} for off chip use. The power consumption of V_{OA} varies with frequency and is presented in Figure 8.

INCREASING AND DECREASING AVAILABLE POWER

The V_{ADJ} pin is used to increase or decrease the available power at the V_{ISO} pin. This allows the increase the V_{ISO} voltage for a given load or to increase the maximum V_{ISO} load. On the other hand, power can also be reduced when it is not required at the output, lowering the quiescent current and saving power.

Power adjustment is accomplished by adding a voltage divider between V_{ADJ}, V_{DD1} and GND as shown in Figure 25. Under normal operation, this pin is left open allowing the internal bias network to set the duty factor of the internal PWM. If the V_{ADJ} pin is connected via a resistor divider, a duty factor other than the default can be chosen. The relationship between the duty factor of the internal PWM and the available power under load is shown in Figure 13. When the desired duty factor is chosen, the values of the upper and lower divider resistors can be chosen from Figure 14 which assumes a 10kΩ total divider resistance.

COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM,\,linear} = (\Delta V/\Delta t)\,t$$

where ΔV/Δt is the slope of the transient shown in Figure 22 and Figure 23.

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

The ability of the ADuM5230 to operate correctly in the presence of linear transients is characterized by the data in Figure 19. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM5230 can tolerate without an operational error. This data shows a higher level of robustness than what is shown in Table 5 because the transient immunity values obtained in Table 5 use measured data and apply allowances for measurement error and margin.

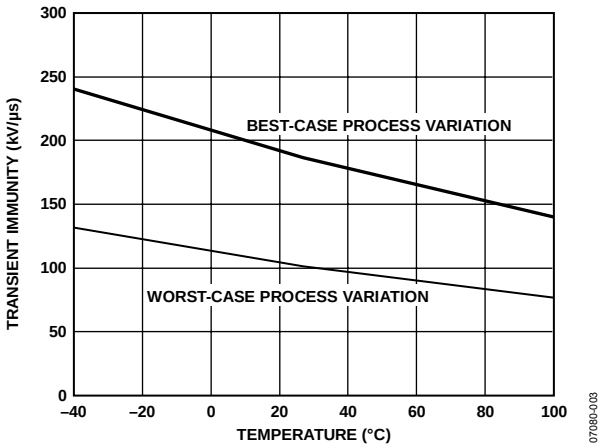


Figure 19. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM,\,sinusoidal} = V_0 \sin(2\pi f t)$$

where:
V_0 is the magnitude of the sinusoidal.
f is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f\,V_0$$

The ability of the ADuM5230 to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 20 and Figure 21. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f\,V_0$) that the ADuM5230 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 5 because measurements to obtain such values have not been possible.

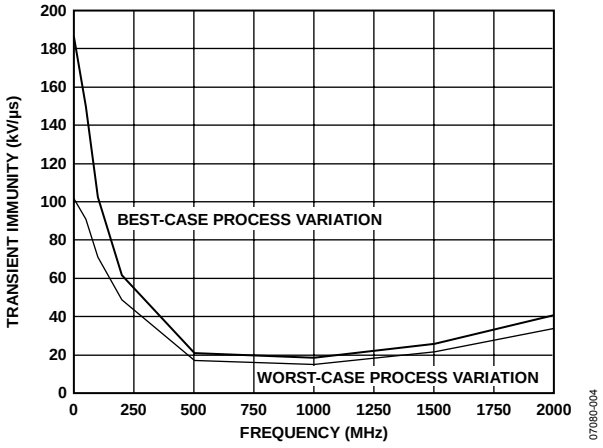


Figure 20. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

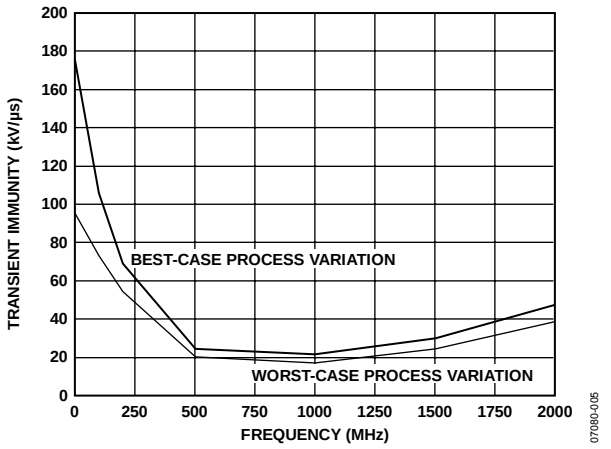


Figure 21. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

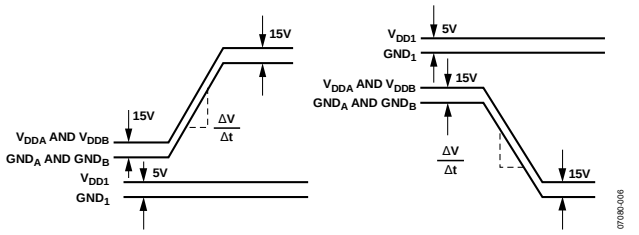


Figure 22. Common-Mode Transient Immunity Waveforms—Input to Output

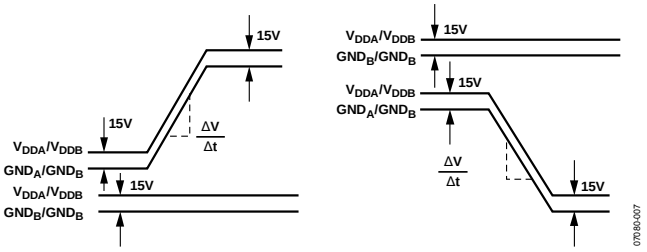


Figure 23. Common-Mode Transient Immunity Waveforms—Between Outputs

Figure 24. Transient Immunity Waveforms—Output Supplies

TYPICAL APPLICATION USAGE

The ADuM5230 is intended for driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these application, users can implement a buffer configuration with the ADuM5230, as shown in Figure 25. In many cases, the buffer configuration is the least expensive options and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to fit the needs of the application.

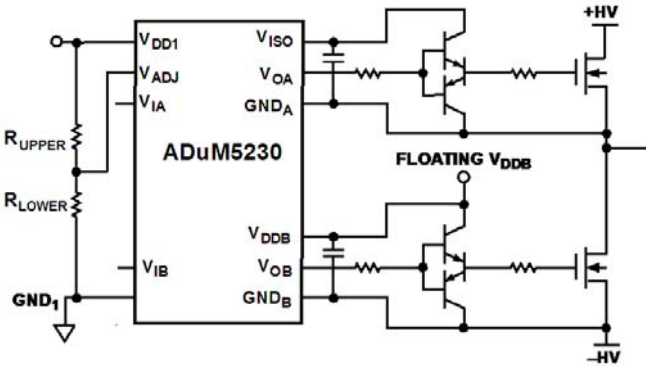


Figure 25.Application Circuit

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5230.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. Table 7 summarizes the peak voltages for 50 years of service life for a bipolar ac operating condition and the maximum Analog Devices recommended working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM5230 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 26, Figure 27, and Figure 28 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 7 can be applied while maintaining the 50-year minimum lifetime provided the voltage

conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 27 or Figure 28 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 7. Note that the voltage presented in Figure 27 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

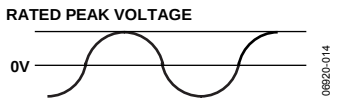


Figure 26. Bipolar AC Waveform

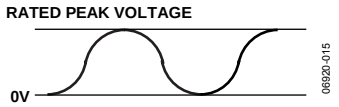


Figure 27. Unipolar AC Waveform

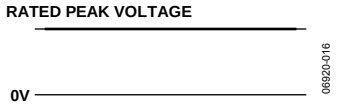
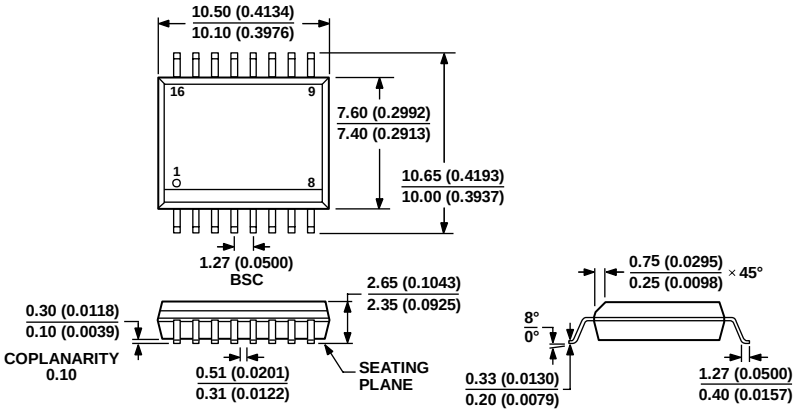


Figure 28. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 6. 16-Lead Standard Small Outline Package [SOIC_W]—Wide Body (RW-16)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	No. of Channels	Output Peak Current (A)[1]	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM5230ARWZ[2]	2	0.1/0.3	15	–40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5230ARWZ-RL[2]	2	0.1/0.3	15	–40°C to +105°C	16-Lead SOIC_W, 13-inch Tape and Reel Option (1,000 Units)	RW-16

[1] Sourcing/sinking.
[2] Z = RoHS Compliant Part.

PR07080-0-3/08(PrF)