GENERAL DESCRIPTION

This product is SD Digital-To-Analog Converter for digital audio System (CDP). The product contains Serial-to-Parallel Converter and Compensation Filter, Digital Volume Attenuator by the MICOM Interface, De-Emphasis Filter, FIR filter, Sinc Filter, digital sigma-delta modulator, analog postfilter, AIF (Anti-Image-Filter). The normal input and output channels provides 90dB SNR (Signal to Noise Ratio) over in band (20kHz).

The product employs the 1bit 4th-order sigma-delta architecture with 16bit resolution, over sampling of 64X. And analog postfilter with low clock sensitivity and linear phase, filters the shaping-nosie and outputs analog voltage with high resolution. An on-chip reference voltage is included to allow single supply operations.

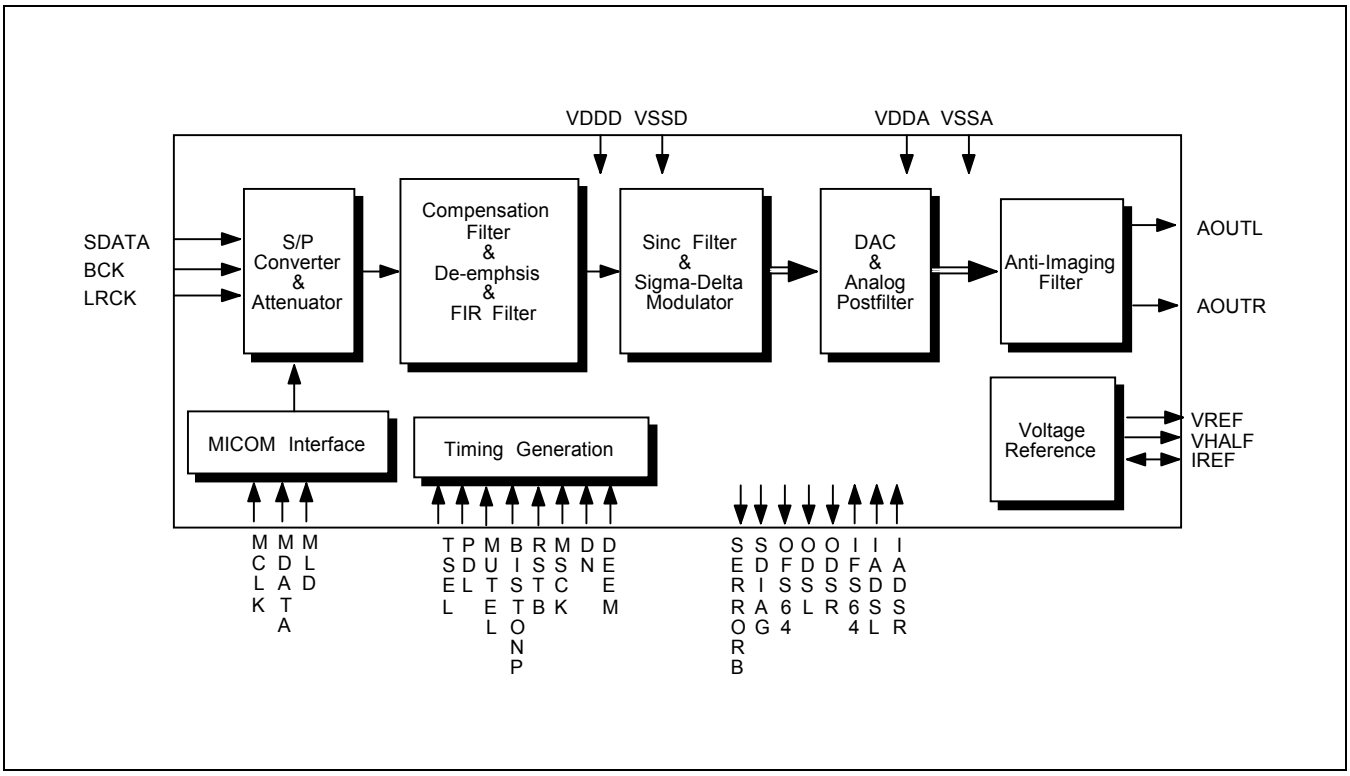
FEATURES

— 16bit SD Digital-To-Analog Converter
— On-Chip Analog Postfilter
— Filtered Line-Level Outputs, Linear Phase Filtering
— On-Chip Voltage Reference
— 90dB SNR
— Sampling Rate 44.1kHz
— Input Rate 1Fs or 2Fs by Normal Mode/Double Mode Selection
— Zero Input Detection Mute
— On-Chip Compensation Filter
— Input Volume Attenuator by the MICOM Interface
— On-Chip De-Emphasis Filter
— On-Chip 4 times oversampling Digital Filter
— Low Clock Jitter Sensitivity
— Single 3.3V~2.5V Power Supply

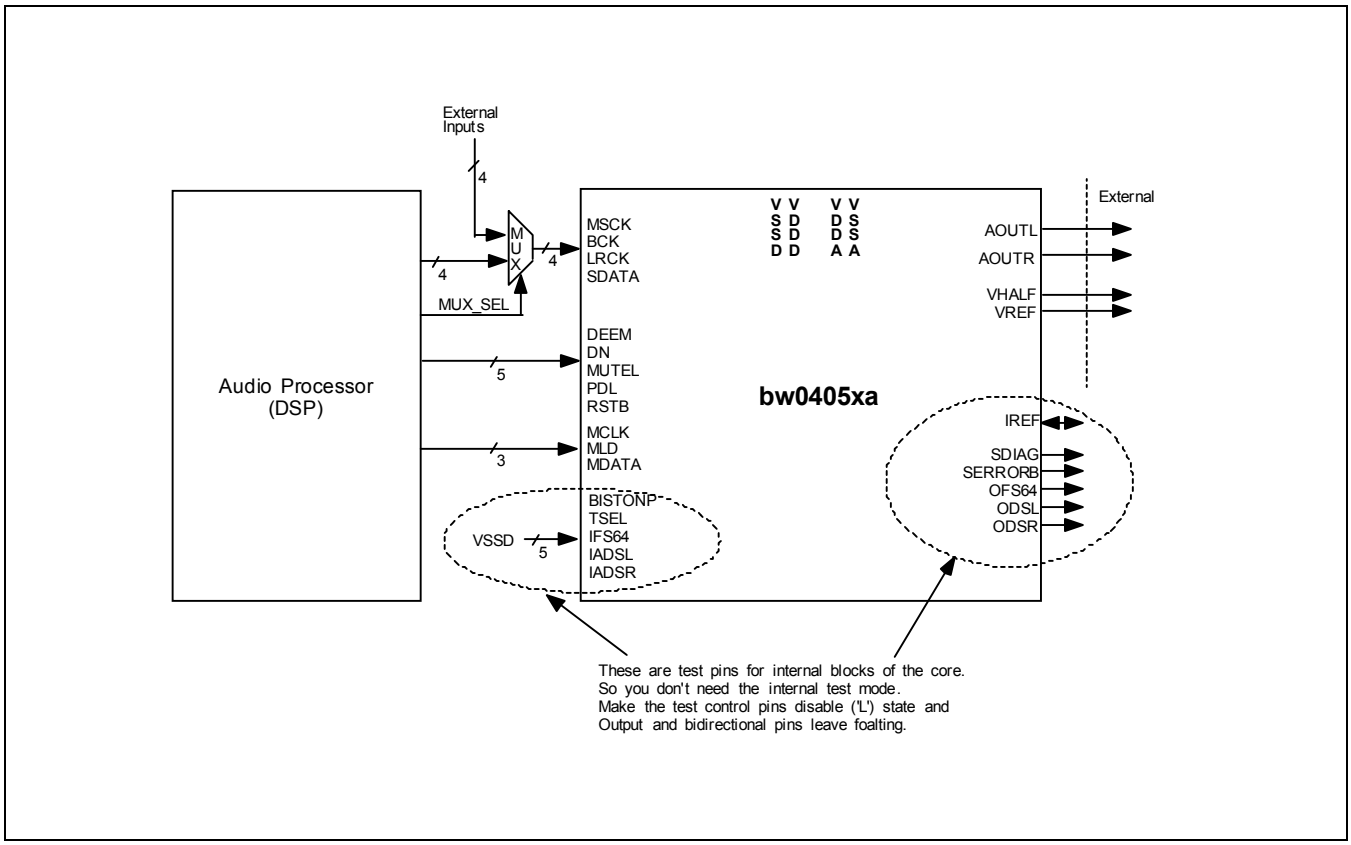
APPLICATIONS

CD Player, Portable CD Player, CD-ROM, Video-CD, Mini-Disk, DVD etc

FUNCTIONAL BLOCK DIAGRAM



EMBEDDED CORE BLOCK DIAGRAM



EMBEDDED CORE USER GUIDE

— Digital serial data input and clock input refer to digital input format.

— Digital control pins inform refer to pin description.

— Micom I/F pin inform refer to micom interface.

— External application of analog output pins refer to application circuit.

— If you want to test only embedded analog core block (Sigma-Delta DAC), you can do it just adding the 4 pins to supply digital serial input data (LRCK, BCK, SDATA, MSCK) and MUX block.

— Analog power(VDDA,VSSA) and digital power(VDDD, VSSD) should be seperated.

— Two pads should be dedicated to analog power(VDDA, VSSA)

— If you need not use test mode for the testability of internal core block, you make internal core block test pins disable state. (Test Input pins are 'L' state and Test output, bidirection pins leave floating)

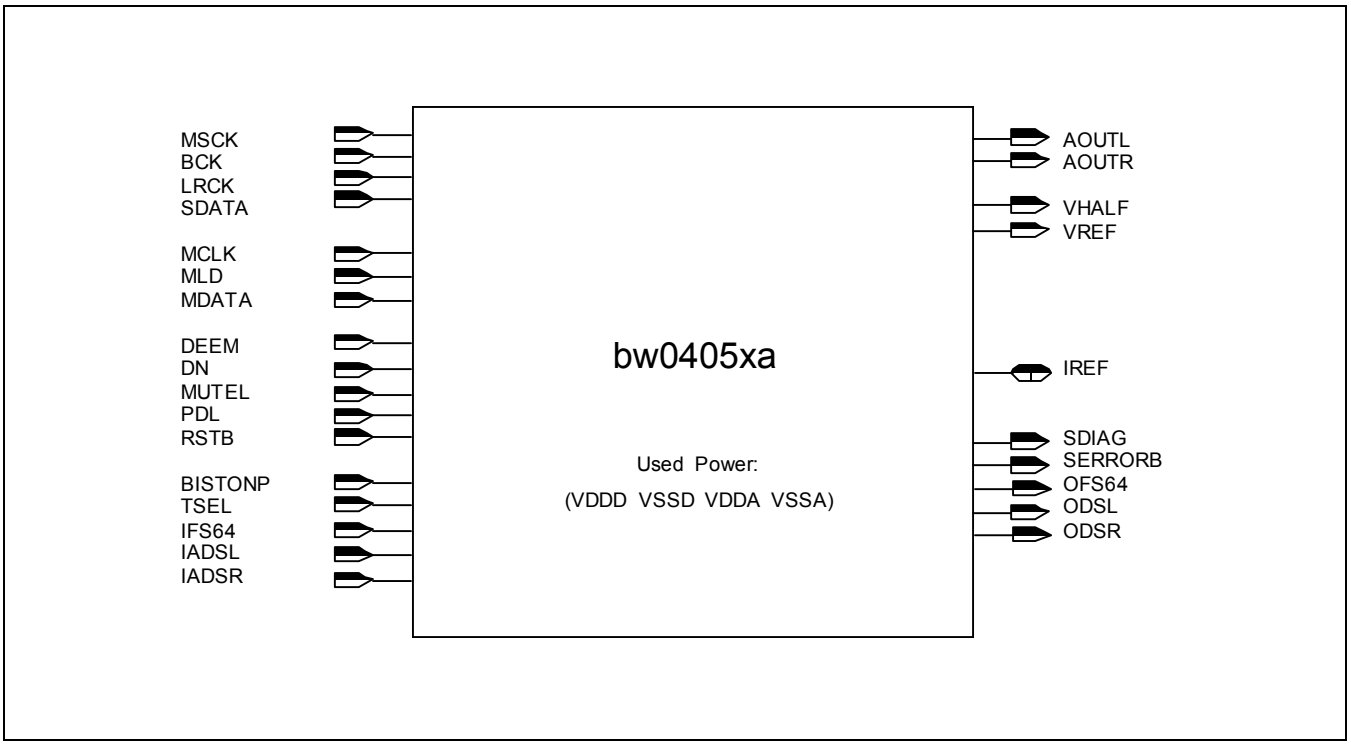
CORE PIN DESCRIPTION

Symbol	I/O Type	I/O Pad	Description
Power Supply Pins			
VDDD	DP	vdd3t_bb	Digital Supply
VSSD	DG	vsst_bb	Digital Ground
VDDA	AP	vdd3t_bb	Analog Supply
VSSA	AG	vsst_bb	Analog Ground
Digital Pins			
MSCK	DI	picc_bb	Master Clock Input. 384Fs Clock
BCK	DI	picc_bb	Bit Clock Input. (32Fs or 64Fs)
LRCK	DI	picc_bb	Sample Rate Clock Input. (Fs or 2Fs)
SDATA	DI	picc_bb	Serial Digital Input
MCLK	DI	picc_bb	Micom Interface Clock Input
MLD	DI	picc_bb	Micom Interface Command load Input (When low,load)
MDATA	DI	picc_bb	Micom Interface Command Data Input
DEEM	DI	picc_bb	De-Emphasis On/Off. "H" is enabled. "L" is disabled.
DN	DI	picc_bb	Input Rate Select. High is Double(2Fs) Mode, Low is Normal(Fs) Mode.
MUTEL	DI	picc_bb	Analog Output Mute. "L" enabled
PDL	DI	picc_bb	Power Down. "L" enabled
RSTB	DI	picc_bb	Reset Input. "L" Enabled
Analog Pins			
AOUTL	AO	poa_bb	Analog Output for L-CH
AOUTR	AO	poa_bb	Analog Output for R-CH
VHALF	AO	poar50_bb	Reference Voltage Output for Bypass
VREF	AO	poar50_bb	Reference Voltage Output for Bypass
Core Internal Block Test Pins			
BISTONP	DI	picc_bb	Memory Bist Test Mode. "H" enabled
TSEL	DI	picc_bb	Test pin for Analog Postfilter Input Selection
IFS64	DI	picc_bb	64X Sampling Clock Input for Analog Postfilter (When TSEL=H)
IADSL	DI	picc_bb	Inputs for Analog Postfilter of L-CH (When TSEL=H)
IADSR	DI	picc_bb	Inputs for Analog Postfilter of R-CH (When TSEL=H)
SDIAG	DO	pot2_bb	Test Output pin for embeded memory BIST (BIST_ON="H")
SERRORB	DO	pot2_bb	Test Output Pin for Embeded memory BIST (BIST_ON="H")
OFS64	DO	pot2_bb	64X Sampling Clock output for Digital sigma-delta Modulator
ODSL	DO	pot2_bb	L-CH Output for Digital sigma-delta Modulator.
ODSR	DO	pot2_bb	R-CH Output for Digital sigma-delta Modulator.
IREF	AB	poa_bb	Test Pin for Analog Supply Current

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

CORE CONFIGURTION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Values	Unit
Supply Voltage	VDDD,VDDA	-0.15 ~ 3.8	V
Voltage on Any Digital Pin	Vin	VSS-0.15 to VDD+0.15	V
Storage Temperature Range	Tstg	-45 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Charateristics	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	VDDD VDDA	2.3	2.5	3.6	V
Operating Temp.	Topr	0	25	70	°C

ELECTRICAL CHARACTERISTICS

(VDDD,VDDA=2.5V, Temp=25°C, Fs=44.1kHz, Signal Frequency=20-20kHz, Cload of AoutL, AoutR=10pF)

Parameter	Min	Typ	Max	Units
Resolution		16		bits
SNR[1]	80	90		dB
THD[2]		0.005	0.01	%
SND(THD+Noise)[3]	76	80		dB
Dynamic Range[4]	85	90		dB
Reference Voltage Ouput		0.5 x VDDA		V
Frequency Responce		± 0.1	± 0.5	dB
Analog Output				
Voltage Range		0.75 x VDDA		Vpp
Load Impedance	10k			Ω
Digital Filter				
Pass Band Ripple		± 0.0072		dB
Stop Band Attenuation		62.7		dB
Pass Band		0.45		Fs
Power Supply				
Analog Current		2	3	mA
Digital Current		5	6	mA
Power Dissipation		17.5	22.5	mW
Power Down Current		0.1	1	mA

NOTES:

1. 1kHz 0dB Sinewave Input, EIAJ
2. 1kHz -3dB Sinewave Input
3. 1kHz 0dB Sinewave Input, (Not EIAJ)
4. 1kHz -60dB Sinewve Input, and then measured data + 60dB

AC TIMING CHARACTERISTICS

(VDDD=2.5V, VSSD=0V, Temp=25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
MSCK Frequency	Fmck	–	16.9344	–	MHz
BCK Frequency (Normal/Doube Mode)	Fbck		1.4112 / 2.8224	–	MHz
MSCK Rising and LRCK Edge Dealay	Tmld	10	–	–	ns
MSCK Risng and LRCK Edge Setup Time	Tmlst	10	–	–	ns
BCK Rising and LRCK Edge Dealay	Tbld	10	–	–	ns
BCK Risng and LRCK Edge Setup Time	Tblst	10	–	–	ns
SDATA and BCK Rising Setup Time	Tsbst	10	–	–	ns
BCK Ring and SDATA Hold Time	Tbsht	10	–	–	ns

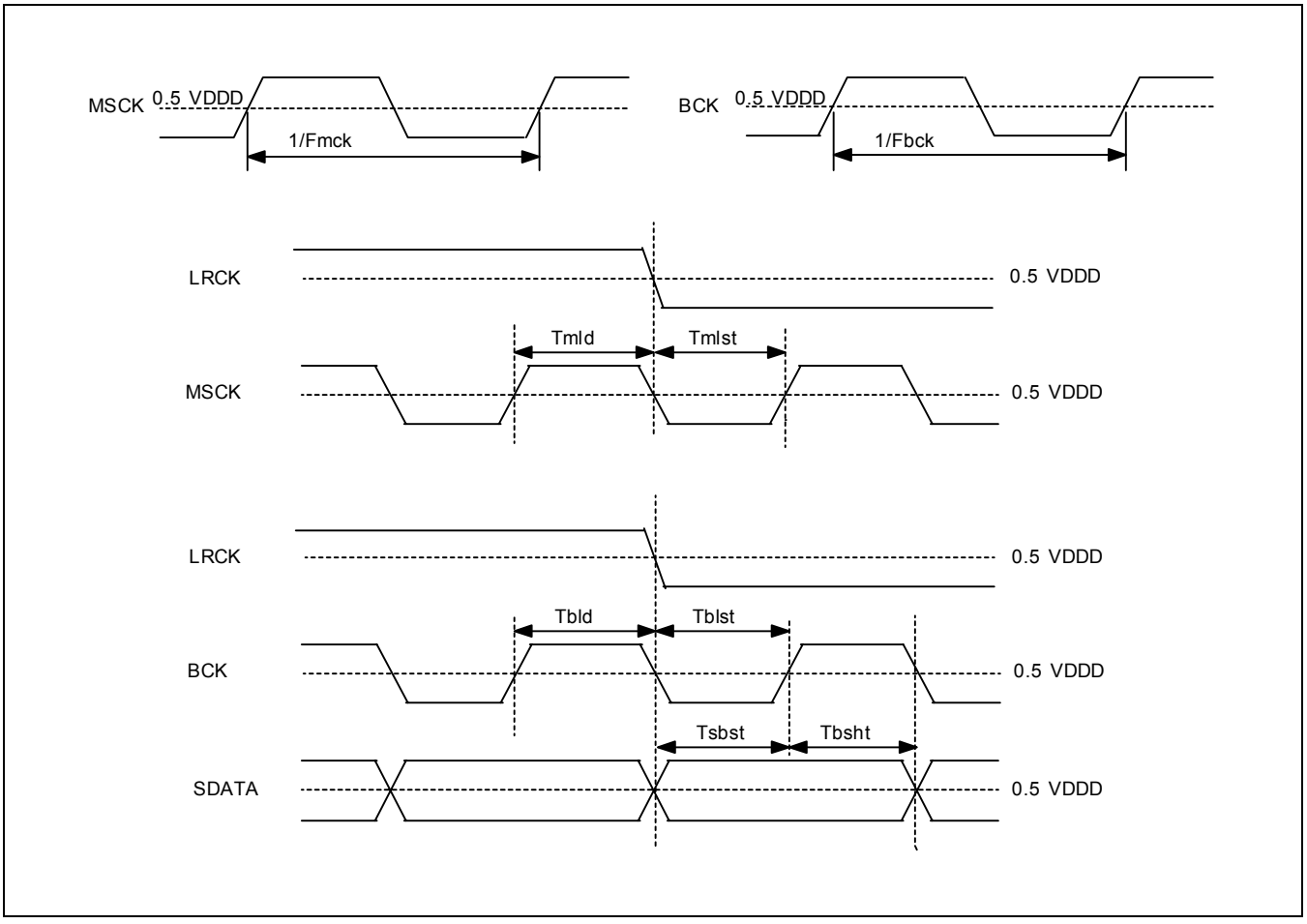


Figure 1. Timing Chart

SAMSUNG ELECTRONICS

CLOCK INPUT AND SERIAL INPUT DATA INFORM (FS=44.1KHZ)

DN is normal and double mode selection control pin. Refer to the following table for clock input inform.

Table 1. Input Clock Informs

	Normal Mode (DN='Low')	Double Mode (DN='High')
LRCK	44.1kHz	88.2kHz
MSCK	16.9344MHz	16.9344MHz
BCK	1.4112MHz	2.8224MHz

Serial input data (SDATA) is MSB fisrt at falling edge triggered of BCK.

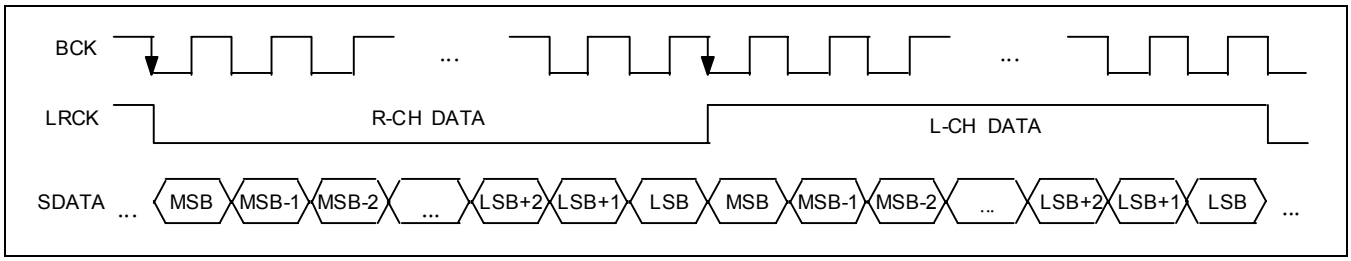


Figure 2. Digital Input Data Format

MICOM INTERFACE (DIGITAL ATTENUATION)

This product can do the function of digital attenuation whenever it receives thd MDATA, MLD, MCLK signals form the MICOM. When the 14-bit serial data is applied to the MDATA, MCLK, MLD in the form of Fig3, according to the data digital attenuation is accomplished. The lower eight LSBs should be 5D(LSB First Format-Hex) and according to the upper 6 bits(LSB First Format-Bin) the attenuation level can be adjusted. (see Table1) When RSTB is low state the latch circuitry for setting the attenuation level becomes reset and the attenuation level is 0dB. At this instance, because the digital filter circuit gets to stop operation the act of attenuation is impossible. In addition, whenever MDATA is not carried, MCLK must be 'HIGH' state. In case of no attenuation fuction needed, MDATA should be 'L', MCLK and MLD should be 'H.

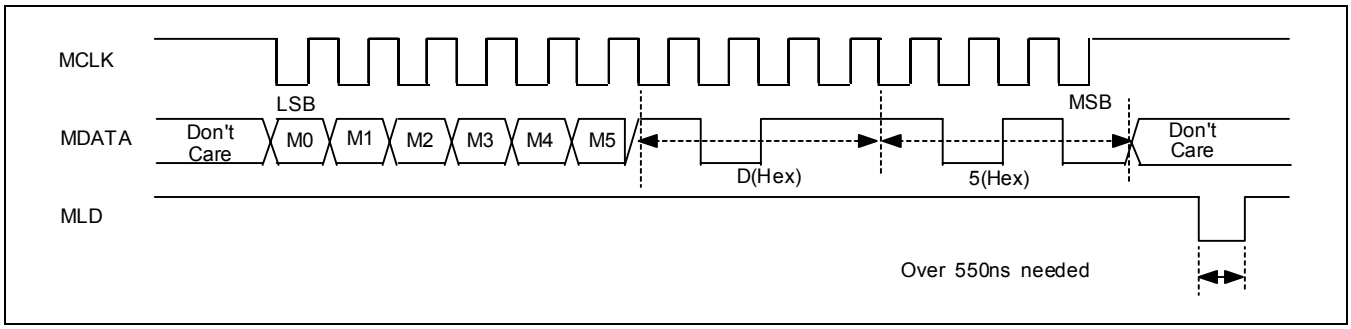


Figure 3. MICOM Interface Timing Chart

Table 2. Digital Attenuation Level

MDATA	Attenuation Level (dB)	MDATA	Attenuation Level (dB)
MSB LSB M5 M4 M3 M2 M1 M0 (h h b b b b b b)		MSB LSB M5 M4 M3 M2 M1 M0 (h h b b b b b b)	
5 D 0 0 0 0 0 0	0	5 D 1 0 0 0 0 0	-6.30
5 D 0 0 0 0 0 1	-0.28	5 D 1 0 0 0 0 1	-6.58
5 D 0 0 0 0 1 0	-0.42	5 D 1 0 0 0 1 0	-6.88
5 D 0 0 0 0 1 1	-0.56	5 D 1 0 0 0 1 1	-7.18
5 D 0 0 0 1 0 0	-0.71	5 D 1 0 0 1 0 0	-7.50
5 D 0 0 0 1 0 1	-0.86	5 D 1 0 0 1 0 1	-7.82
5 D 0 0 0 1 1 0	-1.01	5 D 1 0 0 1 1 0	-8.16
5 D 0 0 0 1 1 1	-1.16	5 D 1 0 0 1 1 1	-8.52
5 D 0 0 1 0 0 0	-1.32	5 D 1 0 1 0 0 0	-8.89
5 D 0 0 1 0 0 1	-1.48	5 D 1 0 1 0 0 1	-9.28
5 D 0 0 1 0 1 0	-1.64	5 D 1 0 1 0 1 0	-9.68
5 D 0 0 1 0 1 1	-1.80	5 D 1 0 1 0 1 1	-10.10
5 D 0 0 1 1 0 0	-1.97	5 D 1 0 1 1 0 0	-10.55
5 D 0 0 1 1 0 1	-2.14	5 D 1 0 1 1 0 1	-11.02
5 D 0 0 1 1 1 0	-2.32	5 D 1 0 1 1 1 0	-11.51
5 D 0 0 1 1 1 1	-2.50	5 D 1 0 1 1 1 1	-12.04
5 D 0 1 0 0 0 0	-2.68	5 D 1 1 0 0 0 0	-12.60
5 D 0 1 0 0 0 1	-2.87	5 D 1 1 0 0 0 1	-13.20
5 D 0 1 0 0 1 0	-3.06	5 D 1 1 0 0 1 0	-13.84
5 D 0 1 0 0 1 1	-3.25	5 D 1 1 0 0 1 1	-14.54
5 D 0 1 0 1 0 0	-3.45	5 D 1 1 0 1 0 0	-15.30
5 D 0 1 0 1 0 1	-3.66	5 D 1 1 0 1 0 1	-16.12
5 D 0 1 0 1 1 0	-3.87	5 D 1 1 0 1 1 0	-17.04
5 D 0 1 0 1 1 1	-4.08	5 D 1 1 0 1 1 1	-18.06
5 D 0 1 1 0 0 0	-4.30	5 D 1 1 1 0 0 0	-19.22
5 D 0 1 1 0 0 1	-4.53	5 D 1 1 1 0 0 1	-20.56
5 D 0 1 1 0 1 0	-4.76	5 D 1 1 1 0 1 0	-22.14
5 D 0 1 1 0 1 1	-5.00	5 D 1 1 1 0 1 1	-24.08
5 D 0 1 1 1 0 0	-5.24	5 D 1 1 1 1 0 0	-26.58
5 D 0 1 1 1 0 1	-5.49	5 D 1 1 1 1 0 1	-30.10
5 D 0 1 1 1 1 0	-5.75	5 D 1 1 1 1 1 0	-36.12
5 D 0 1 1 1 1 1	-6.02	5 D 1 1 1 1 1 1	-∞

FUNCTIONAL DESCRIPTION

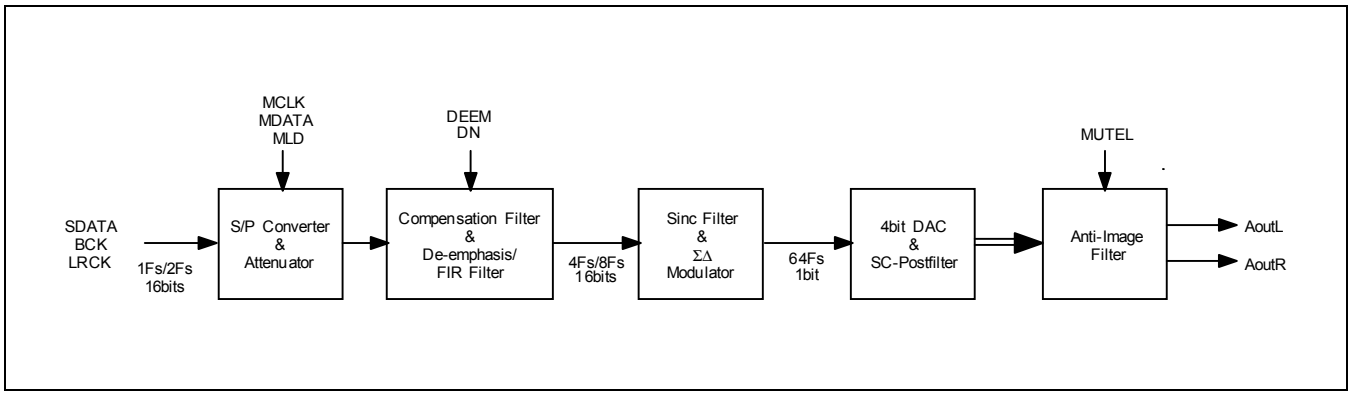


Figure 4. Funtional Block Diagram

Fig4 is the 1bit 4th order sigma-delta DAC block daigram. S/P Converter converts serial 16bit input data to parallel 16bit data. Digital input data is attenuated by MICOM interface pin control. Compensation Filter compensates gain droop in Passband by Sinc Filter and Sigma-Dellta Modulator Signal Transfer Function. De-emphasis Block de-emphasizes pre-emphasised input data to emphssize high frequency in audible band. FIR Filter perfroms 4X interpolation. And it outputs 4Fs(DN='Low') rate data or 8Fs(DN='High') rate data by variabled input data rate. It also removes the images of the input signal that are present at multiples of the input sample frequency. And Sinc filter makes the constant 64Fs rate data by 16 times or 8 times upsampling FIR Filter output data according to DN(Double/Normal Mode) Pin Selection. This operation intorduces a sinc function responce on the resulting frequency spectrum, which greatly attenuates the energy of images at the multifules of 4Fs(or 8Fs).

Digital sigma-delta modulator of bit-stream type has the IFL (Inverse-Follower-Leader) topology, and it performs a noise-shaping function. The modulator shapes the quantization noise by suppressing its in-band component and pushes the noise energy of outside the band-of-interest without deteriorating the audio input signal. The 64 times oversampled 1-bit PDM outputs from the modulator drives a analog postfilter.

The analog postfilter comprises SC-postfilter, anti-imaging filter. The SC-postfilter removes the quantization noise shaped to out-of-band by digital sigma-delta modulator. This analog filter has the good clock jitter characteristc and very linear characteristic. And following the CTF(continuous time filter) removes the sampling images and makes the high resolution analog output.

APPLICATION CIRCUIT

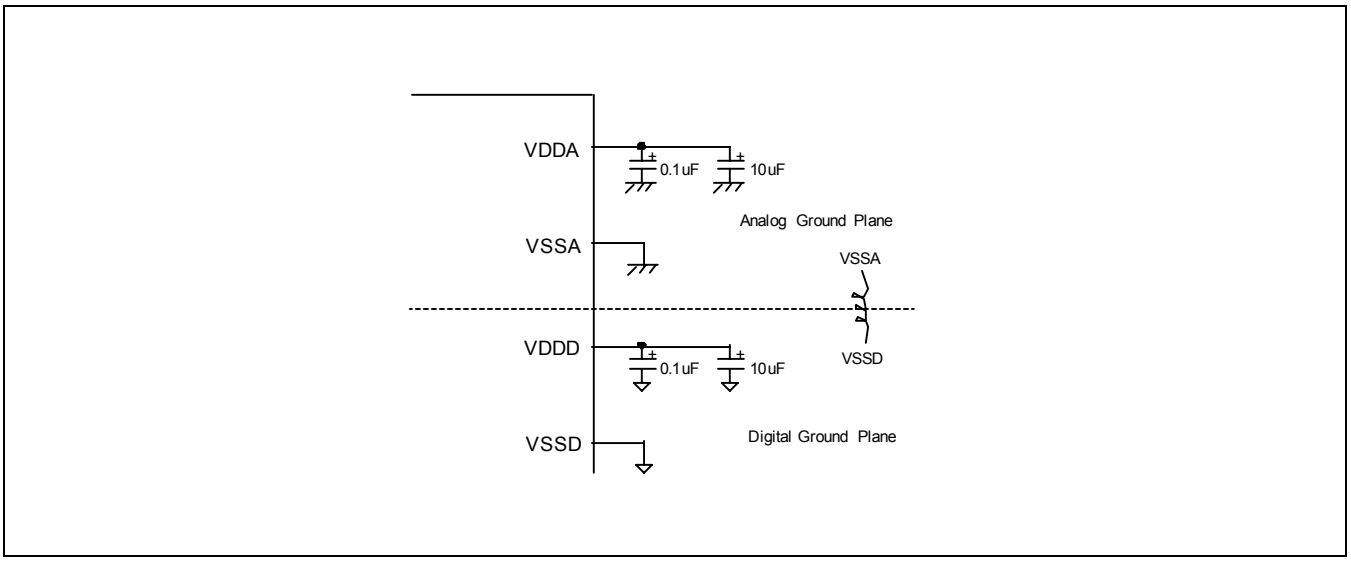


Figure 5. Bypass Capacitor for Power Supply Pins

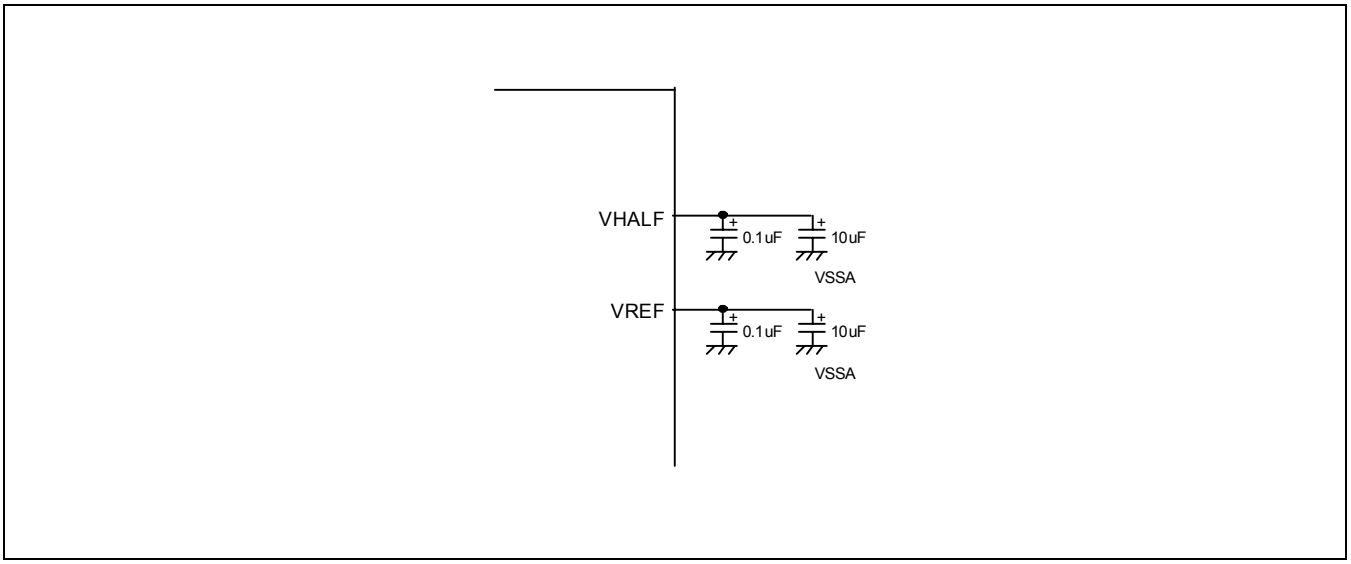


Figure 6. Bypass Capacitors for Reference Pins

Analog pins and digital pins must be seperated, Analog pins should be located on the analog ground plane and digital pins should be located on the digital ground plane. Analog ground and digital ground connection is recommended to only one path through ferrite bead like Fig5. Supply bypass capacitors should be located as close as possible to chip. Small bypass capacitor (0.1uF) should be positioned first to chip than large bypass capacitor (10uF).

Reference (VHALF, VREF) bypass capacitors (Fig6) should be located as close as possible to chip.

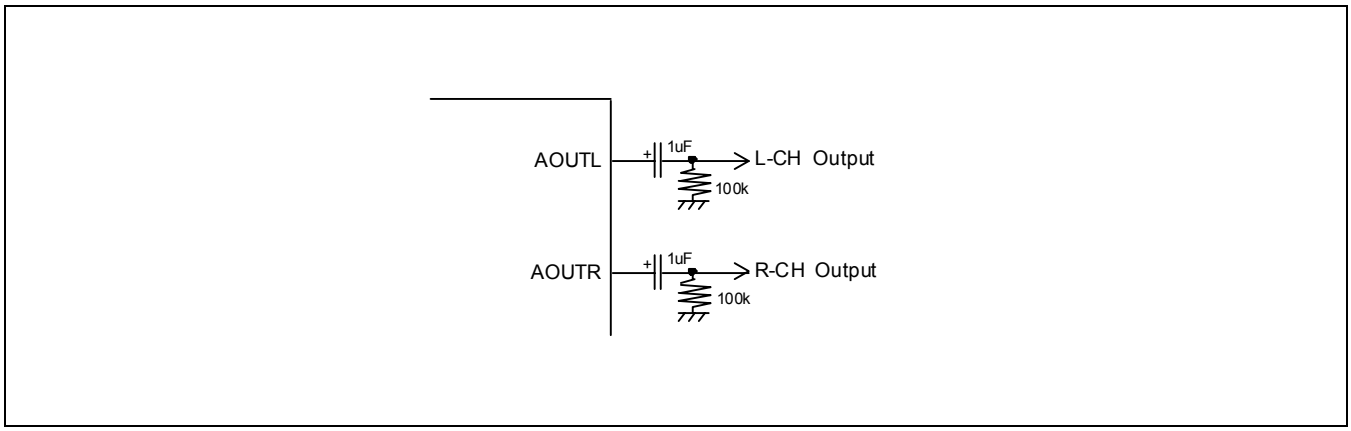


Figure 7. Ananlog output application

FIg7 is simple high pass filter circuit for analog output. It performs ac-coupling for analog output signal from analog common level to analog ground. Recommended component values are 1uF and 100kΩ.

User Guide

— This analog Core Verilog behavioral-modeling will be supplied.

FEEDBACK REQUEST

Sigma-Delta DAC Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
supply voltage				V	
Max master clock frequency				Hz	
Operating temperature				°C	
Sampling Frequency				Hz	
Dynamic range				dB	
Total harmonic distortion				dB	
Signal-to-noise ratio				dB	
Input format resolution (Serial/Parallel interface)				Bit	
Channel	Mono			Stereo	
Power dissipation				mW	
Full scale output voltage range				Vpp	
Group delay				sec	
Phase linearity deviation for passband region				– (Deg)	
Peak-to-peak frequency response ripple for passband region				dB	

— Could you explain external/internal pin configurations as required?

— Specially requested function list: