**TENTATIVE**

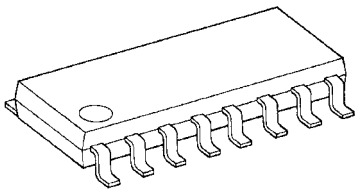
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

# TD7626F,TD7626FN

## 2.7GHz FREQUENCY SYNTHESIZER FOR SATELLITE TV

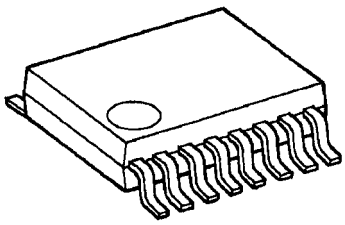
TD7626F and TD7626FN are single-chip frequency synthesizer ICs that can be combined with a μCPU to configure an advanced-function frequency synthesizer system.
TD7626FN comes in a more compact package, pitch 0.65mm.

TD7626F



SOP16-P-225-1.27

TD7626FN



SSOP16-P-225-0.65B

Weight
SOP16-P-225-1.27 : 0.16g (Typ.)
SSOP16-P-225-0.65B : 0.07g (Typ.)

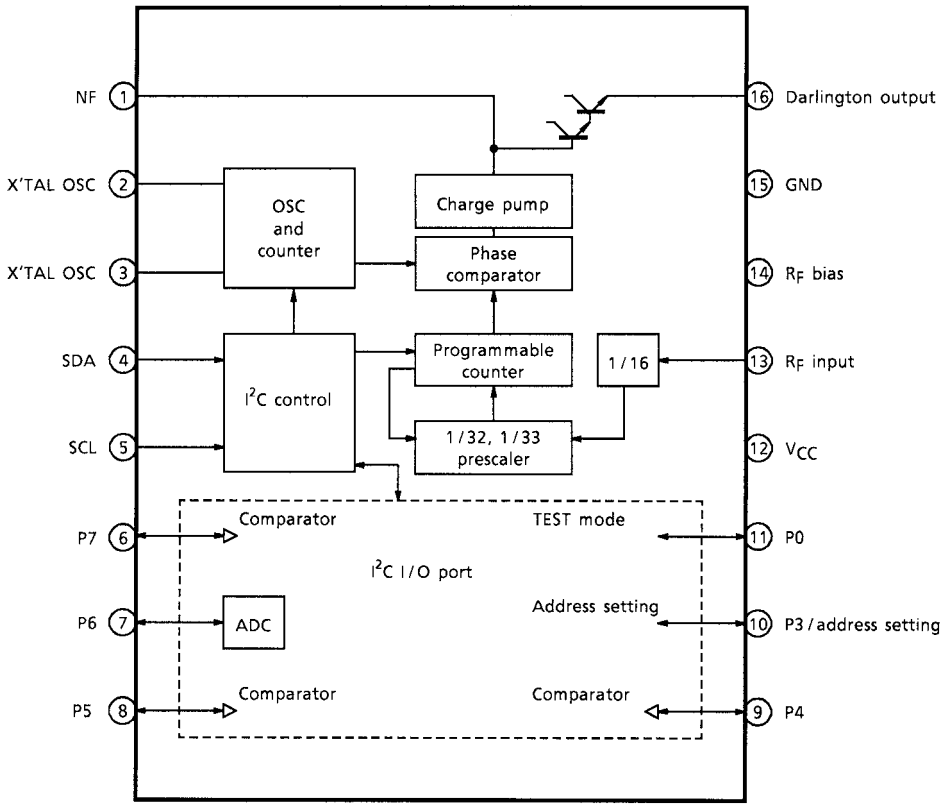
## FEATURES

- High input sensitivity
  $f_{in}$ = 0.5~2.7GHz : −15dBmW (50Ω) (Min.)
- Built-in 1 / 16 prescaler
- Built-in 5-level AD converter
- Built-in simple comparators×3
- Simple control bus ($I^2C$ bus)
- Four-address selectable by address selector
- Frequency divider ratio settings : 1 / 512, 1 / 1024
- Built-in power-on reset circuit
- Small flat package version
  : TD7626F : SOP16 (1.27mm pitch)
  TD7626FN : SSOP16 (0.65mm pitch)

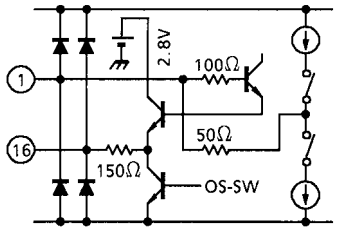
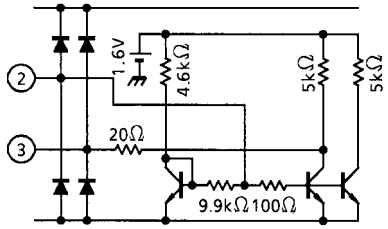
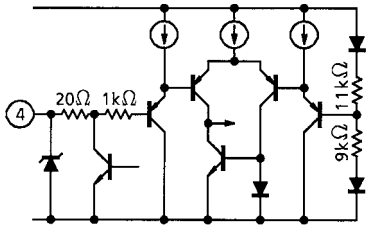
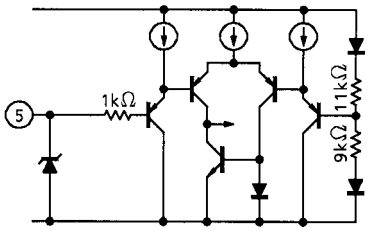
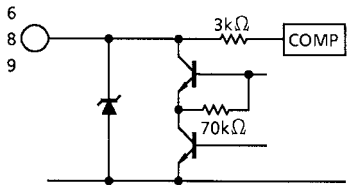
  Note: These devices are easy to be damaged by high static voltage or electric fields.
  In regards to this, please handle with care.
- Status after power-on reset

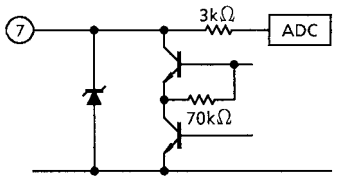
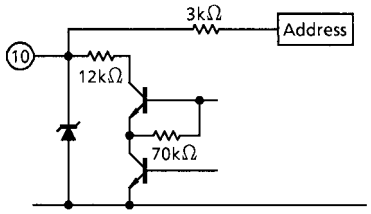
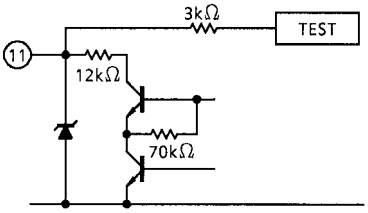
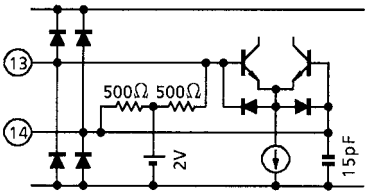
| | |
|---|---|
| Band drive $P_7$~$P_0$ | : OFF |
| Tuning amp | : ON |
| Tuning voltage output ($V_t$) | : Low level |
| Charge pump output current | : 50μA |
| Reference frequency divider ratio | : 1 / 512 |

## BLOCK DIAGRAM



## TERMINAL FUNCTIONS

| PIN No. | PIN NAME | FUNCTION | INTERFACE CIRCUIT |
|---|---|---|---|
| 1 | NF | Compares the phase of the input $R_F$ signal against the frequency data and feeds back its difference output from the current pump. |   |
| 16 | Charge pump output | | |
| 2 | X'tal $OSC_{in}$ | Crystal oscillator pins to generate the reference signal for the phase comparator. Consist of the inverter amp. |   |
| 3 | X'tal $OSC_{out}$ | | |
| 4 | SDA | Normally used as input / output pins for the $I^2C$ bus serial data. In TEST mode, used as the input pin for the signal to be compared by the phase comparator. |   |
| 5 | SCL | Normally used as the $I^2C$ bus serial clock input. In TEST mode, used to input the reference signal of the phase comparator. |   |
| 6 | P7 | Output can be controlled by setting the band switch data. The circuit configuration is open collector output. Each pin has a built-in comparator. The status of the comparator can be checked in READ mode. In TEST mode, P7 is a counter output which allows counter operation to be checked. |   |
| 8 | P5 | | |
| 9 | P4 | | |

| PIN No. | PIN NAME | FUNCTION | INTERFACE CIRCUIT |
|---|---|---|---|
| 7 | P6 | Output can be controlled by setting the band switch data.<br>The circuit configuration is open collector output.<br>An A / D converter is built in. In READ mode, five levels of applied voltage can be read.<br>In TEST mode, outputs the reference signal derived by dividing the crystal OSC signal by the set divider ratio. This allows operation to be checked. |  |
| 10 | P3 | Basically used as the address setting pin. The sub-address can be changed by applied voltage.<br>Can be used as a band switch as well, but incorporates resistance (12kΩ) for limiting current. |  |
| 11 | P0 | Output can be controlled by setting the band switch data. Incorporates resistance (12kΩ) for limiting current. (Can also be used for setting the prescaler in TEST mode.)<br>(Open collector output) |  |
| 12 | $V_{CC}$ | Power supply pin | — |
| 13<br>14 | $R_F$ input<br>$R_F$ bias | Prescaler input pins.<br>The circuit configuration is differential input.<br>Differential reference bias pin 14 has a built-in 15pF capacitor. |  |
| 15 | GND | Ground pin | — |

## MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage 1 | $V_{CC1}$ | 6.0 | V |
| Power Dissipation | $P_D$ | (Note 1) | mW |
| Operating Temperature | $T_{opr}$ | −20~85 | °C |
| Storage Temperature | $T_{stg}$ | −55~150 | °C |

Note 1: F-type : 540mW, FN-type : 560mW
Note 2: When using the device at temperatures higher than 25°C, maximum power dissipation decreases for every 1°C as follows : 4.3mW with F-type : 4.5mW with FN-type.
Note 3: Do not set the port pins (Pins 6, 7, 8, 9, 10, and 11) at or lower than the level of the GND pin.
Note 4: These devices are easy to be damaged by high static voltage or electric fields.
In regards to this, please handle with care.

## RECOMMENDED SUPPLY VOLTAGE

| PIN No. | PIN NAME | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| 12 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |

## ELECTRICAL CHARACTERISTICS (Unless otherwise stated, $V_{CC}$ = 5V, Ta = 25°C)
## AC CHARACTERISTICS

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Current | $I_{CC1}$ | 1 | Band switch : OFF<br>OS : [ 1] | 20 | 35 | 52 | mA |
| Prescaler Input Sensitivity | $V_{in}$ | 2 | f = 500~2700MHz | −15 | — | +3 | dBmW |
| Logic Input High Voltage | $V_{IH}$ | 3 | Logic pins (SDA, SCL)<br>In the test circuit, transfer P5 data and determine reception from the lighting of the LED lamp.<br>Measure the output using a logic analyzer. | 3.0 | — | — | V |
| Logic Input Low Voltage | $V_{IL}$ | | | — | — | 0.8 | |
| Logic Output High Voltage | $V_{OH}$ | | | 3.8 | — | — | |
| Logic Output Low Voltage | $V_{OL}$ | | | — | — | 0.5 | |
| Logic Input High Current | $I_{IH}$ | 3 | Apply 5V to input pin. | — | — | 10 | μA |
| Logic Input Low Current | $I_{OL}$ | | Apply 0V to input pin. | — | — | −20 | |
| External OSC Input Amplitude | $OSC_{in}$ | 3 | OSCin (Pin 2) | 350 | — | 1000 | $MV_{p-p}$ |
| OSC Operating Frequency | $OSC_{fin}$ | 3 | Pins 2, 3 | 3.0 | 4.0 | 4.5 | MHz |
| Crystal Negative Resistance | $X_{tR}$ | 3 | TEST mode, frequency divided crystal signal output, P6 monitor | — | 1.5 | — | kΩ |
| Output Port Flow Current | $IP_{in}$ | 3 | P4, P5, P6, P7 | 5 | — | — | mA |
| Output Port Leakage Current | $IP_{lk}$ | 3 | Apply 12V as pull-up voltage. | — | — | 10 | μA |
| Output Port Built-In Resistance | $R_{port}$ | — | P0 and P3 | — | 12 | — | kΩ |
| Output Port MAX Voltage | $V_{port}$ | — | P0, P3, P4, P5, P6, P7 | — | — | 13.2 | V |
| A / D Converter Input Voltage | $V_{ADC}$ | — | P6 | 0.0 | — | 13.2 | V |
| Comparator Pin Input Voltage | $V_{CMP}$ | 3 | P4, P5, and P7 | 0.0 | — | 13.2 | V |
| Comparator High Voltage | $V_{HCMP}$ | 3 | P4, P5, and P7 | 2.0 | — | 13.2 | V |
| Comparator Low Voltage | $V_{LCMP}$ | 3 | P4, P5, and P7 | 0.0 | — | 0.8 | V |
| Charge Pump Output Current | $I_{chg0}$ | — | CP : [0] | — | 50 | — | μA |
| | | | CP : [1] | — | 170 | — | |

## DATA FORMAT

a) WRITE MODE

| BYTE | | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ADDRESS Byte | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R / W = 0 | ACK |
| 2 | DIVIDER Byte (1) | 0 | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | ACK |
| 3 | DIVIDER Byte (2) | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ | ACK (L) |
| 4 | CONTROL Byte | 1 | CP | $T_1$ | $T_0$ | TS2 | TS1 | TS0 | OS | ACK |
| 5 | BAND SW Byte | P7 | P6 | P5 | P4 | P3 | X | X | P0 | ACK (L) |

(L) : DATA LATCH
× : DON'T Care
ACK : Acknowledgment

b) READ MODE

| BYTE | | MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ADDRESS Byte | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R / W = 1 | ACK |
| 2 | STATUS Byte | 0 | FL | IP7 | IP5 | IP4 | $A_2$ | $A_1$ | $A_0$ | ACK |

ACK : Acknowledgment

## DATA DETAILS

- MA1, MA0 :Programmable address bits
  (Indicate applied voltage of pin 10 and corresponding address setting.)

| ADDRESS PIN APPLIED VOLTAGE | MA1 | MA0 |
|---|---|---|
| $0 \sim 0.2 \times V_{CC}$ | 0 | 0 |
| $0.3 \times V_{CC} \sim 0.7 \times V_{CC}$ | 1 | 0 |
| $0 \sim V_{CC}$ | 0 | 1 |
| $0.8 \times V_{CC} \sim V_{CC}$ | 1 | 1 |

- CP : Charge pump current setting
  [0] : 50μA (Typ.)
  [1] : 170μA (Typ.)
- $T_1$ : Test mode switching
  [0] : NORMAL mode
  [1] : TEST mode
- $T_0$ :Charge pump control setting
  [0] : Charge pump ON
  [1] : Charge pump OFF

- TS2, TS1, TS0 : TEST mode settings

| CHARACTERISTIC | $T_1$ | TS2 | TS1 | TS0 | FREQUENCY DIVIDER RATIO | REMARKS |
|---|---|---|---|---|---|---|
| Normal State | 0 | × | × | 0 | 1 / 1024 | — |
| Normal State | 0 | × | × | 1 | 1 / 512 | — |
| Charge Pump Sink | 1 | 1 | 0 | 0 | 1 / 1024 | FL = 0 : Charge pump output sink side only on |
| Charge Pump Source | 1 | 1 | 0 | 1 | 1 / 512 | FL = 1 : Charge pump output source side only on |
| Output Port OFF | 1 | 1 | 1 | 0 | 1 / 1024 | P7~P4 = OFF |
| Phase Comparator Test | 1 | 1 | 1 | 1 | 1 / 512 | SDA: Input of signal to be compared<br>SCL: Reference signal input |
| Crystal Divider Counter Output | 1 | 0 | × | 0 | 1 / 1024 | P6 : Crystal divider output<br>P7 : Counter output (1 / 16×32×count data)<br>P0 : Prescaler settings ··· [0] : ON [1] : OFF<br>P7~P4 = OFF |
| | 1 | 0 | × | 1 | 1 / 512 | |

× : DON'T Care

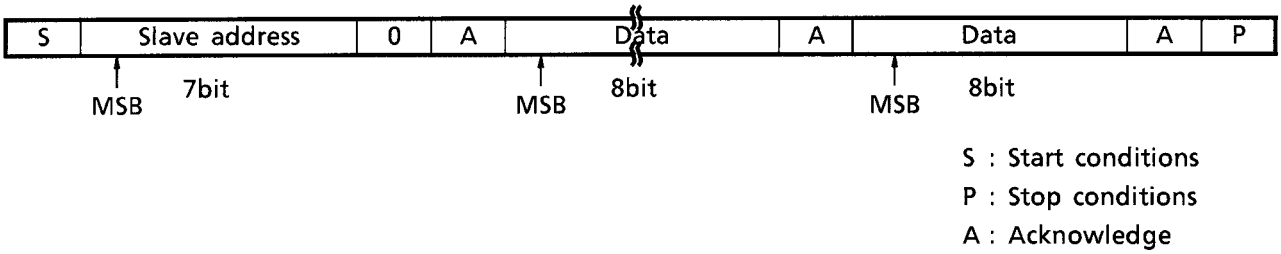
- OS : Tuning amp control settings
  [0] : Tuning on (Normal state)
  [1] : Tuning off (Fixes charge pump output at 0.0~0.2V)
- FL : Lock detect flag
  [0] : Unlocked
  [1] : Locked
- IP7, IP5, IP4 : Comparator output (P7, P5, P4)
  [0] : Applied voltage ..... 0.0~0.8V
  [1] : Applied voltage ..... 2.0~13.2V
- A2, A1, A0 : 5-level A / D converter (P6)

| ADC PIN APPLIED VOLTAGE | $A_2$ | $A_1$ | $A_0$ |
|---|---|---|---|
| $0.60\times V_{CC}$~13.2V | 1 | 0 | 0 |
| $0.45\times V_{CC}$~$0.60\times V_{CC}$ | 0 | 1 | 1 |
| $0.30\times V_{CC}$~$0.45\times V_{CC}$ | 0 | 1 | 0 |
| $0.15\times V_{CC}$~$0.30\times V_{CC}$ | 0 | 0 | 1 |
| 0~$0.15\times V_{CC}$ | 0 | 0 | 0 |

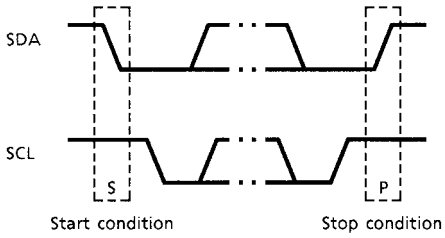
## I²C BUS CONTROLLED FORMAT SUMMARY

Bus controlled format of TD7626F, TD7626FN are based on I²C Bus Control format of Philips.

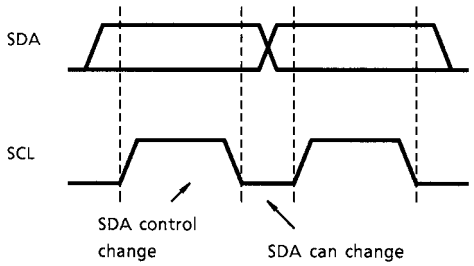
Data transfer format



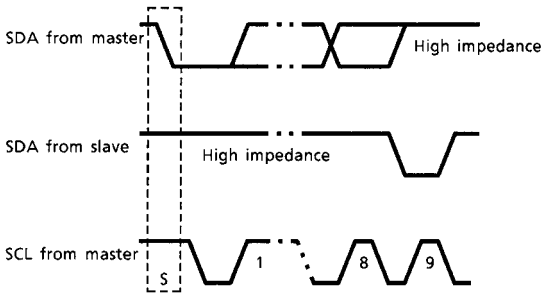

(1) Start condition and stop condition




(2) Bit transfer




(3) Acknowledgement

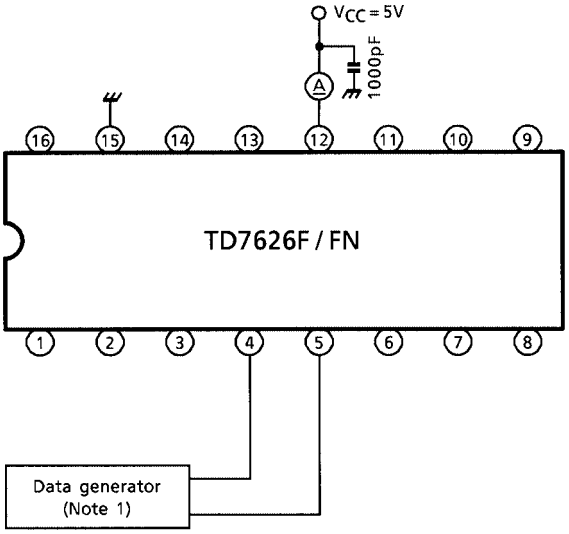



(4) Slave addresses

| $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | R / $\overline{W}$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | X | X | 0 |

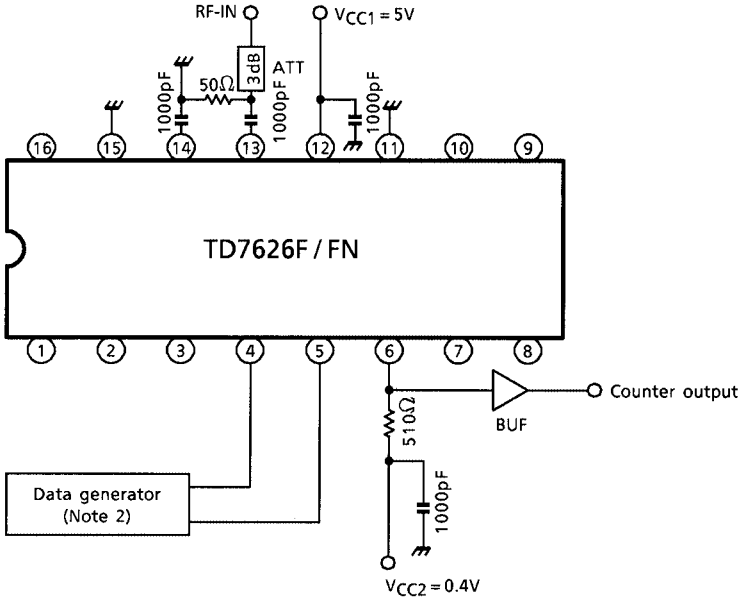
Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

## TEST CIRCUIT 1



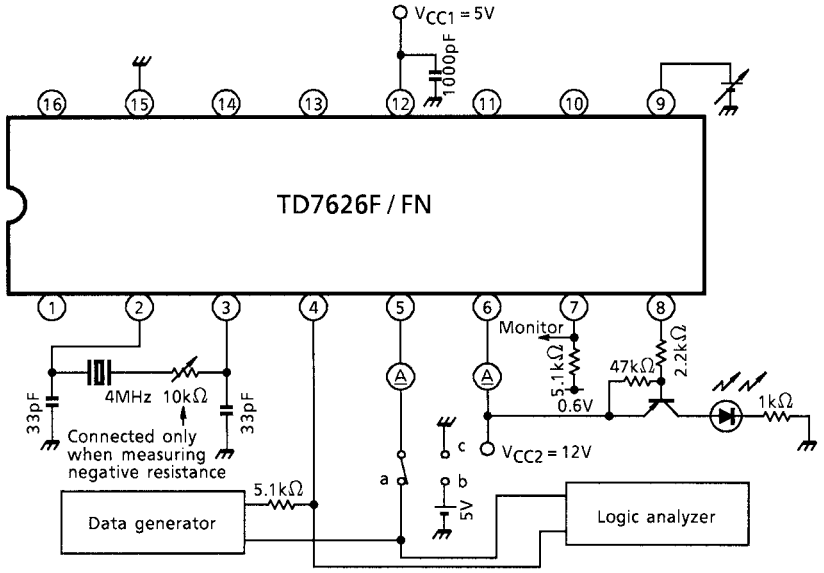

Note 1: Band switch…OFF, tuning amp…OFF

## TEST CIRCUIT 2

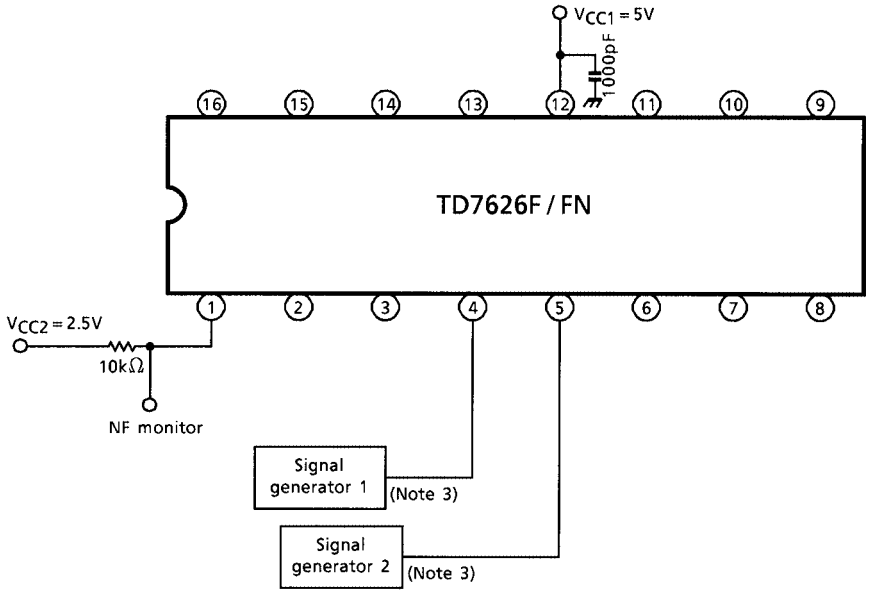



Note 2: See TEST mode settings (Counter output)

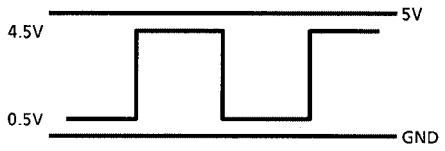
## TEST CIRCUIT 3



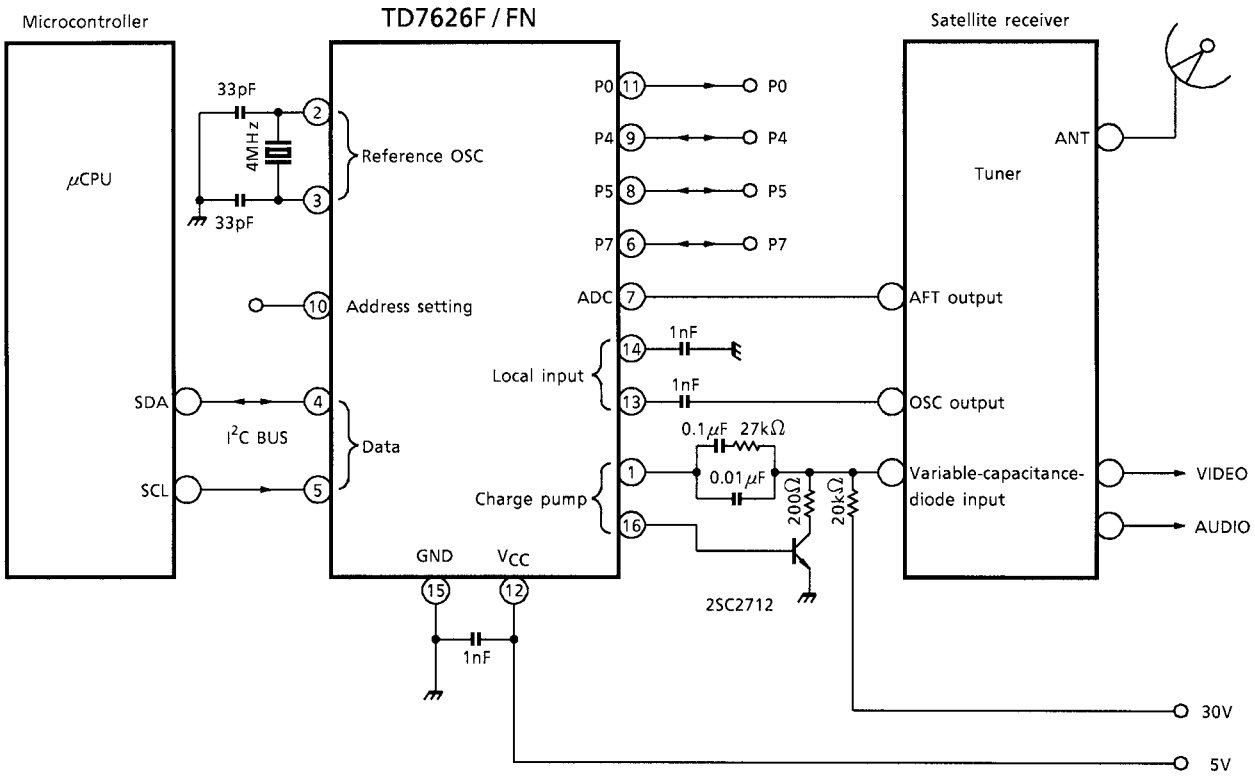

## TEST CIRCUIT 4




Note 3: Phase comparator input level

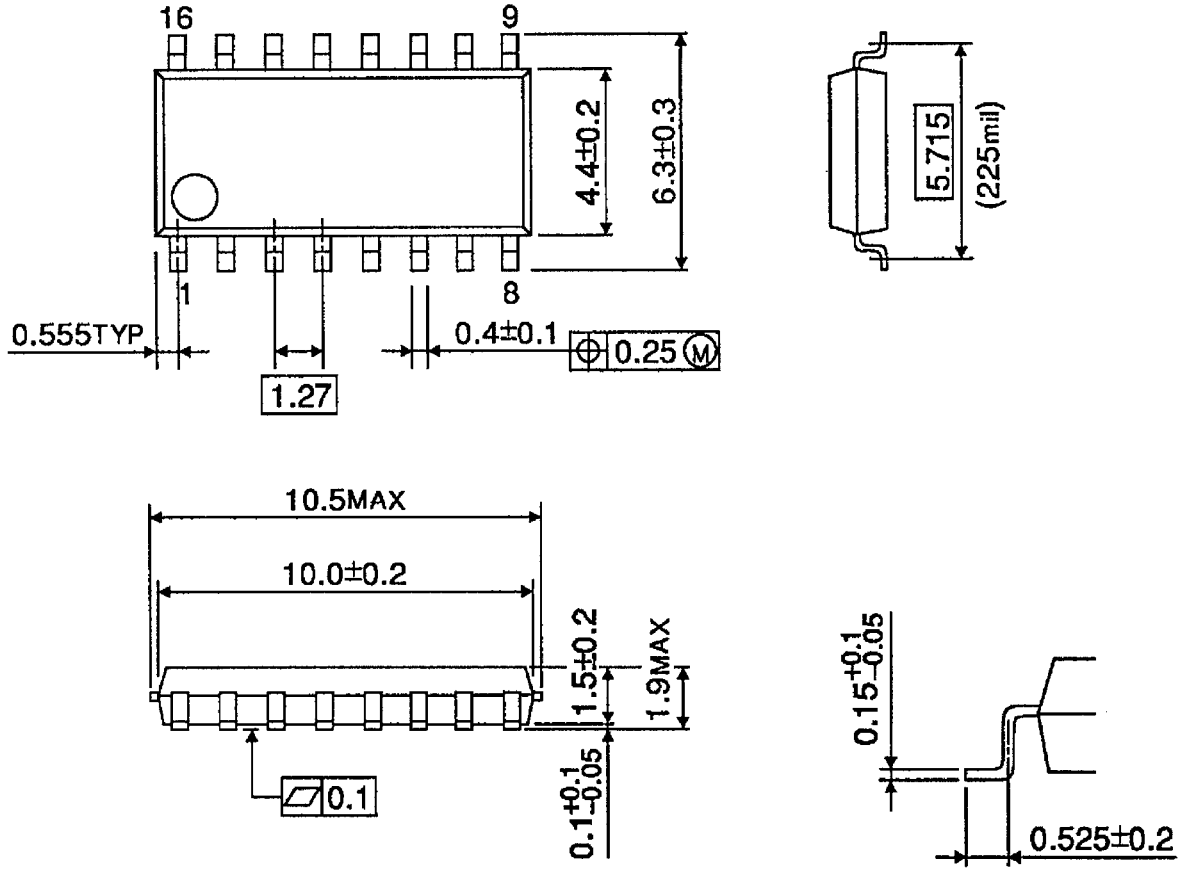


## EXAMPLE OF FREQUENCY SYNTHESIZER APPLICATION CIRCUIT



## PACKAGE DIMENSIONS

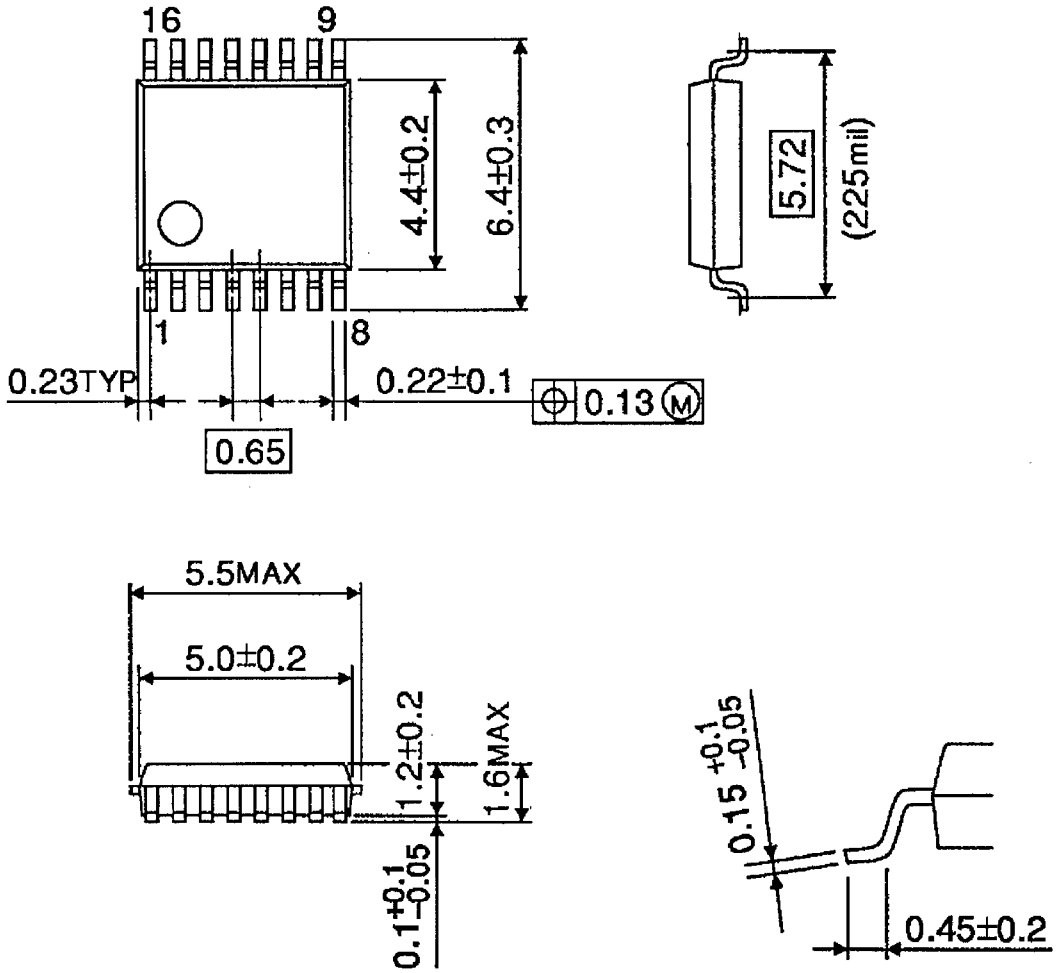
SOP16-P-225-1.27 Unit : mm




Weight: 0.16g (Typ.)

**PACKAGE DIMENSIONS**

SSOP16-P-225-0.65B Unit : mm




Weight: 0.07g (Typ.)