MSVD-HD

Multi-Standard High-Definition Video Decoder (H.264, VC-1, MPEG-1/2)

The Multi-Standard High-Definition Video Decoder DesignObject™ (MSVD-HD*) is one of the smallest synthesizable cores in the market, performing time multiplexed decoding of multiple streams in different standards at all resolutions up to 2048x2048 pixels. It is substantially smaller than a fully programmable solution. The MSVD-HD is a real-time solution for dual-stream high-definition video decoding with a single core at a low clock rate.

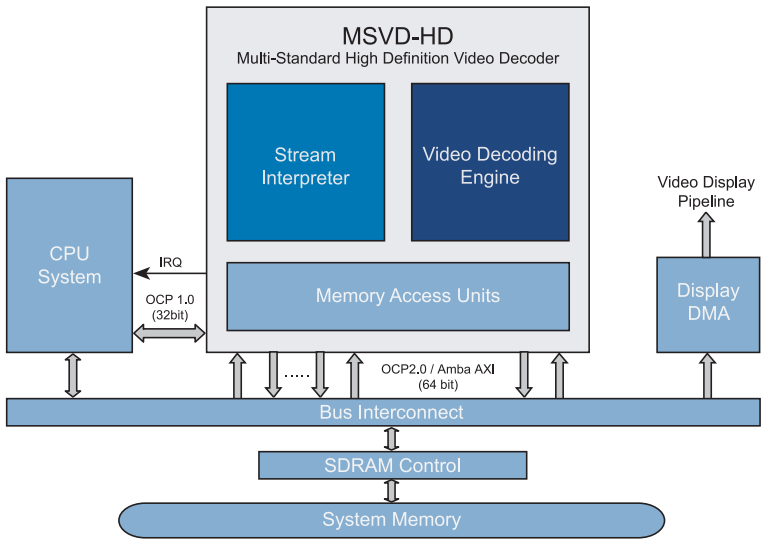
The MSVD-HD currently supports H.264, MPEG-1/2 and VC-1 standards. The decoding functionality is implemented as an autonomously working pipeline consisting of various hardware blocks. The driver software running on an external controller, a general purpose 32-bit processor, performs setup and general controlling tasks.

The MSVD-HD reads the input stream from a buffer located in the system memory (SDRAM) and generates decoded video in YCbCr 4:2:0 format. The output pictures are stored in the decoded picture buffer area within the system memory.

MSVD-HD is an optimized solution for video decoding applications, based on an architecture that implements pipelining and parallelism on different levels. MSVD-HD consists of a software part and a hardware part. The hardware part is composed of two main blocks, the Stream Interpreter and the Multi-standard Video Decoding Engine. In order to achieve maximum performance, the two blocks work in parallel.

The MSVD-HD is optimized to satisfy a wide range of applications and technologies with optimal performance at low silicon cost. Its interfaces are designed for easy integration into system-on-chip designs.

MSVD-HD System Diagram



Applications

- **Set-top boxes**
- **Digital TV sets and IPTV applications**
- **DVD, HD-DVD and Blu-ray players and recorders**
- **Portable multimedia players**
- **Surveillance**

Key Features

- **Supports H.264, MPEG-1/2 & VC-1 up to 1080p @ 60 fps**
- **Supports all DVB, ATSC, HDTV, DVD, VCD resolutions**
- **Supports picture size from 48x32 to 2048x2048 pixel**

*MSVD-HD was formerly part of the sci-worx GmbH product portfolio. Silicon Image acquired sci-worx in January 2007.

MSVD-HD Features

Silicon Image Video Cores

Decoder for SD resolution:

- Consumer DV
- MPEG-1, MPEG-2 (multi-stream)
- MPEG-1/2/4, DivX, Xvid

Encoder for SD resolution:

- MPEG-1, MPEG-2 (I-frame)
- MPEG-1, MPEG-2 (IPB-frame)
- MPEG-1/2/4, DivX, Xvid (IPB-frame)

Decoder for HD resolution:

- MPEG-1, MPEG-2 (dual-HD)

- Supported standards:
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2)
  - SMPTE 421M VC-1 (simple, main and advanced profile @ level 4)
  - ISO/IEC 11172-2 MPEG-1
  - ISO/IEC 13818-2 MPEG-2 (main profile @ high level)
- Supports all DVB, ATSC, HDTV, DVD, VCD resolutions (e.g. 1080p, 1080i, 720p, D1)
- Supports picture size from 48x32 pixel to 2048x2048 pixel
- Error detection and concealment
- Trick mode support
- Processing of ES and PES streams, extraction and provision of time stamps
- SOC prototyping on FPGA including ASIC bus interconnect and DDR2 SDRAM
- Allegro H.264 certification test suite proven
- 64-bit ports to memory system, OCP 2.0 and AMBA AXI compliant

Key Advantages

- Silicon area efficient solution
- True multi-stream decoding features:
  - HD dual-stream processing performance
  - Multiple streams (up to 16 supported by HW, minimal SW support)
  - Applications are program preview, multiple thumbnail streams
- Fine granular context switching between streams on macroblock row level:
  - Minimizes memory requirements for input buffers
  - Minimizes input to output delay
- Simultaneous multi-stream and multi-standard decoding:
  - E.g. one HD H.264 and one HD MPEG-2 stream

Performance

- Dual-stream decode up to 1080i @ 30 fps at 150MHz core clock frequency
- Single-stream decode up to 1080p @ 60 fps at 150MHz core clock frequency
- Time multiplexed multi-stream decoding with fine granular context switching, possible combinations are:
  - Two HD video streams H.264, VC-1, MPEG-2
  - One H.264 HD stream and four VC-1 SD streams
  - One HD stream and 16 CIF streams
- Hardwired, autonomously running decoding pipeline, two samples per clock throughput
- Hardware supported context switching between video streams (configurable up to 16 streams)
- MSVD-HD core and memory system can run with different clocks; clock domain crossing is part of MSVD-HD

MSVD-HD Gate Count

	Gate Count[1]	Ram Size	SRAM Instances
MSVD-HD	970 kgates[2]	152 kbits	41

[1] Gate = 2 input NAND equivalent, using a TSMC 90 nm library (tsmc90g library under worst-case condition, 20% security margin), MBIST not included

[2] Gate count includes complete memory interfacing, stream reader functionality and extra logic for context switch support (245 kGates)

Silicon Image, Inc.
1060 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000
F 408.830.9530
www.siliconimage.com

Simply Stored. Connected. Beautiful.

Part Number: MSVD-HD

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