

8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

- HIGH SPEED:
 $t_{PD} = 8.3 \text{ ns}$ (TYP.) at $V_{CC} = 3.3 \text{ V}$
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- LOW NOISE:
 $V_{OLP} = 0.5\text{V}$ (TYP.) at $V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 12\text{mA}$ (MIN) at $V_{CC} = 3.0 \text{ V}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2\text{V to } 3.6\text{V}$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74LVQ299 is a low voltage CMOS 8 BIT PIPO SHIFT REGISTER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and low noise 3.3V applications.



Table 1: Order Codes

PACKAGE	T & R
SOP	74LVQ299MTR
TSSOP	74LVQ299TTR

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1) as shown in the Truth Table.

When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high impedance state; however sequential operation or clearing of the register is not affected. Clear function is asynchronous to clock.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

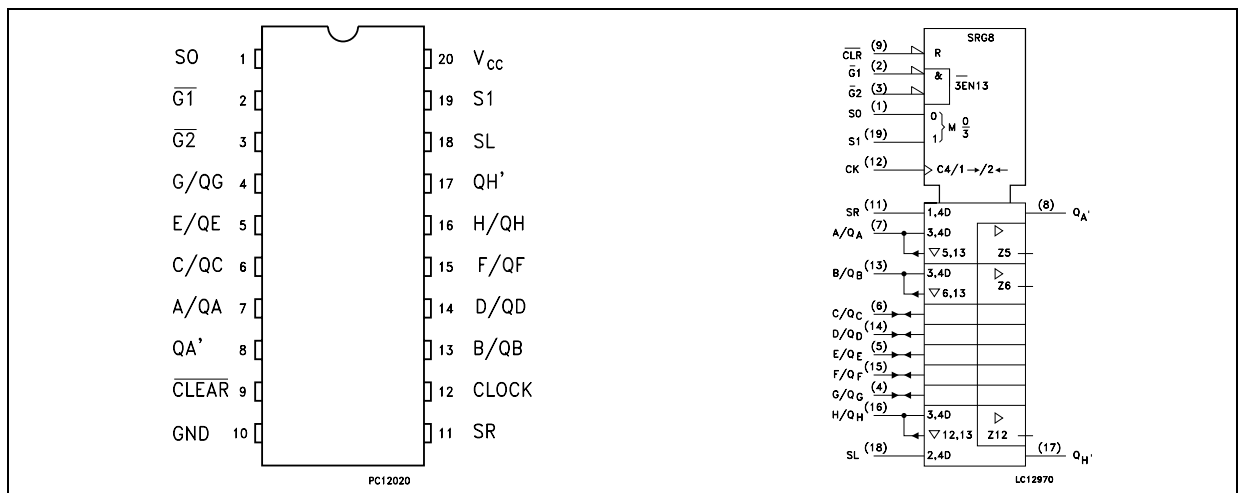


Figure 2: Input And Output Equivalent Circuit

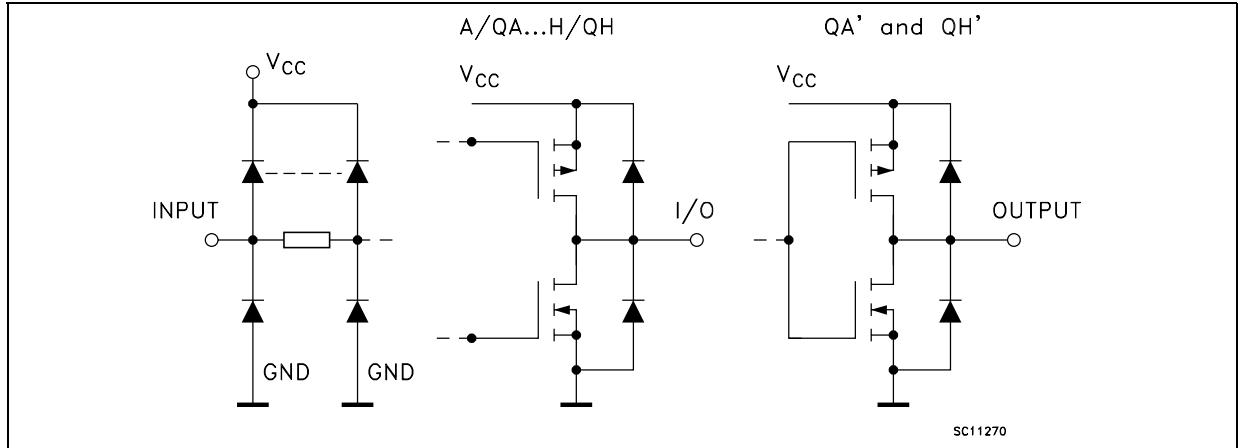


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 19	S0, S1	Mode Select Inputs
2, 3	G1, G2	3-State Output Enable Inputs (Active LOW)
7, 13, 6, 14, 5, 15, 4, 16	A/QA to H/QH	Parallel Data Inputs or 3-State Parallel Outputs (Bus Driver)
8, 17	QA',QH'	Serial Outputs (Standard Output)
9	CLEAR	Asynchronous Master Reset Input (Active LOW)
11	SR	Serial Data Shift Right Input
12	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
18	SL	Serial Data Shift Left Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

Table 3: Truth Table

MODE	INPUTS						INPUTS/OUTPUTS				OUTPUTS	
	CLEAR	FUNCTION SELECTED		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	G1*	G2*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	⌋	X	H	H	QGn	H	QGn
	H	L	H	L	L	⌋	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	⌋	H	X	QBn	H	QBn	H
	H	H	L	L	L	⌋	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	⌋	X	X	a	h	a	h

* When one or both controls are high, the eight input/output terminals are the high impedance state: however sequential operation or cleaning of the register is not affected.

Z: High Impedance

Qn0: The level of An before the indicated steady state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by OR

a, h: The level of the steady state inputs A, H, respectively.

X: Don't Care

Figure 3: Logic Diagram

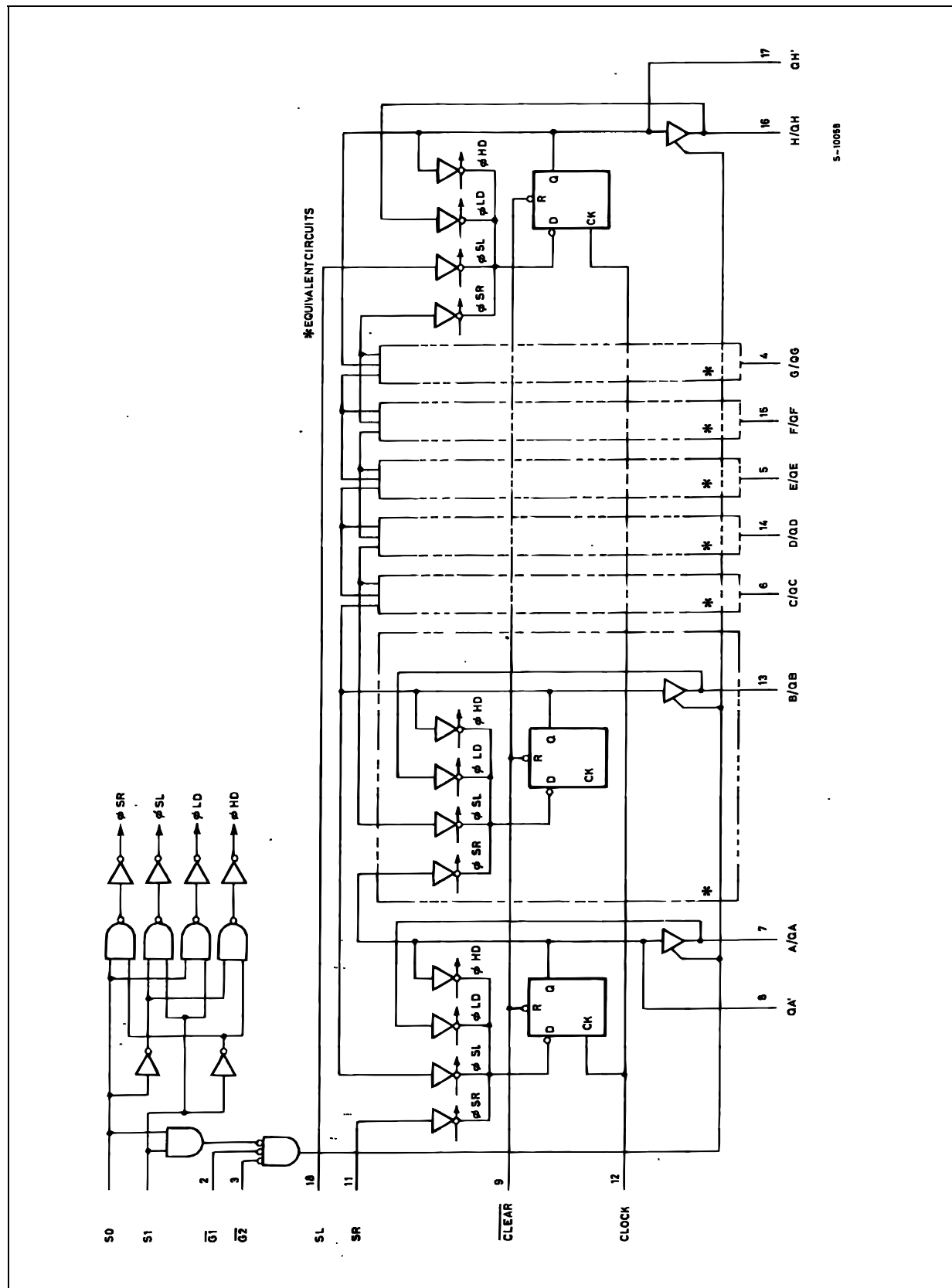


Figure 4: Timing Chart

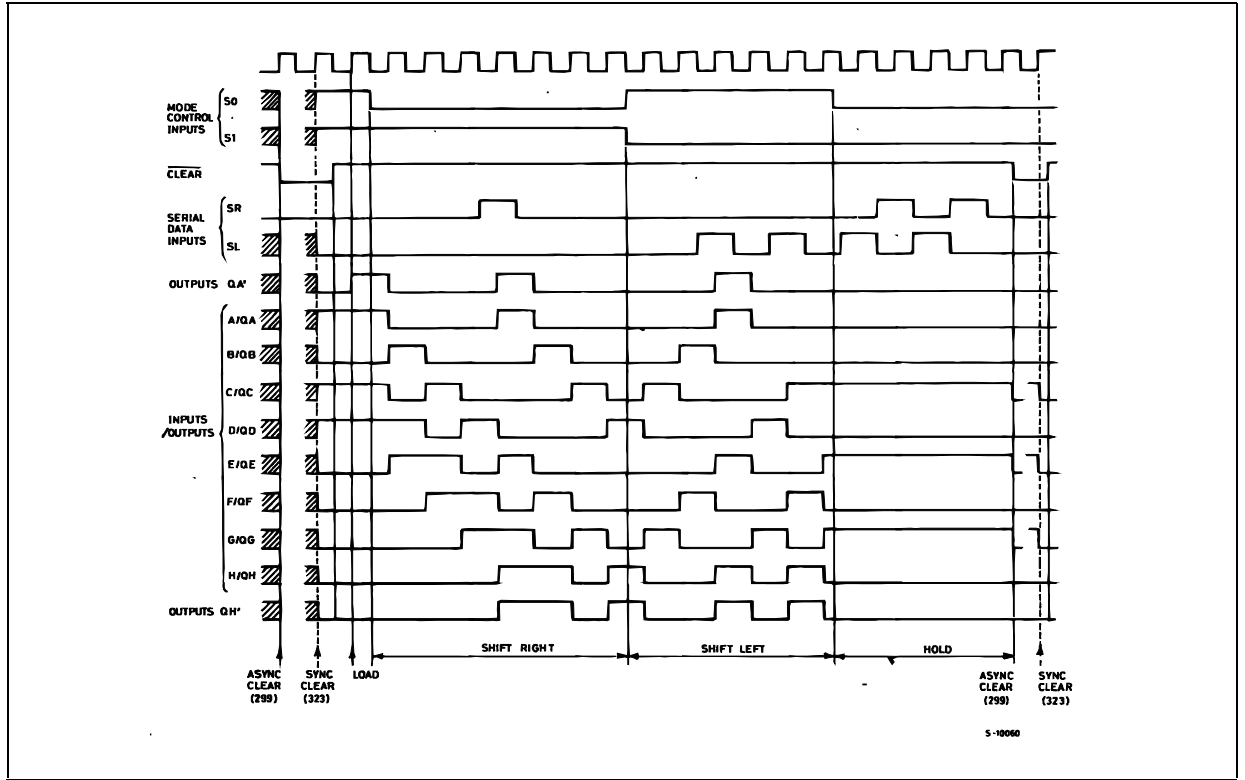


Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0V$ (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	3.0 to 3.6		2.0			2.0		2.0		V
V _{IL}	Low Level Input Voltage					0.8		0.8		0.8	V
V _{OH}	High Level Output Voltage	3.0	I _O =-50 μA	2.9	2.99		2.9		2.9		V
			I _O =-12 mA	2.58			2.48		2.48		
			I _O =-24 mA				2.2		2.2		
V _{OL}	Low Level Output Voltage	3.0	I _O =50 μA		0.002	0.1		0.1		0.1	V
			I _O =12 mA		0	0.36		0.44		0.44	
			I _O =24 mA					0.55		0.55	
I _I	Input Leakage Current	3.6	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 5.0	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			4		40		40	μA
I _{OLD}	Dynamic Output Current (note 1, 2)	3.6	V _{OLD} = 0.8 V max				36		25		mA
I _{OHD}			V _{OHD} = 2 V min				-25		-25		mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.5	0.8					V
V _{OLV}				-0.8	-0.6						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2						V	
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics ($C_L = 50$ pF, $R_L = 500$ Ω , Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK to Q'_A or Q'_H	2.7			9.7	15.0		17.5		20.0	ns
		3.3 ^(*)			8.2	12.0		14.0		16.5	
t_{PLH} t_{PHL}	Propagation Delay Time CLOCK to A/QA, H/QH	2.7			9.8	15.0		17.5		20.0	ns
		3.3 ^(*)			8.3	12.0		14.0		16.5	
t_{PHL}	Propagation Delay Time CLEAR to Q'_A or Q'_H	2.7			8.4	14.0		16.5		19.0	ns
		3.3 ^(*)			7.1	11.0		13.0		15.0	
t_{PHL}	Propagation Delay Time CLEAR to A/QA, H/QH	2.7			8.9	15.0		17.5		20.0	ns
		3.3 ^(*)			7.4	12.0		14.0		16.5	
t_{PZL} t_{PZH}	Output Enable Time G1 or G2 to A/QA, H/QH	2.7			9.9	15.0		17.5		20.0	ns
		3.3 ^(*)			8.0	12.0		14.0		16.5	
t_{PLZ} t_{PHZ}	Output Disable Time G1 or G2 to A/QA, H/QH	2.7			9.8	15.0		17.5		20.0	ns
		3.3 ^(*)			8.0	12.0		14.0		16.5	
t_W	CLEAR Pulse Width LOW	2.7		5.0	2.1		5.0		5.0		ns
		3.3 ^(*)		4.0	2.0		4.0		4.0		
t_W	CLOCK Pulse Width LOW	2.7		5.0	2.1		5.0		5.0		ns
		3.3 ^(*)		4.0	2.0		4.0		4.0		
t_s	Setup Time HIGH or LOW (A/QA, H/QH to CLOCK)	2.7		4.0	1.4		4.0		4.0		ns
		3.3 ^(*)		3.0	1.1		3.0		3.0		
t_h	Hold Time HIGH or LOW (A/QA, H/QH to CLOCK)	2.7		1.0	-1.3		1.0		1.0		ns
		3.3 ^(*)		1.0	-1.0		1.0		1.0		
t_s	Setup Time HIGH or LOW (S0 or S1 to CLOCK)	2.7		6.0	3.1		6.0		6.0		ns
		3.3 ^(*)		5.0	2.5		5.0		5.0		
t_h	Hold Time HIGH or LOW (S0 or S1 to CLOCK)	2.7		1.0	-3.1		1.0		1.0		ns
		3.3 ^(*)		1.0	-2.6		1.0		1.0		
t_s	Setup Time HIGH or LOW (SR or SL to CLOCK)	2.7		4.0	1.5		4.0		4.0		ns
		3.3 ^(*)		3.0	1.1		3.0		3.0		
t_h	Hold Time HIGH or LOW (SR or SL to CLOCK)	2.7		1.0	-1.5		1.0		1.0		ns
		3.3 ^(*)		1.0	-1.1		1.0		1.0		
t_{REM}	Recovery Time CLEAR to CLOCK	2.7		1.0	-0.7		1.0		1.0		ns
		3.3 ^(*)		1.0	-0.5		1.0		1.0		
f_{MAX}	Maximum Clock Frequency	2.7		100	150		80		60		ns
		3.3 ^(*)		120	180		100		80		
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.7			0.5	1.0		1.0		1.0	ns
		3.3 ^(*)			0.5	1.0		1.0		1.0	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

2) Parameter guaranteed by design

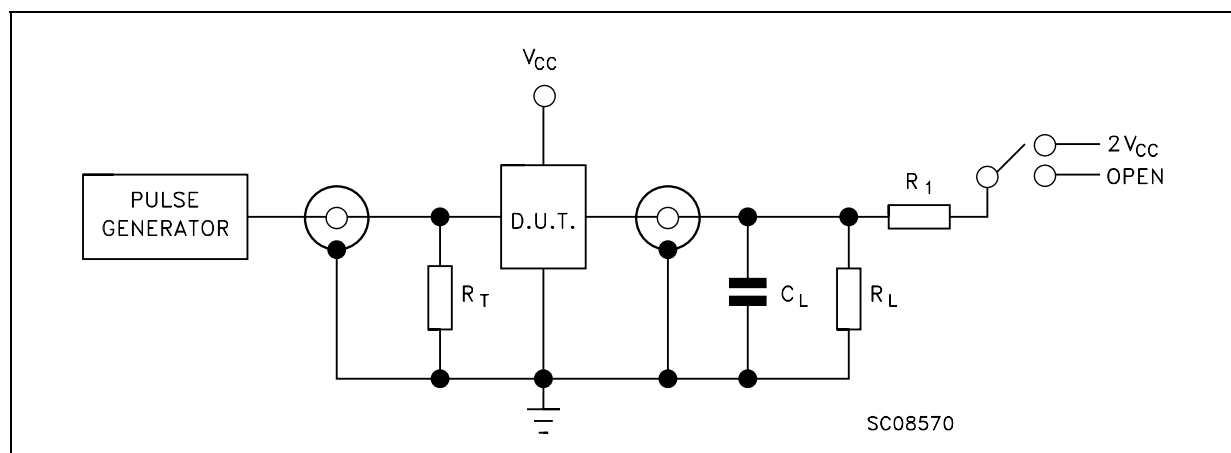
(*) Voltage range is 3.3V \pm 0.3V

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	3.3			4						pF
$C_{I/O}$	Bus Input Capacitance										pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	$f_{IN} = 10\text{MHz}$		10						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

Figure 5: Test Circuit



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	$2V_{CC}$
t_{PZH} , t_{PHZ}	Open

$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 6: Waveform - Propagation Delays (f=1MHz; 50% duty cycle)

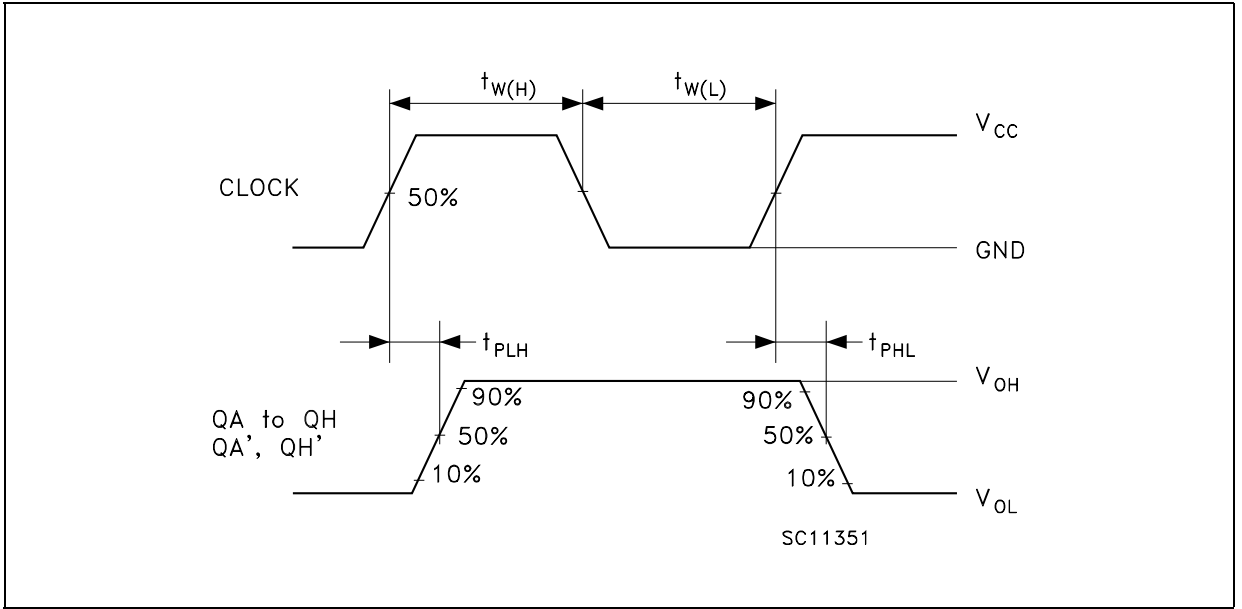


Figure 7: Waveform - Propagation Delays (f=1MHz; 50% duty cycle)

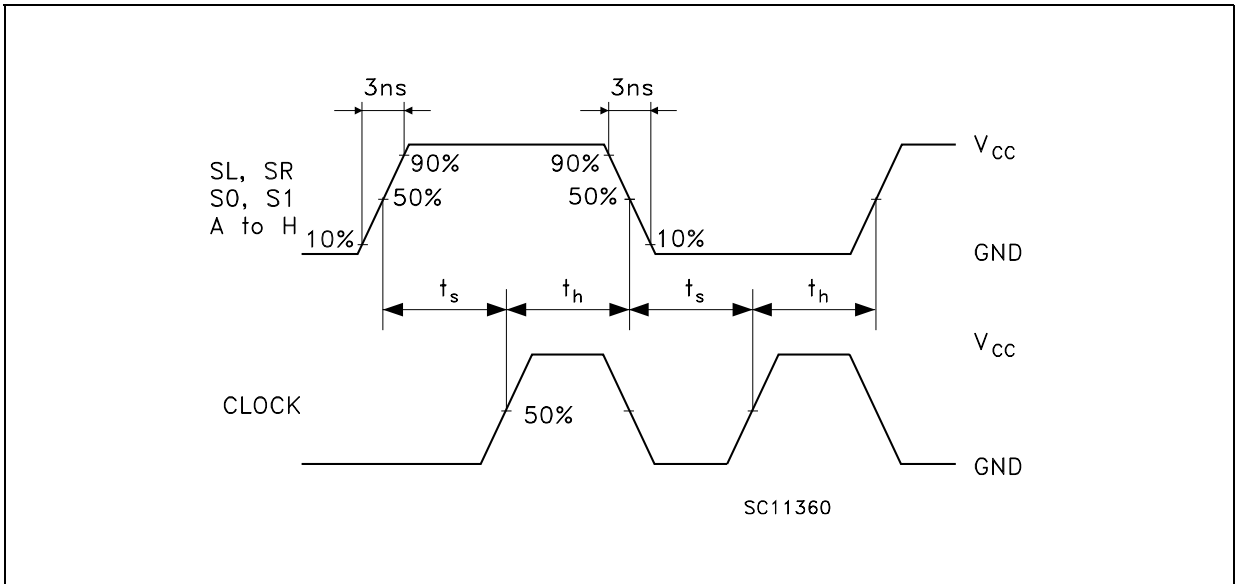
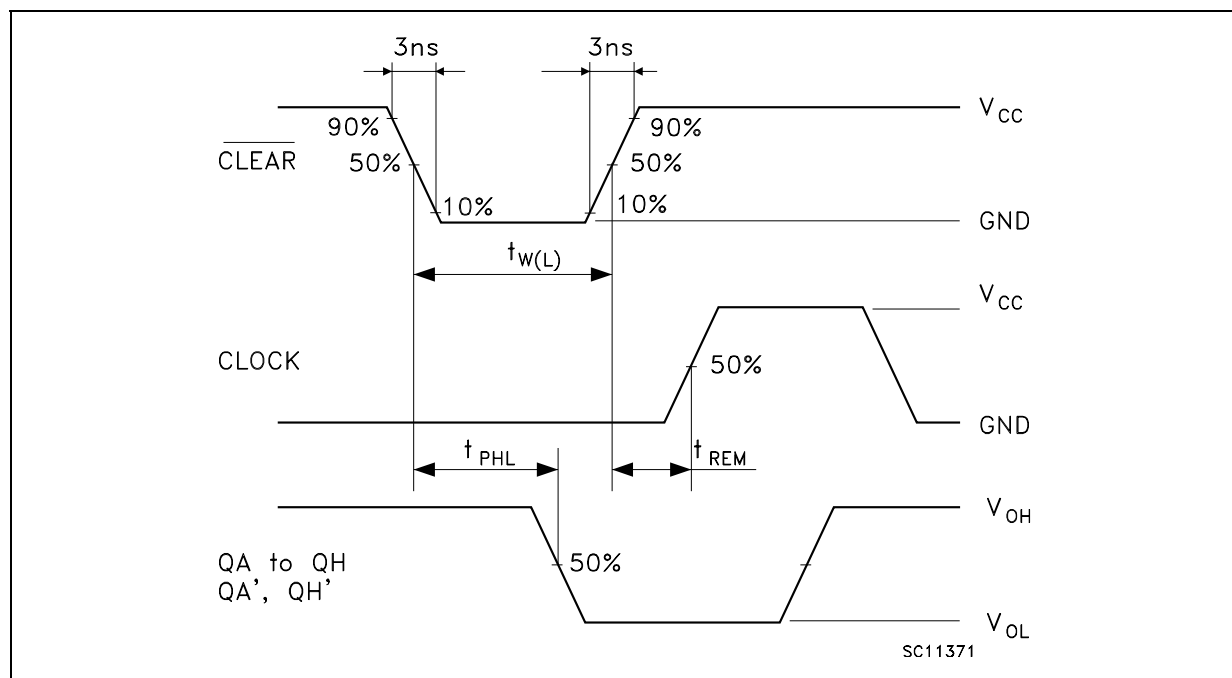
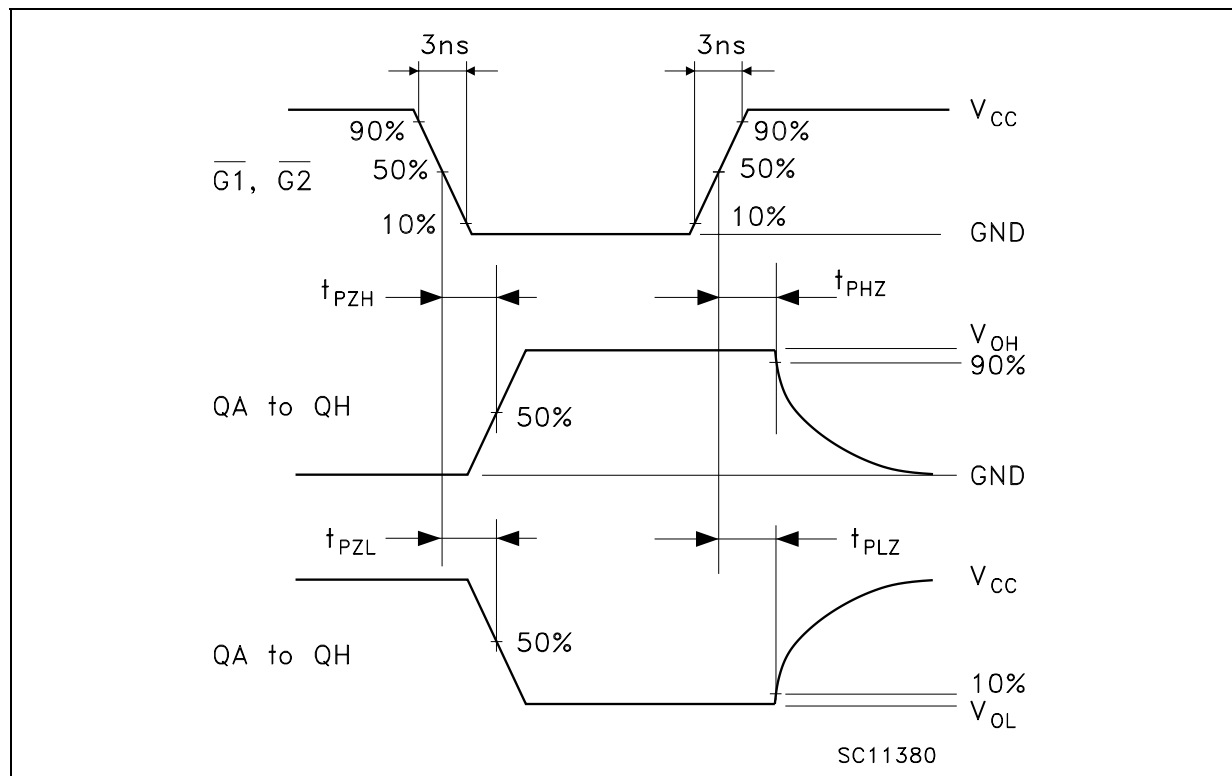
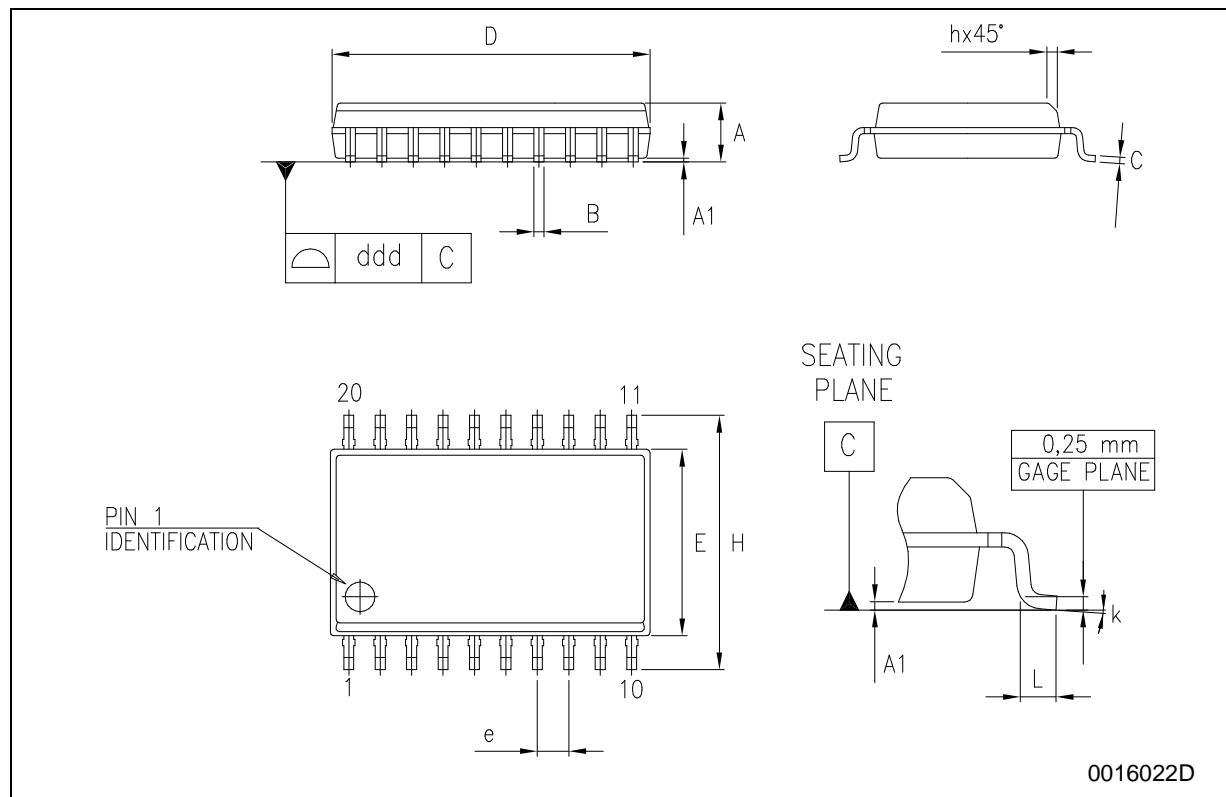


Figure 8: Waveform - Propagation Delays ($f=1\text{MHz}$; 50% duty cycle)Figure 9: Waveform - Propagation Delays ($f=1\text{MHz}$; 50% duty cycle)

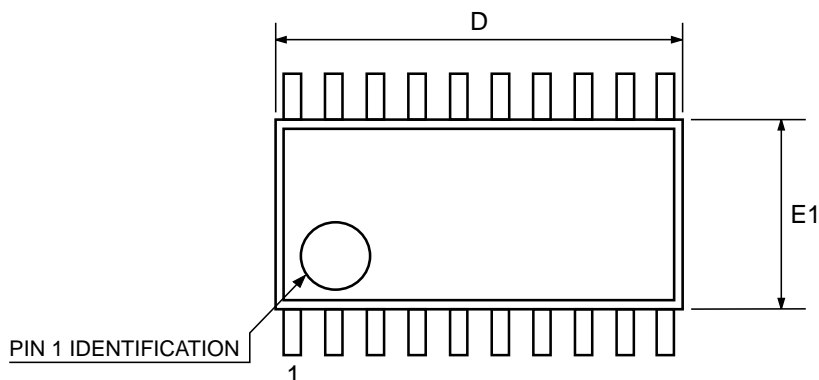
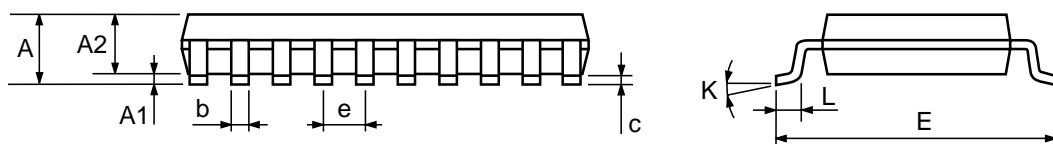
SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



TSSOP20 MECHANICAL DATA

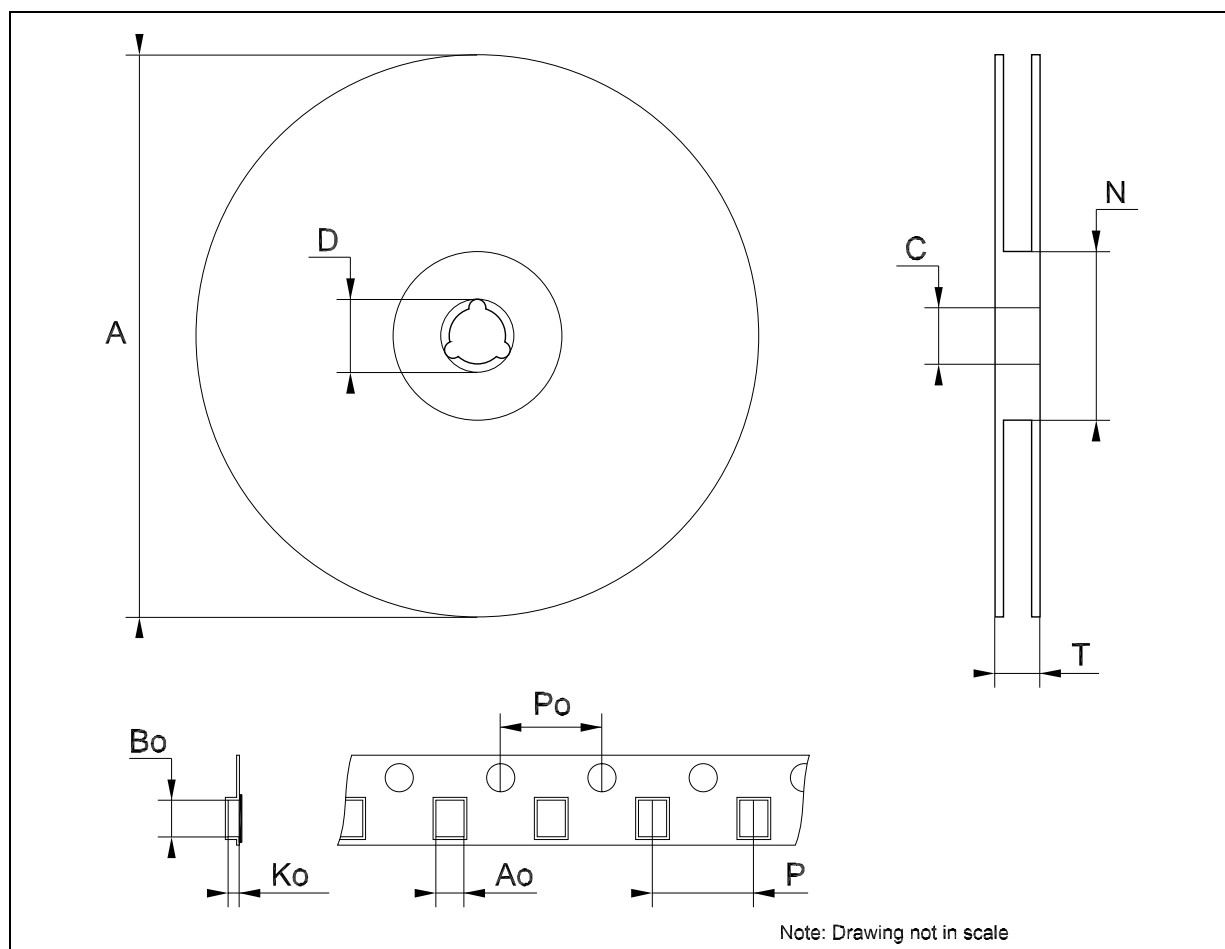
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0087225C

Tape & Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

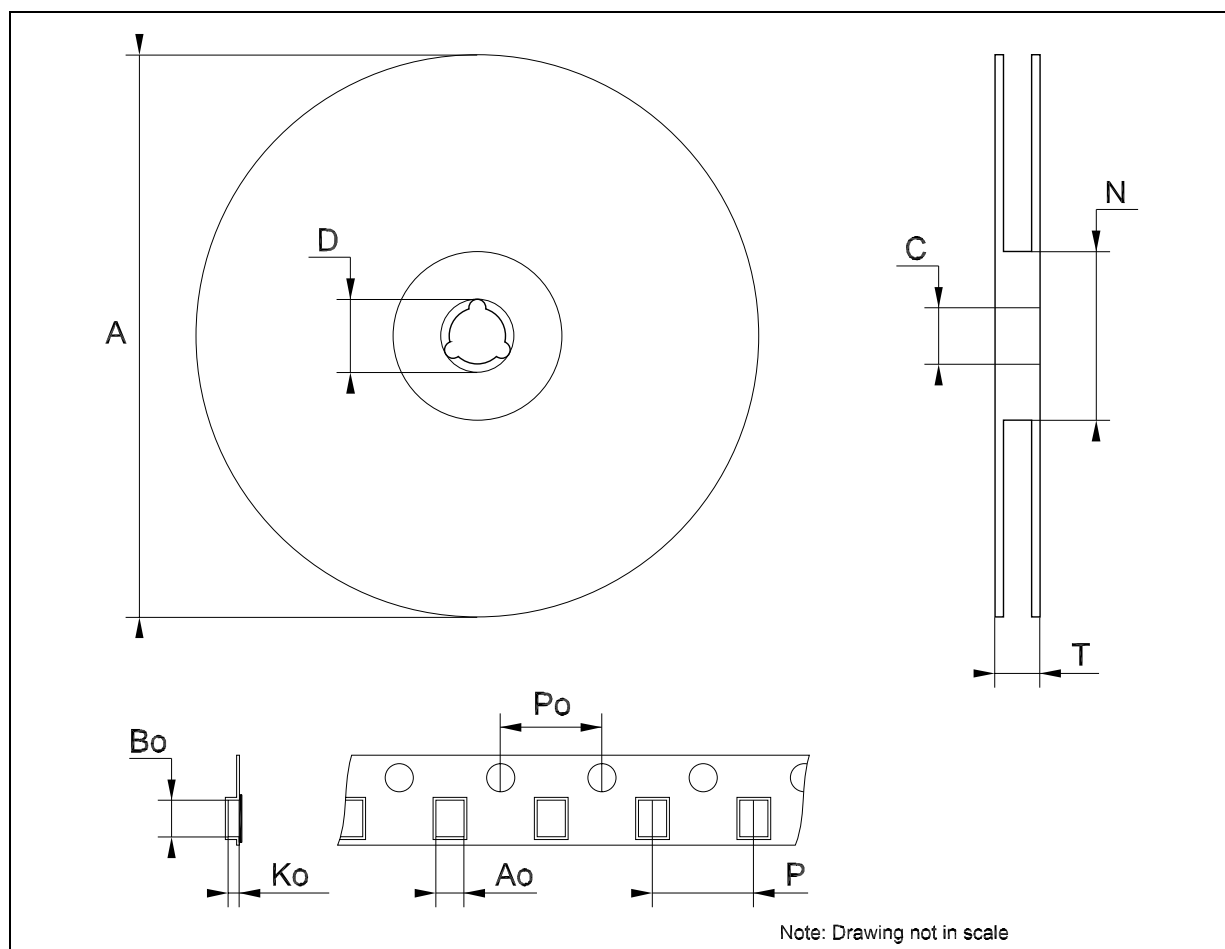


Table 10: Revision History

Date	Revision	Description of Changes
29-Jul-2004	2	Ordering Codes Revision - pag. 1.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com