PCI 6350

Asynchronous 32-bit PCI–to–PCI Bridge

Connectivity

- PCI r3.0 compatible
- 3.3V signaling including 5V input signal tolerance
- 32-bit, 66MHz Asynchronous operation
- Support for 9 Bus Masters
- PQFP and BGA packages

Performance

- Flow-Thru zero wait state burst up to 4 KB for optimal large volume data transfer
- 192 buffering bytes (data FIFO)
- Two-entry 64-byte upstream Posted Write buffer
- Two-entry 32-byte downstream Posted Write buffer
- Two-entry 64-byte upstream Read Data buffer
- One-entry 32-byte downstream Read Data buffer
- Out-of-order delayed transactions
- Serial EEPROM loadable and programmable PCI Read-Only register configurations
- External arbiter or programmable arbitration for nine bus masters on secondary interface support
- Ten secondary clock outputs with pin controlled enable and individual maskable control
- Four GPIO pins with output control and power-up status latch capable
- Enhanced address decoding
- 32-bit I/O Address range
- ISA Aware mode for legacy support in the first 64 KB of I/O Address range
- VGA addressing and palette snooping support
- IEEE Standard 1149.1-1990 JTAG interface for boundary scan test
- Industry-standard 208-pin (ball) Plastic Quad Flat Pack (PQFP) or 256-pin (ball) Plastic Ball Grid Array (PBGA) package
- Address Stepping hardcoded to two clocks
- Multiple IDs check all Device and Revision IDs
- ISA I/O—Added decode of legacy ISA devices
- Added optional flow-through enable
- Fast back-to-back enable—Read-only supported

High Performance Asynchronous 32-bit, 66MHz, PCI–to–PCI Bridge for Cost-sensitive Applications

The PLX FastLane™ PCI 6350 is an asynchronous, 32-bit, 66MHz PCI-to-PCI bridge for enhanced cost-effective bridging for add-in cards in image processing, video capture, PCI I/O expansion, storage or network servers, telecommunication, networking, and embedded appl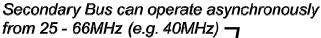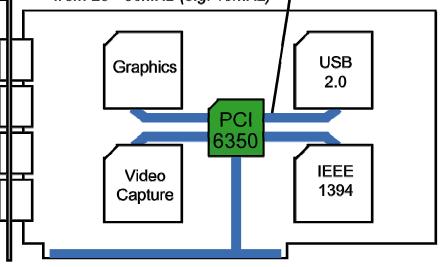ications. And, like all PLX interconnect chips, the PLX PCI 6350 is supported by best-of-class, comprehensive reference design tools, along with PLX's industry-recognized support infrastructure. The PCI 6350 is designed for applications such bus load /PCI slot expansion, and frequency conversion from slower PCI to faster PCI buses or vice versa, using Asynchronous bridging.

Asynchronous bridging is a key feature of the PCI 6350, in which the primary and secondary buses can operate at independent frequencies. In addition, the PCI 6350 includes sophisticated buffer management and buffer configuration options designed to provide customizable performance optimization. All of this is in an industry-standard pin-out, which is compatible with the PCI 6150 and 21150-type devices. The PCI 6350 is available in both PQFP and BGA packages with a lead-free ROHS compliant option.
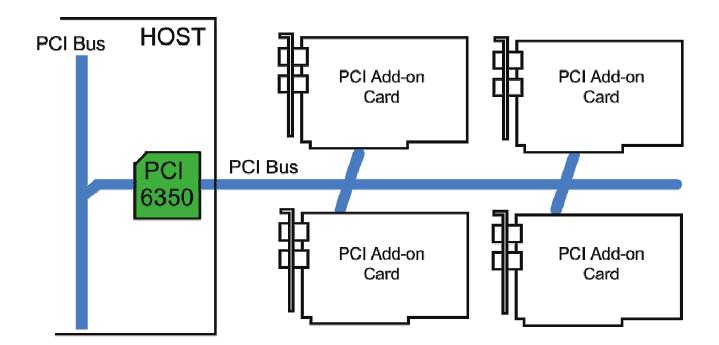

Figure 1. Asynchronous PCI Bridging

Figure 2. Bus Load Expansion Example

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Product Ordering Information

Part Number	Description
PCI 6350-AA66PC	PCI 6350 PCI-to-PCI Bridge Chip (PQFP)
PCI 6350-AA66PC G	PCI 6350 PCI-to-PCI Bridge Chip (PQFP) (Lead Free)
PCI 6350-AA66BC	PCI 6350 PCI-toPCI Bridge Chip (BGA)
PCI 6350-AA66BC G	PCI 6350 PCI-toPCI Bridge Chip (BGA) (Lead Free)
PCI 6350RDK	Flexible development platform for PCI 6350-based PCI-to-PCI Bridging designs.

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for more information.