74ALVC541

Octal buffer/line driver; 3-state

Rev. 02 — 5 November 2007

1. General description

The 74ALVC541 is an octal non-inverting buffer/line drivers with 3-state bus compatible outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}0$ and $\overline{OE}1$. A HIGH on $\overline{OE}$n causes the outputs to assume a high-impedance OFF-state.

2. Features

- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.5 V)
  - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2 000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1.   Ordering information

| Type number	Package			
	Temperature range	Name	Description	Version
74ALVC541D	−40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC541PW	−40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC541BQ	−40 °C to +85 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1

NXP
founded by Philips

4. Functional diagram
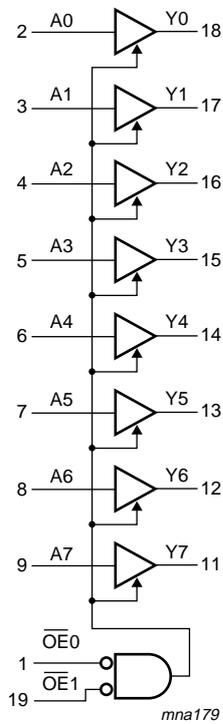
Fig 1. Logic symbol
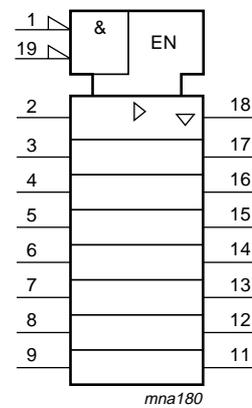
Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

74ALVC541

OE0 [1] □ 20 V_{CC}
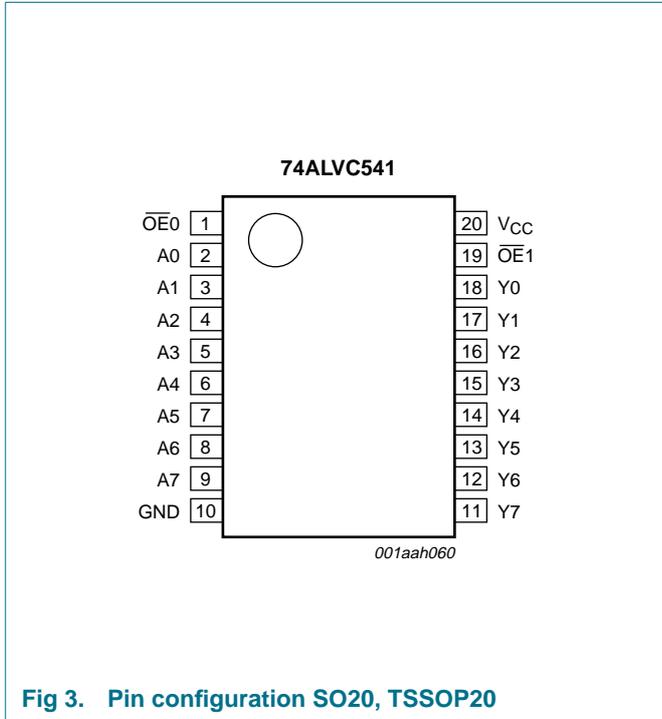
Fig 3. Pin configuration SO20, TSSOP20

74ALVC541

Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.
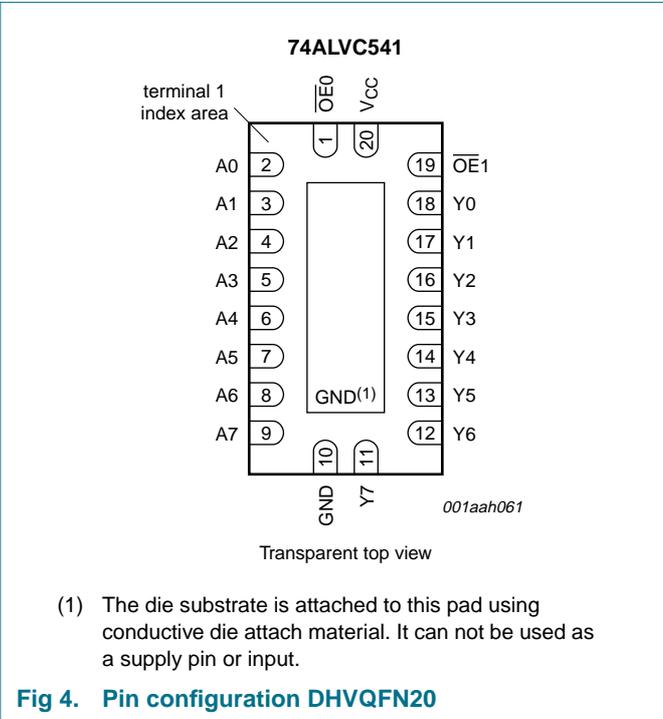
Fig 4. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE0}$	1	output enable input (active LOW)
A[0:7]	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y[0:7]	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE1}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3.   Functional table[1]

Control		Input	Output
$\overline{OE0}$	$\overline{OE1}$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

[1]   H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+4.6	V
V_I	input voltage			−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	[1]	−50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	−0.5	$V_{CC} + 0.5$	V
		output 3-state	[2]	−0.5	+4.6	V
		power-down mode, $V_{CC} = 0$ V	[3]	−0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			−100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C				
	SO20 package		[4]	-	500	mW
	TSSOP20 package		[5]	-	500	mW
	DHVQFN20 package		[6]	-	500	mW

[1]   The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2]   The output voltage ratings may be exceeded if the output current ratings are observed.

[3]   When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 3.6 V in normal operation.

[4] P_{tot} derates linearly with 8 mW/K above 70 °C.

[5] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[6] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

74ALVC541_2

Product data sheet   **Rev. 02 — 5 November 2007**   **4 of 15**

8. Recommended operating conditions

Table 5. **Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		power-down mode, $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		−40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. **Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ µA; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = 6$ mA ; $V_{CC} = 1.65$ V	1.25	-	-	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	1.8	-	-	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	2.2	-	-	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	2.4	-	-	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	2.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ µA; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = -6$ mA ; $V_{CC} = 1.65$ V	-	-	0.3	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	-	-	0.4	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	-	-	0.6	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	-	-	0.4	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	-	-	0.4	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	-	-	0.55	V
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	±0.1	±10.0	µA

Table 6.   Static characteristics …*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 3.6$ V	-	±0.1	±5.0	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	±0.1	±10.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	0.2	10	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0$ V to 3.6 V; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A;	-	5	750	μA
C_I	input capacitance		-	3.5	-	pF

[1]   All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

10. Dynamic characteristics

Table 7.   Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	An to Yn; see Figure 5 [2]				
		$V_{CC} = 1.65$ V to 1.95 V	1.0	3.0	4.6	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	2.2	3.3	ns
		$V_{CC} = 2.7$ V	1.0	2.5	3.3	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	2.3	3.0	ns
t_{en}	enable time	$\overline{OE}$n to Yn; see Figure 6 [2]				
		$V_{CC} = 1.65$ V to 1.95 V	1.0	4.2	7.5	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	3.3	5.4	ns
		$V_{CC} = 2.7$ V	1.0	3.7	5.8	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	3.3	4.9	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Figure 6 [2]				
		$V_{CC} = 1.65$ V to 1.95 V	1.0	4.8	7.5	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	3.1	4.5	ns
		$V_{CC} = 2.7$ V	1.0	3.1	4.8	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	2.9	4.6	ns

74ALVC541_2

Product data sheet   **Rev. 02 — 5 November 2007**   6 of 15

Table 7. **Dynamic characteristics** *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	−40 °C to +85 °C			Unit
			Min	**Typ[1]**	**Max**	
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]				
		outputs enabled	-	25	-	pF
		outputs disabled	-	0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

 t_{en} is the same as t_{PZL} and t_{PZH}.

 t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

 N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms
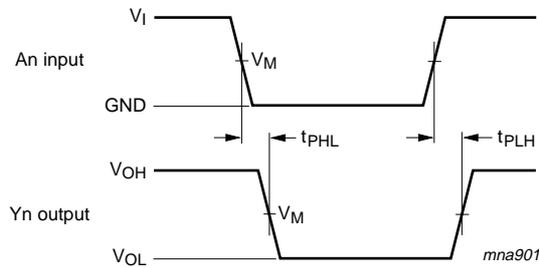
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

**Fig 5.** **Propagation delay input (An) to output (Yn)**
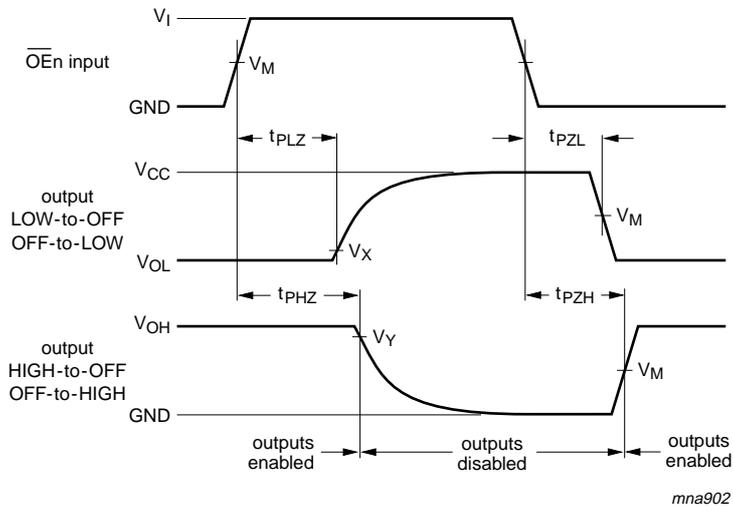
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
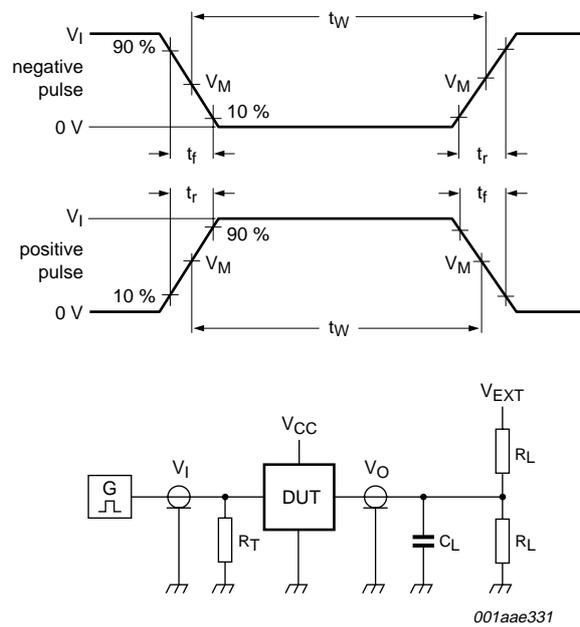
Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

Fig 7. Load circuitry for switching times

Table 9.   Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6	GND

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

**Fig 8. Package outline SOT163-1 (SO20)**

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[2]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19
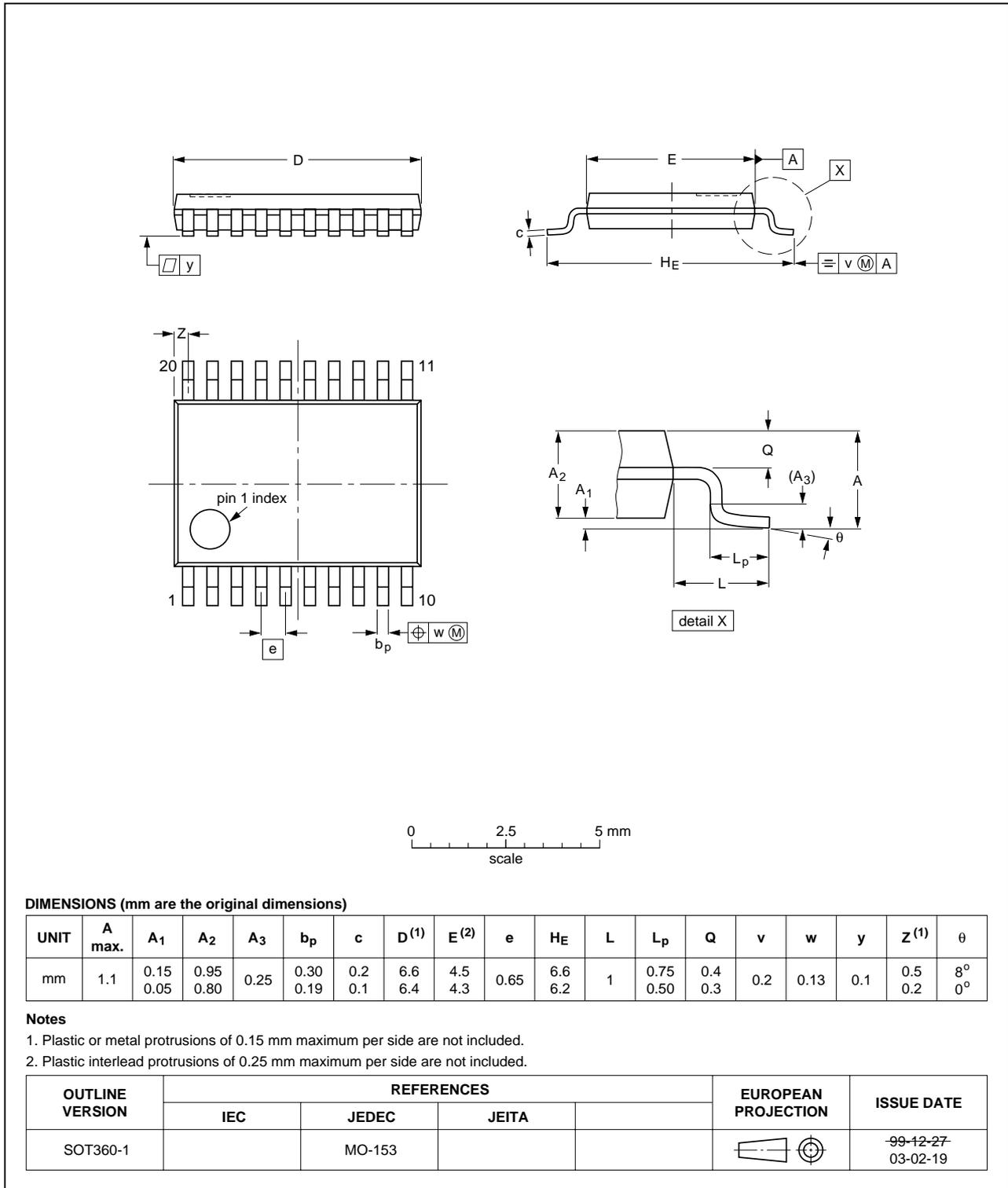
Fig 9. Package outline SOT360-1 (TSSOP20)

74ALVC541_2

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27
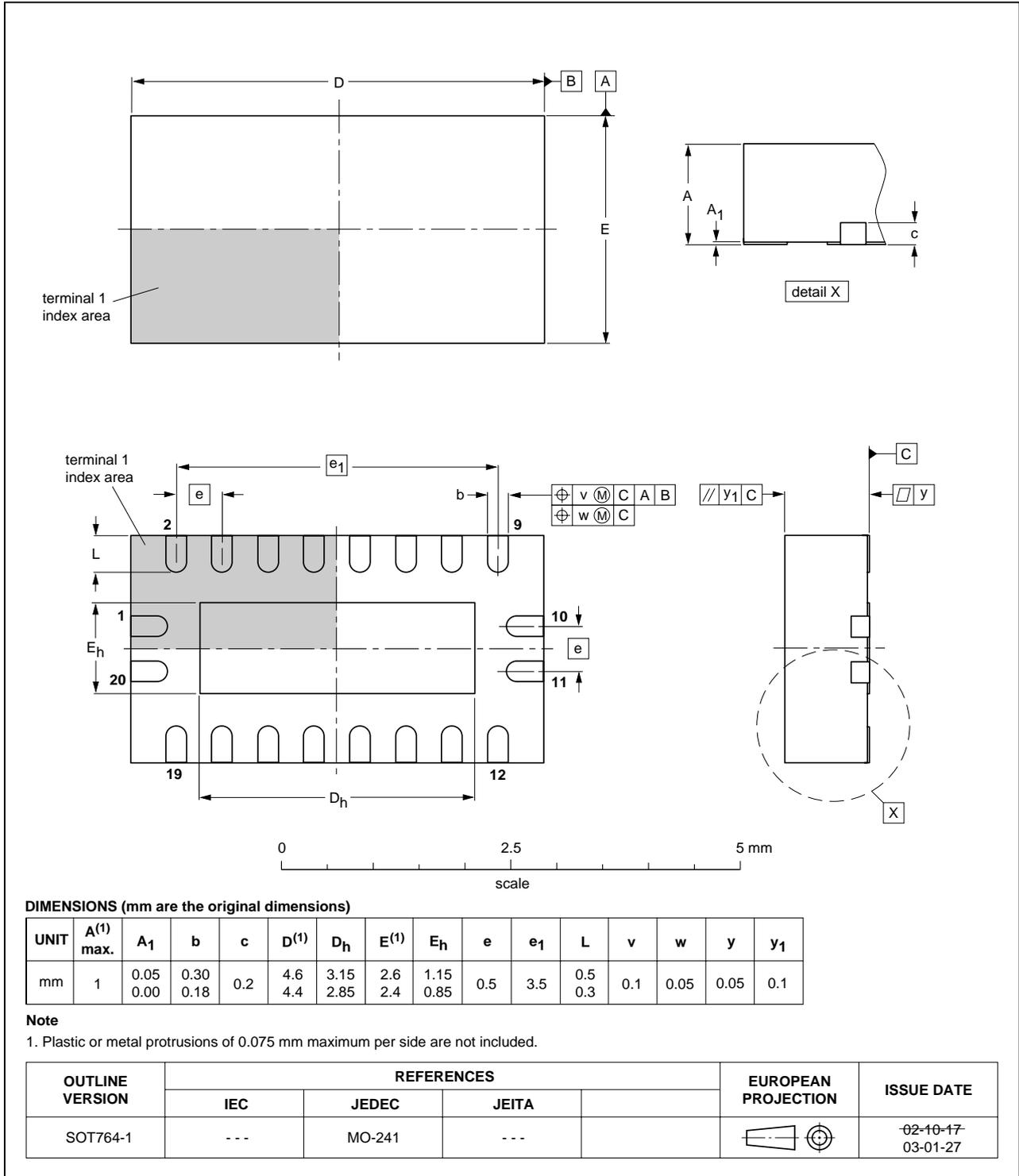
Fig 10. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10.   Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC541_2	20071105	Product data sheet	-	74ALVC541_1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Section 3: DHVQFN20 package added. - Section 8: derating values added for DHVQFN20 package. - Section 12: outline drawing added for DHVQFN20 package.			
74ALVC541_1	20020226	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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74ALVC541_2

Product data sheet

Rev. 02 — 5 November 2007

14 of 15

17. Contents