4-BIT TELEPHONE CONTROLLER

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1. GENERAL DESCRIPTION

The W742S819 is a high-performance 4-bit micro-controller (μC) that provides an LCD driver and three OpAmps. The device contains a 4-bit ALU, two 8-bit timers, two dividers (for two oscillators) in dual-clock operation, a 24 × 8 LCD driver, six 4-bit I/O ports (including 1 output port for LED driving), three OpAmps(Operational Amplifiers), and one channel DTMF generator. There are also five interrupt sources and 16-levels subroutine nesting for call subroutine or interrupt applications. The W742S819 operates on very low current and has two power reduction modes, that is the dual-clock slow operation and STOP mode, which help to minimize power dissipation.

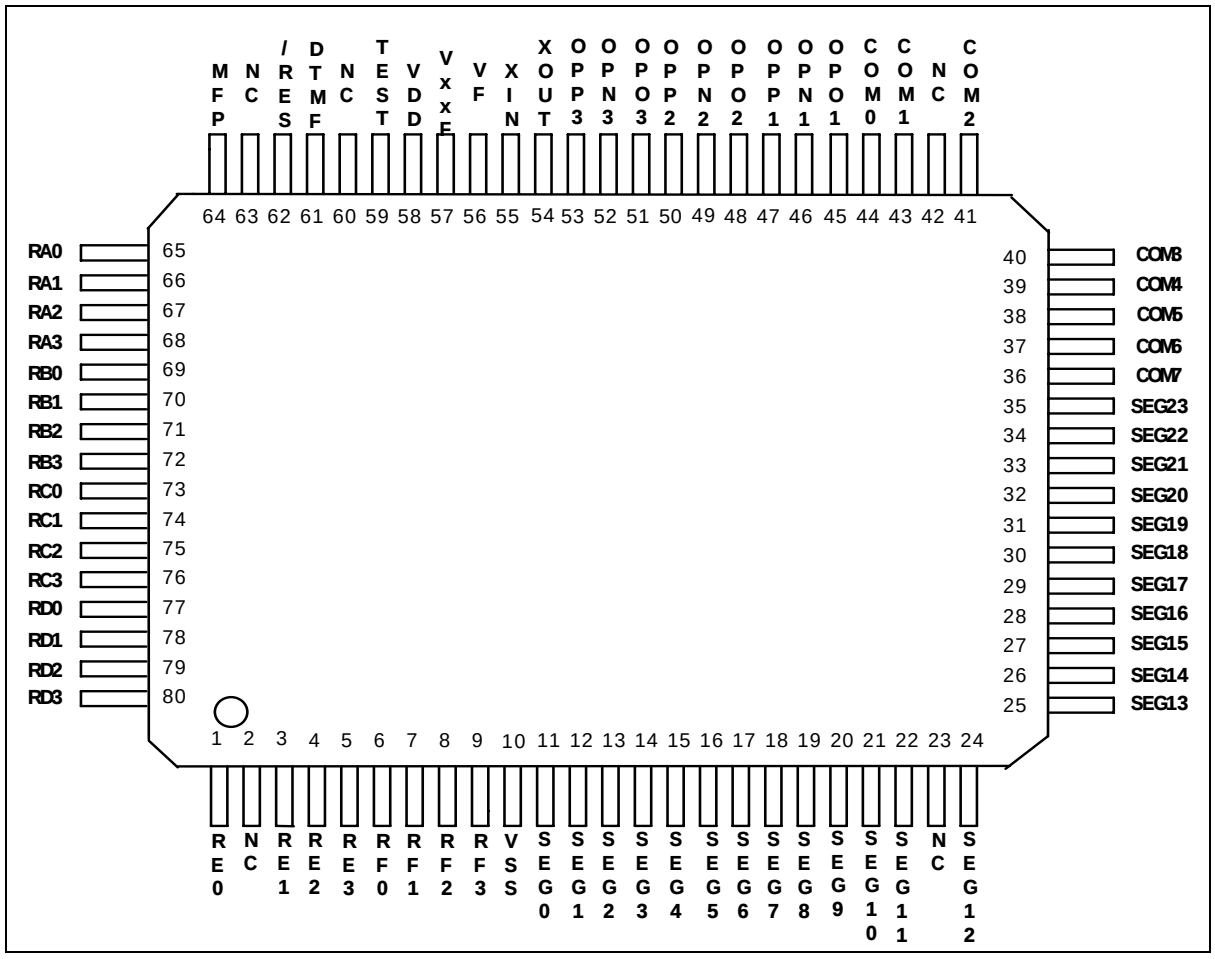
2. FEATURES

- Operating voltage: 2.4V - 5.5V
- Dual-clock operation mode (Connect to 32768 Hz crystal only)
  - Fslow oscillator : 32768Hz OSC
  - Ffast oscillator : PLL (Phase Lock Loop) output enable
- Memory
  - 12288 x 16 bits program ROM (including 48K x 4 bit look-up table)
  - 1536 x 4 bits data RAM (including 16 nibbles x 16 pages working registers)
  - 24 x 8 LCD data RAM
- 24 input/output pins
  - Port for input only: 1 ports/4 pins(RC)
  - Input/output ports: 3 ports/12 pins(RA, RB & RD)
  - High sink current output port for LED driving: 1 port /4 pins(RE)
  - Port for output only: 1 ports/4 pins(RF)
- Power-down mode
  - Hold function: no operation (excluding Fslow and Fosc oscillator)
  - Stop function: no operation (Fslow and Fosc oscillator are stopped)
  - Dual-clock slow operation mode: system is operated by 32768Hz (FOSC=Fslow and Ffast stopped)
- Five types of interrupts
  - Four internal interrupts (Divider0, Divider1, Timer 0, Timer 1)
  - One external interrupts (RC Port)
- LCD driver output
  - 24 segments x 8 commons
  - 1/8 duty, 1/3 bias driving mode by option code
  - 16 level software LCD contrast adjusting
- MFP output pin
  - Output is software selectable as modulating or non-modulating frequency
  - Works as frequency output specified by Timer 1
- DTMF output pin (PLL should be enable in this function)
  - Output is one channel Dual Tone Multi-Frequency signal for dialing
- Three OpAmps(Operational Amplifiers)
  - Three general purpose OpAmps with positive inputs, negative inputs and outputs.

- Two built-in 14-bit frequency dividers
  - Divider0: the clock source is the output of the Fosc-oscillator
  - Divider1: the clock source is the output of the Fslow-oscillator
- Two built-in 8-bit programmable countdown timers
  - Timer 0: one of two internal clock frequencies (FOSC/4 or FOSC/1024) can be selected
  - Timer 1: with auto-reload function and one of three internal clock frequencies (FOSC, FOSC/64 or Fslow) can be selected by MR1 register; and the specified frequency can be delivered to MFP pin
- Built-in 18/15-bit watchdog timer selectable for system reset; enable the watch dog timer or not is determined by code option
- Build-in Power-on reset detested circuit
- Powerful instruction set: 1XX instructions
- 16-levels subroutine (include interrupt) nesting

3. PIN CONFIGURATION

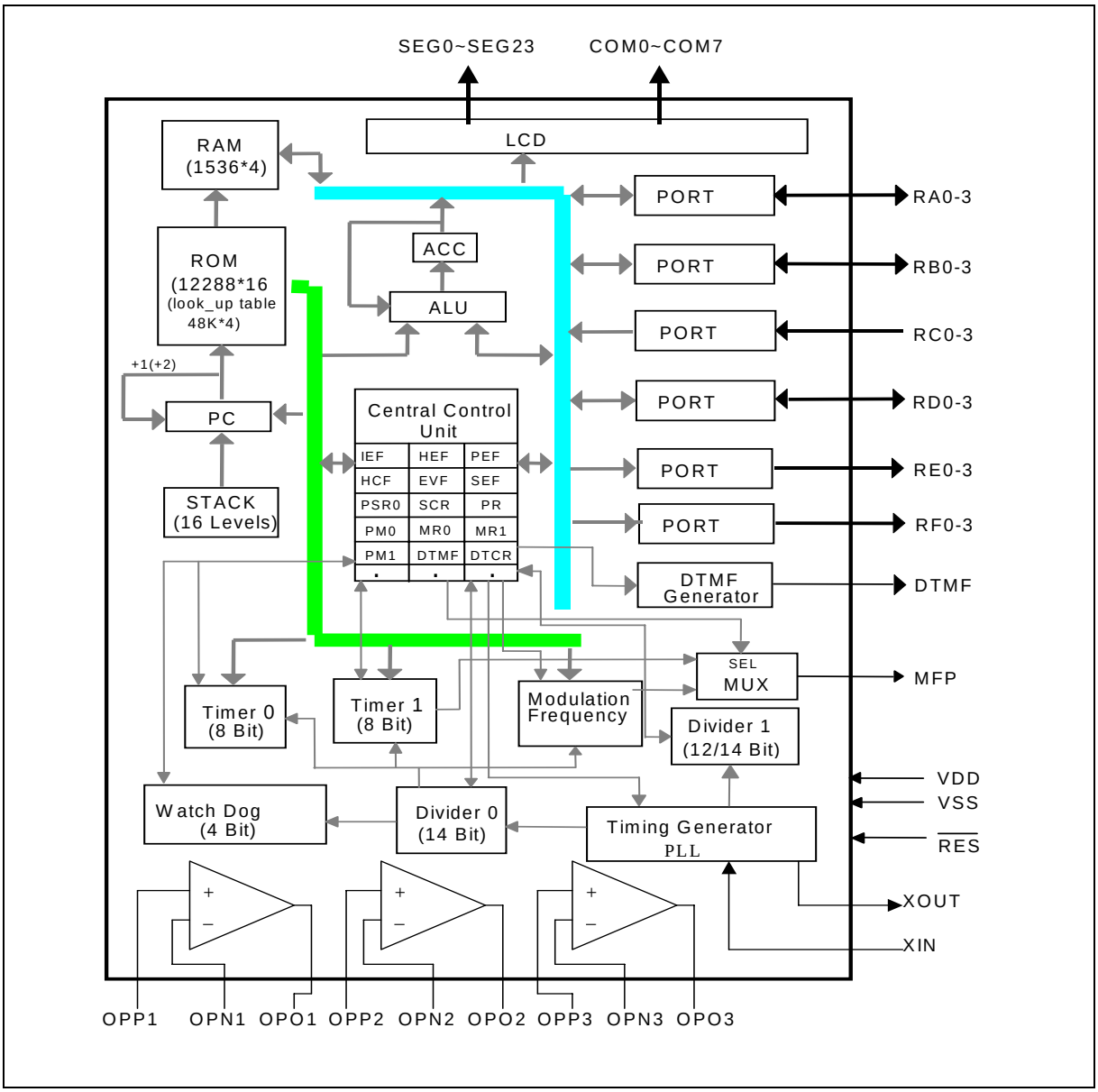
For W742S819 QFP 80 pin



4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
XIN	I	Input pin for 32.768 Hz oscillator. Connected to 32.768 KHz crystal only.
XOUT	O	Output pin for 32.768 Hz oscillator. Connected to 32.768 KHz crystal only.
VXXF	I	Regulator for PLL circuit. Connected capacitor (10 uF) to VSS.
VF	I	Low pass filter for PLL circuit. Connected capacitor 0.022uF to VSS.
RA0-RA3	I/O	Input/Output port. Input/output mode specified by port mode 1 register (PM1). Internal pull-up resistors specified by RAM 7FEH(Refer to chapter 6.16.5)
RB0-RB3	I/O	Input/Output port. Input/output mode specified by port mode 2 register (PM2). Internal pull-up resistors specified by RAM 7FFH (Refer chapter 6.16.5)
RC0-RC3	I	4-bit port for input only. Each pin has an independent interrupt capability.
RD0-RD3	I/O	Input/Output port. Input/output mode specified by port mode 5 register (PM5).
RE0-RE3	O	Output port only. With high sink current capacity for the LED application.
RF0-RF3	O	Output port only.
MFP	O	Output pin only. This pin can output modulating or nonmodulating frequency, or Timer 1 specified frequency. It can be selected by bit 0 of BUZCR (BUZCR.0).
DTMF	O	This pin can output dual-tone multi frequency signal for dialing.
$\overline{\text{RES}}$	I	System reset pin with low active.
SEG0-SEG23	O	LCD segment output pins.
COM0- COM7	O	LCD common signal output pins. The LCD alternating frequency can be selected by code option.
OPP1~3	I	OpAmp1~3 positive input pins
OPN1~3	I	OpAmp1~3 negative input pins
OPO1~3	O	OpAmp1~3 output pins
TEST	I	For IC testing. Connected to Vss in normal usage.
V_{DD}	I	Positive power supply (+).
V_{SS}	I	Negative power supply (-).

5. BLOCK DIAGRAM



6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

7. DC CHARACTERISTICS

7.1 DC CHARACTERISTICS: VDD-VSS=3.0V

(VDD-VSS = 3.0 V, Ffast = 3.6042MHz, Fslow = 32.768 KHz, Ta = 25° C, LCD on; Power-on reset circuit active, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	2.4	-	5.5	V
Op. Current (Crystal type)	I_{OP1}	No load (Ext-V) All OpAmps disabled In dual-clock normal operation.	-	0.7	1.0	mA
Op. Current (Crystal type)	I_{OP3}	No load (Ext-V) All OpAmps disabled In dual-clock Fslow operation and Ffast is stopped	-	-	65	μA
Op. Current (Crystal type)	I_{OP4}	No load (Ext-V) All OpAmps enabled In dual-clock Fslow operation and Ffast is stopped	-	-	75	μA
Hold Current (Crystal type)	I_{HM1}	Hold mode No load (Ext-V) All OpAmps disabled In dual-clock normal operation	-	-	450	μA

DC CHARACTERISTICS: VDD-VSS=3.0V, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hold Current (Crystal type)	I_{HM3}	Hold mode No load (Ext-V) All OpAmps disabled In dual-clock Fslow operation and Ffast is stopped	-	31	45	μA
Hold Current (Crystal type)	I_{HM4}	Hold mode No load (Ext-V) All OpAmps enabled In dual-clock Fslow operation and Ffast is stopped	-	65	75	μA
Stop Current (Crystal type)	I_{SM1}	Stop mode No load (Ext-V) All OpAmps disabled LCD driver should be turned off	-	8	12	μA
Input Low Voltage	V_{IL}	-	V_{SS}	-	$0.3V_{DD}$	V
Input High Voltage	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V
MFP Output Low Voltage	V_{ML}	I_{OL} = 3.5mA	-	-	0.4	V
MFP Output High Voltage	V_{MH}	I_{OH} = 3.5mA	2.4	-	-	V
MFP Sink Current	I_{ML}	V_{OL} = 0.9V	9	-	-	mA
Port RA, RB and RD Output Low Voltage	V_{ABL}	I_{OL} = 2.0mA	-	-	0.4	V
Port RA, RB and RD Output high Voltage	V_{ABH}	I_{OH} = 2.0mA	2.4	-	-	V
LCD Supply Current	I_{LCD}	All Seg. ON	-	-	45	μA
SEG0-SEG31 Sink Current (Used as LCD output)	I_{OL1}	V_{OL} = 0.4V V_{LCD} = 0.0V	90	-	-	μA
SEG0-SEG31 Drive Current (Used as LCD output)	I_{OH1}	V_{OH} = 2.4V V_{LCD} = 3.0V	90	-	-	μA
Port RE Sink Current	I_{EL}	V_{OL} = 0.9V	9	-	-	mA
Port RE Source Current	I_{EH}	V_{OH} = 2.4V	0.4	1.2	-	mA
DTMF Output DC level	V_{TDC}	R_L=5KΩ, V_{DD}=2.5 to 3.8V	1.1	-	2.8	V

DC CHARACTERISTICS: VDD-VSS=3.0V, continued

PARAMETER		SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF Distortion		THD	RL=5KΩ, VDD=2.5 to 3.8V	-	-30	-23	dB
DTMF Output Voltage		VTO	Low group, RL=5KΩ	130	150	170	mVrms
Pre-emphasis			Col/Row	1	2	3	dB
DTMF Output Sink Current		ITL	VTO=0.5V	0.2	-	-	mA
Pull-up Resistor		RC	Port RC	100	350	1000	KΩ
Pull-up Resistor		RA	Port RA	100	350	1000	KΩ
Pull-up Resistor		RB	Port RB	100	350	1000	KΩ
OP-AMPs	Input Leakage Current	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	1	μA
	Input Resistance	R_{IN}		10	-	-	MΩ
	Input Offset Voltage	V_{OS}		-	-	25	mV
	Power Supply Rejection Ratio	PSRR	1KHz 0.1V_{PP} ripple on V_{DD}	40	-	-	dB
OP1	Maximum Capacitive Load	C_L		-	-	30	pF
	Minimum Resistive Load	R_L		500	-	-	KΩ
OP2 OP3	Maximum Capacitive Load	C_L		-	-	20	pF
	Minimum Resistive Load	R_L		1000	-	-	KΩ

7.2 DC CHARACTERISTICS: VDD-VSS=3.6V

(VDD-VSS = 3.6 V, Ffast = 3.6042MHz, Fslow = 32.768 KHz, Ta = 25° C, LCD on; Power-on reset circuit active, unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Current (Crystal type)	I_{OP1}	No load (Ext-V) All OpAmps disabled In dual-clock normal operation.	-	0.8	1.0	mA
Op. Current (Crystal type)	I_{OP3}	No load (Ext-V) All OpAmps disabled In dual-clock Fslow operation and Ffast is stopped	-	-	65	µA
Op. Current (Crystal type)	IOP4	No load (Ext-V) All OpAmps enabled In dual-clock Fslow operation and Ffast is stopped	-	-	85	µA
Hold Current (Crystal type)	I_{HM1}	Hold mode No load (Ext-V) All OpAmps disabled In dual-clock normal operation	-	-	450	µA
Hold Current (Crystal type)	I_{HM3}	Hold mode No load (Ext-V) All OpAmps disabled In dual-clock Fslow operation and Ffast is stopped	-	34	45	µA
Hold Current (Crystal type)	I_{HM4}	Hold mode No load (Ext-V) All OpAmps enabled In dual-clock Fslow operation and Ffast is stopped	-	75	85	µA
Stop Current (Crystal type)	I_{SM1}	Stop mode No load (Ext-V) All OpAmps disabled LCD driver should be turned off	-	8	12	µA

8. AC CHARACTERISTICS

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Frequency	F_{OSC}	Crystal type	-	32768	-	KHz
PLL Frequency	Ffast	PLL enable	-	3.6042	-	MHz
Instruction cycle time	T_I	One machine cycle	-	4/F_{OSC}	-	S
Reset Active Width	T_{RAW}	F_{OSC}=32.768 KHz	1	-	-	µS
Interrupt Active Width	T_{IAW}	F_{OSC}=32.768 KHz	1	-	-	µS

9. APPLICATIONS INFORMATION

9.1 Operating Voltage

The chip can be operated from 2.4V-5.5V. If users have much consideration for low power operation, lower voltage supply system can be a better choice.

9.2 Drive Abilities of OP-AMPs

The OP-AMPS have 2 types according to their drive abilities. OP2 and OP3 have weaker drive abilities than which OP1 does, so OP2 and OP3 are provided for driving input port like RC.n.

9.3 FSK Signal Detection and FSK Demodulation

9.3.1 FSK Signal Detection

Figure 10-1 is a typical application circuit for FSK signal detection and FSK demodulation. For purpose of signal detection, user should enable both OP1 and OP2, output low to control and sense the signal by RC.n.

9.3.2 FSK demodulation

For purpose of FSK demodulation, user should enable both OP1 and OP2, output high to control, and sense the FSK signal by RC.n. and demodulate FSK by software.

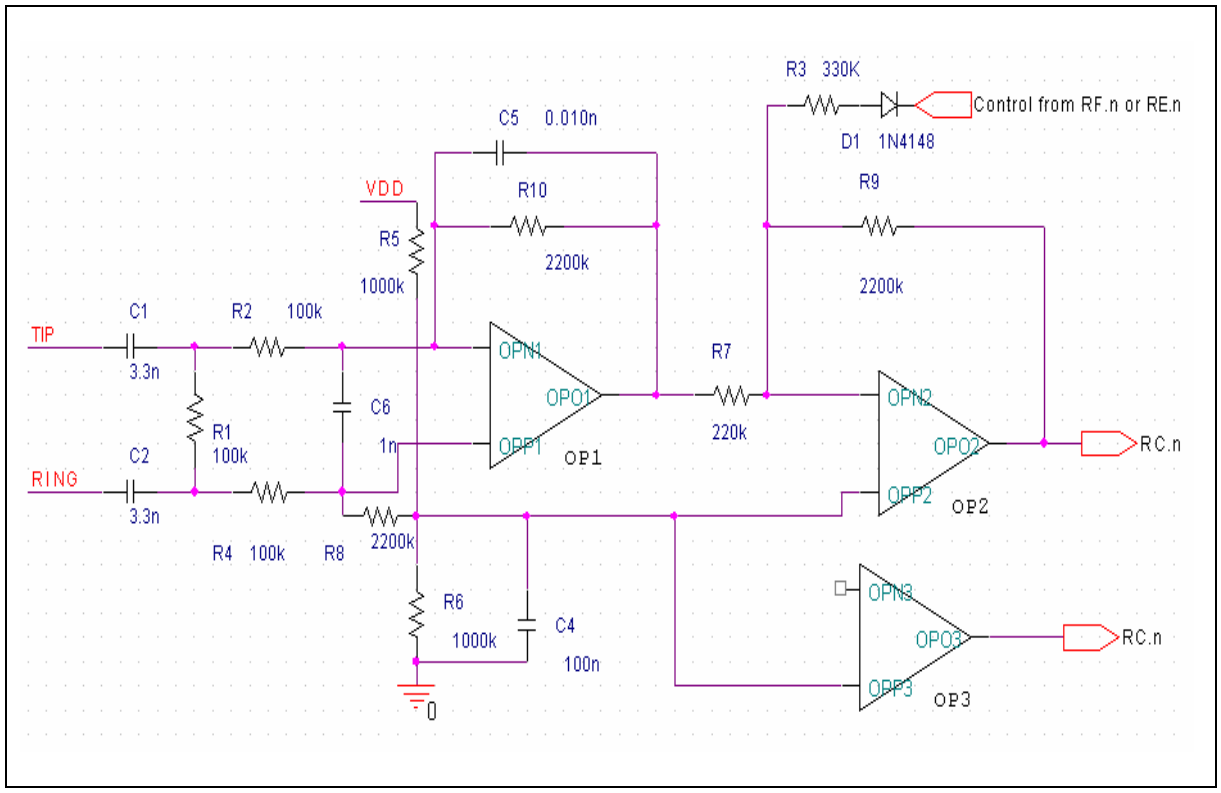


Figure 9-1 Application Circuit for FSK Signal Detection and FSK demodulation

10. REVISION HISTORY

VERSION	DATE	PAGE	MODIFICATION
A1	Aug. 23, 2005	-	Initial data

Important Notice

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