SC2542
High Performance Wide Input Range Dual Synchronous Buck Controller

POWER MANAGEMENT

Description

SC2542 is a high performance dual PWM controller. It is designed to convert a widely ranged battery rail down to two independent output rails. The PWM operation of the two channels are 180 degrees out of phase which can greatly reduce the size and the cost of the input capacitors. Synchronous buck PWM topology and voltage mode control allow fast transient response and flexible component selection for easy designs. A 5V standby regulator is integrated. A 10V internal linear regulator provides the bias for the controller, and this voltage is optimized for gate drivers to deliver high efficiency.

The light load efficiency can be greatly improved by turning off the low side MOSFET upon reversal of inductor current. There is no need for a current sensing resistor because the MOSFET on resistance is used as the sensing element. Under extreme light load conditions, the device will operate in a pulse skip mode. The switching frequency can be dropped significantly to a level programmed by external resistors. The battery energy is better utilized with these efficiency enhancement schemes.

The power sequencing is fully supported including independent start up and power good output. In shutdown mode the controller only draws 100nA from the supply. The controller also offers full protection features for the conditions of under voltage, over voltage, and over current. The switching frequency is adjustable from 100KHz to 300KHz. TSSOP-28-EDP package is offered.

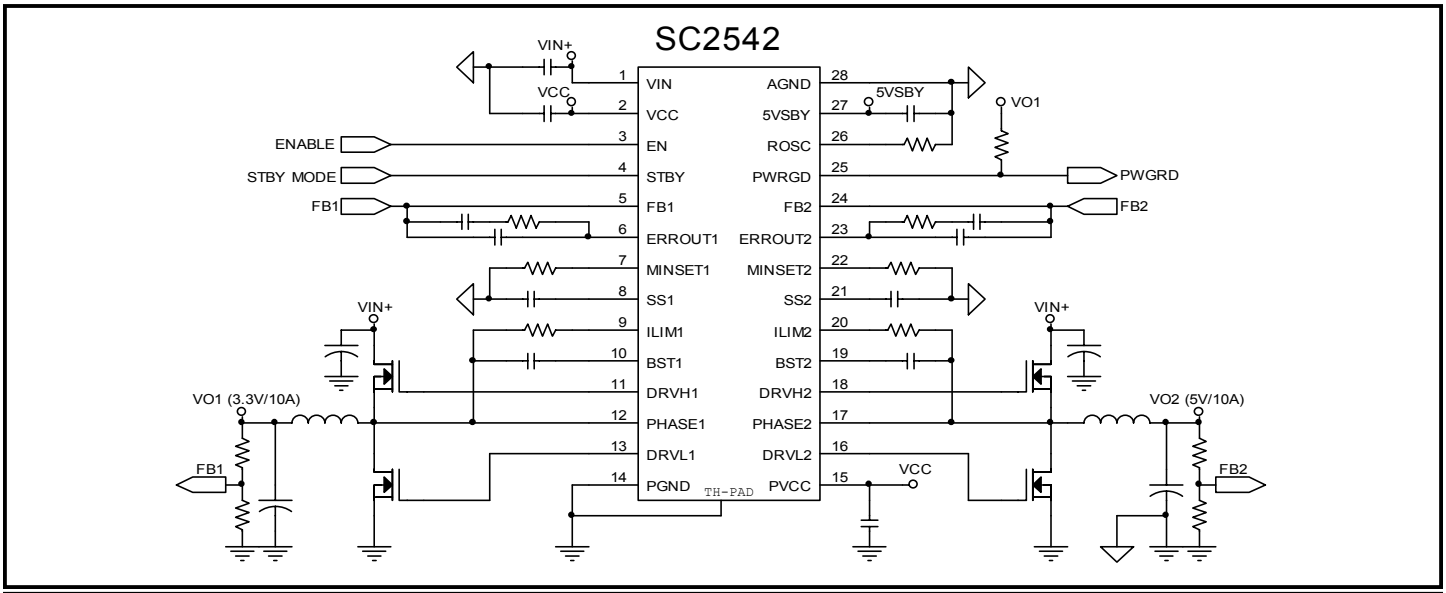
Features

- Independent dual-switcher-outputs
- Integrated 5V standby output with over 50mA capability
- Wide input voltage range: 6.5V ~ 28V
- Adjustable output voltage down to 0.75V
- Light load efficiency enhancement
- Programmable skip mode operation
- Flexible power sequencing with enable and power good output
- Synchronous buck topology with voltage mode control
- Out of phase operation to reduce cost of input capacitor
- 10V internal regulator for gate driver to deliver high efficiency
- Programmable switching frequency: 100KHz ~ 300KHz
- Full protection: UVLO, OVP, and programmable OCP
- No need for current sense resistor
- Low standby operating current (200µA typical)
- Low shut down current (100nA typical)
- 28 lead TSSOP package with exposed die pad (EDP)
- Fully WEEE package and RoHS Compliant

Applications

- Notebook computer system power
- Systems with 6.5V ~ 28V input
- Network and telecom systems
- Other portable devices

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
BST1, BST2 to PGND	V_{BST}	38	V
VIN to PGND	V_{IN}	28	V
ILIM1 and ILIM2 to PGND		VIN	V
VCC and PVCC to PGND		14	V
PGND to AGND		± 0.3	V
BST1 to PH1, BST2 to PH2, DRVH1 to PH1, DRVH2 to PH2		-0.3 to 14	V
DRVL1, DRVL2 to PGND		-0.3 to VCC	V
EN to PGND		-0.3 to VIN	V
All other pins to AGND		-0.3 to VCC	V
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-60 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	3	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W
Lead Temperature (Soldering) 10 Sec.	T_{SOLDER}	260	°C
PHASE to AGND pulse (100nS) peak voltage		-3	V
DRVL to AGND pulse (100nS) peak voltage		-3	V

Note: (1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IN} = 16V, F_S = 200KHz.

Parameter	Test Conditions	Min	Typ	Max	Unit
Undervoltage Lockout					
Start Threshold	VCC rising	5.25	5.5	5.75	V
UVLO Hysteresis	hysteresis		400		mV
Power Supply					
Operating Current (I_{IN} - I_{PVCC})	SS1/SS2, EN = high, F_S = 200 KHz		7	12	mA
PVCC Operating Current	F_S = 200KHz, 1nF on TG and BG		14		mA
VCC Regulated	V_{IN} > 12V		10		V
VCC Load Regulation	Load current 0 to 20mA		2		%
Standby Supply Current	STBY mode		200	350	µA
Shutdown Supply Current	Shutdown mode		0.1	10	µA

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{IN} = 16V, F_S = 200KHz.

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply (Cont.)					
5VSBY Regulation	0A < load current < 50mA	4.85	5	5.15	V
5VSBY Line Regulation	V_{IN} = 12V ~ 28V		1		%
5VSBY Current Limit Threshold			100		mA
Minimum 5VSBY Output Capacitance	0A < load current < 50mA		1		µF
Main Switcher Output					
Line Regulation	7V < VIN < 28V		0.5		%
Load Regulation	0A < load current < 10A, MINSET pin float		0.5		%
Output Voltage Accuracy	Without feedback attenuation, T_A = -40° C to +85° C	0.735	0.750	0.765	V
ENABLE					
EN High Threshold Voltage				2	V
EN Low Threshold Voltage		0.6			V
STBY					
STBY High Threshold Voltage				2	V
STBY Low Threshold Voltage		0.6			V
Soft Start					
Soft Start Charge Current			85		µA
Soft Start Discharge Current			15		µA
Disable Threshold Voltage for DRVL Out of Tri-state	Pull below this level, turning ON DRVL (Turn ON low side FET)		0.65		V
Error Amplifier					
Voltage Feedback Reference	T_A = -40° C to +85° C	0.735	0.750	0.765	V
Input Bias Current (Source)				2	µA
Open Loop Gain (1)			70		dB
Unity Gain Bandwidth (1)			3		MHz
Output Source/Sink Current			1		mA
Slew Rate (1)	100pF capacitive loading		10		V/µS
PWM Comparator to Output Delay (1)			75		nS

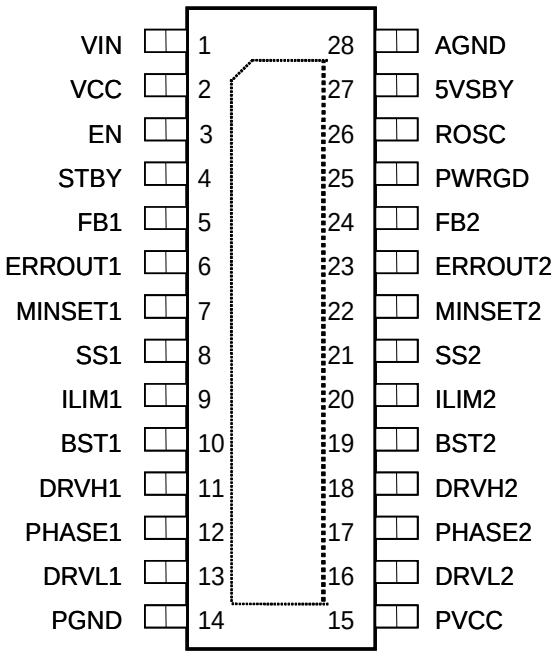
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{IN} = 16V, F_S = 200KHz.

Parameter	Test Conditions	Min	Typ	Max	Units
Oscillator					
Frequency Range per Phase		100		300	KHz
Oscillator Frequency per Phase	R_{OSC} = 73K Ω	175	210	245	KHz
Minimum OFF Time		300	400		nS
Oscillator Ramp Peak Voltage			3.0		V
Oscillator Ramp Valley Voltage			1		V
Current Limit					
ILIM Source Current		9	10	11	µA
ILIM Offset Voltage			2		mV
MINSET					
Minimum Pulse Width Set	V_{IN} = 16V, R = 107K Ω		1		µS
Minimum Pulse Width Set	V_{IN} = 8V, R = 107K Ω		2		µS
Minimum Pulse Width Set	V_{IN} = 16V, R = 53K Ω		500		nS
Duty Cycle					
PWM 1 & 2 Maximum Duty Cycle	R_{OSC} = 73k Ω		90		%
PWM 1 & 2 Minimum Duty Cycle	R_{OSC} = 73k Ω		0		%
Driver					
High Side Gate Drive (Source)	Source/Sink		0.5		A
Low Side Gate Drive (Source)	Source/Sink		0.5		A
Gate Drive Rise Time	C_{OUT} = 1000pF		30		nS
Gate Drive Fall Time	C_{OUT} = 1000pF		30		nS
Dead Time			80		nS
OVP					
OVP Threshold Voltage	Feedback voltage		0.89		V
Power Good					
Threshold Voltage	FB1 & FB2 rising		0.675		V
Threshold Voltage	FB1 & FB2 falling		0.57		V
Power Good Sink Capability	Sink 1mA			0.4	V

Pin Configuration

TOP VIEW



(28 Pin TSSOP-EDP)

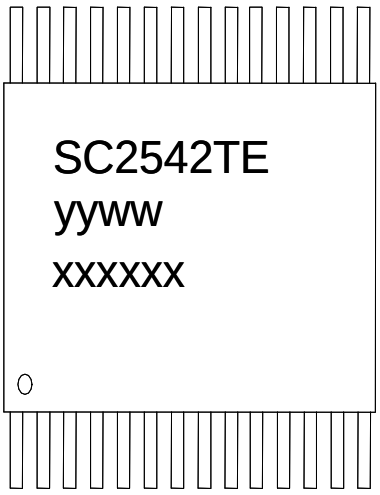
Ordering Information

Part Number	Package[1]	Temp. Range (T_A)
SC2542TETRT[2]	TSSOP-28-EDP	-40 to +85
SC2542EVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Marking Information

(TOP VIEW)



yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: P94A01)

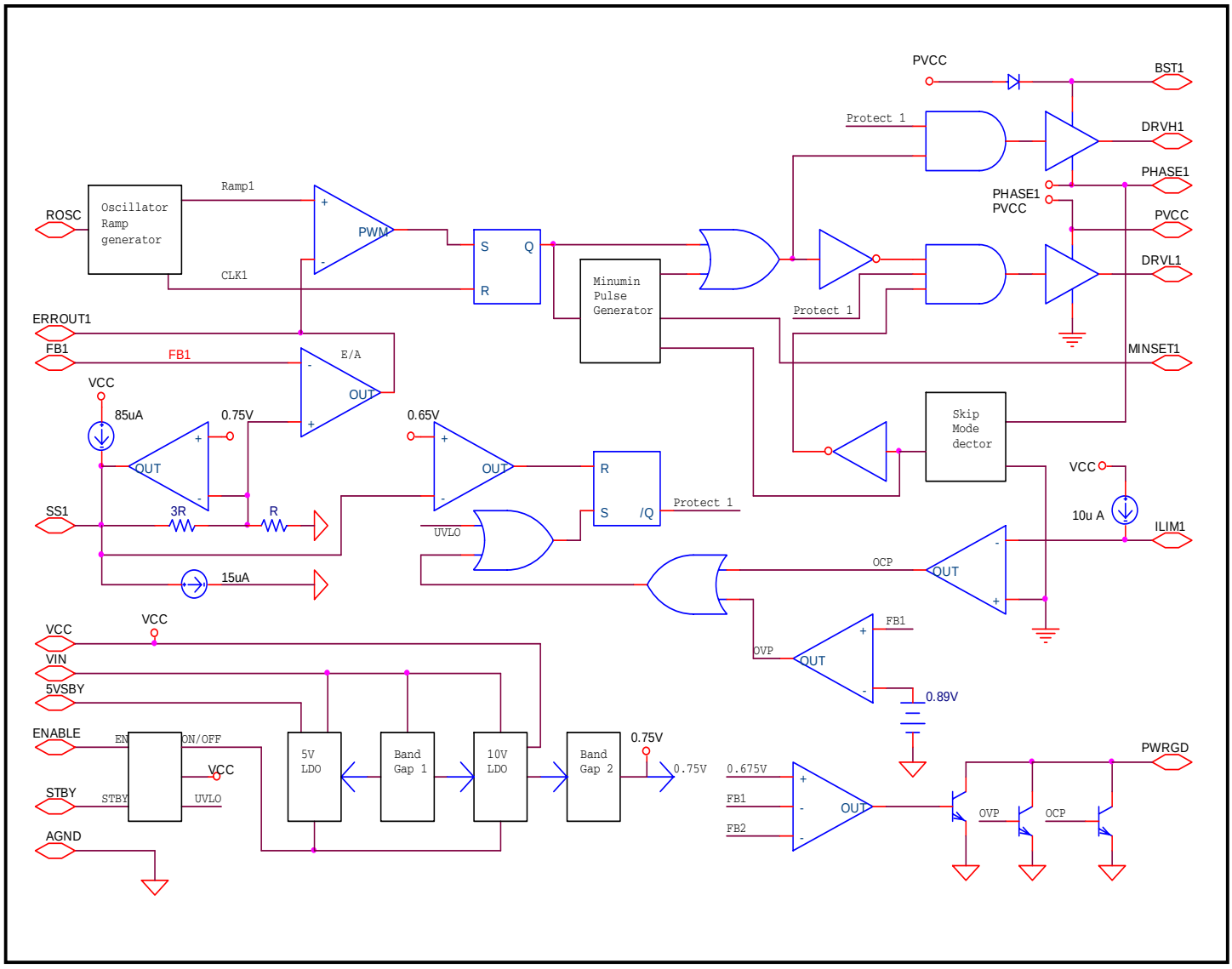
Pin Descriptions

Pin #	Pin Name	Pin Function
1	VIN	Input supply voltage. The range is from 6.5V to 28V.
2	VCC	10V regulator output. Supply voltage for chip bias and gate drivers.
3	ENABLE	TTL compatible level. Then ENABLE is low, all outputs are disabled. Typical shitdown current is 100nA.
4	STBY	When pulled low the 10V regulator and both switcher outputs are disabled. Only 5VSBY is available. Quiescent current is typically 200µA.
5	FB1	Negative input of the error amplifier for output 1.
6	ERROUT1	Error amplifier output for buck converter 1.
7	MINSET1	Connect external resistor from this pin to AGND to set the minimum pulse width in discontinuous mode. This also sets the operating frequency in skip mode for a given load.
8	SS1	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output1 by pulling this pin below 0.65V.
9	ILIM1	An external resistor connected from this pin to PHASE1 sets the overcurrent shutdown trip point.
10	BST1	Boost capacitor connection for OUTPUT1 high side gate drive. Connect an external capacitor as shown in the Typical Application Circuit.
11	DRVH1	Gate drive for the high side MOSFET of OUTPUT1. 180 degree out of phase with DRVH2.
12	PHASE1	Phase node for output 1.
13	DRVL1	Low side gate drive for output 1.
14	PGND	Power ground of low-side drivers.
15	PVCC	Supply voltage for low-side gate drivers.
16	DRVL2	Low-side gate drive for output 2.
17	PHASE2	Phase node for output 2.
18	DRVH2	Gate drive for the high side MOSFET of OUTPUT2. 180 degree out pf phase with GDRVH1.
19	BST2	Boost capacitor connection for the OUTPUT2 high side gate drive. Connect an external capacitors as shown in the Typical Application Circuit.
20	ILIM2	An external resistor connected from this pin to PHASE2 sets the overcurrent shutdown trip point.
21	SS2	An external capacitor connected from this pin to AGND sets the soft-start time. Disable output 2 by pulling this pin below 0.65V.
22	MINSET2	Connect one external resistor from this pin to AGND to set the minimum pulse width in discontinuous mode. This also sets the operating frequency in skip mode for a given load.
23	ERROUT2	Error amplifier output for buck converter 2.
24	FB2	Negative input of the error amplifier for output 2.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Function
25	PWRGD	Open collector output. Pulls low when eigher output is below the power good threshold level.
26	ROSC	An external resistor connected from this pin to AGND sets oscillator frequency.
27	5VSBY	5V regulator output. Disabled when ENABLE is pulled low.
28	AGND	Analog signal ground.
-	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram (Only Channel-1 shown)



Applications Information

General Description

The SC2542 is a fixed frequency dual voltage mode step-down PWM controller for adapter or battery operated systems. The two channels of the controller operate 180 degrees out of phase, which results in lower input current ripple and reduces the amount of input filtering capacitance needed.

Synchronous and "pulse skip" mode of operation are adopted in both switching channels to increase overall efficiency. The internal light-load current detection circuit and minimum pulse setting circuit determine the mode of operation and the "pulse skip" duration.

To extend battery life, the SC2542 features shutdown mode, where the quiescent current is 100nA (typical), and standby mode, where the 5V linear standby regulator is active and quiescent current is typically 200uA.

The functional block diagram is shown in Figure 1.

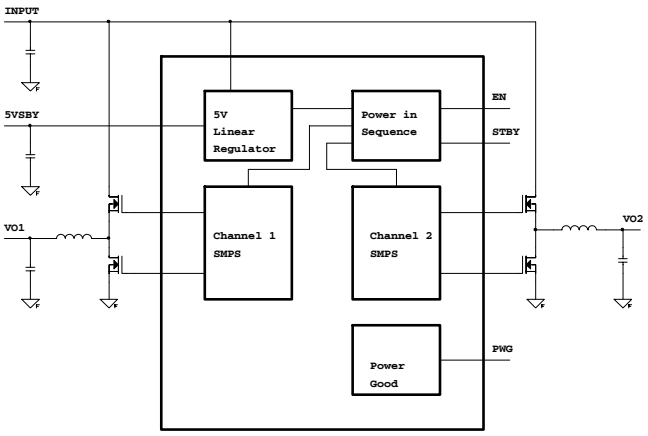


Figure 1. The functional block diagram.

Skip Mode Operation

When the RMIN pin is left open, the SC2542 operates as a synchronous PWM (SPWM) controller with the bottom MOSFET ON whenever the top MOSFET is OFF. Figure 2 shows the typical SPWM waveforms.

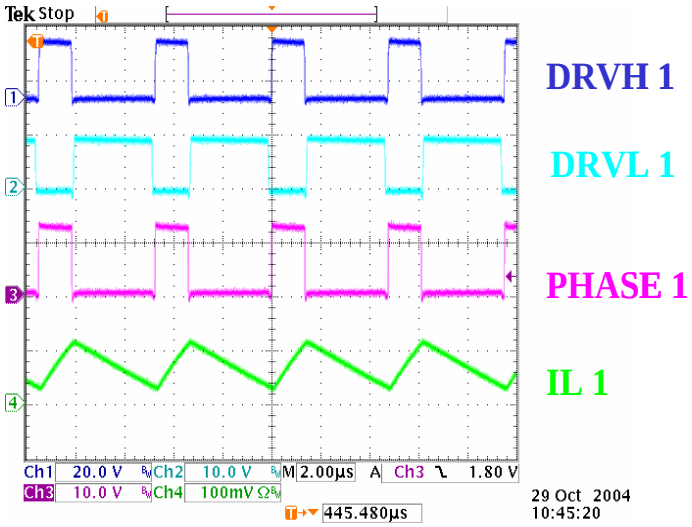


Figure 2. Typical waveforms of SPWM mode.

To enhance light-load efficiency, "pulse skip" mode (SKIP) can be enabled by placing a resistor from the RMIN pin to ground. For normal loads the controller will operate in SPWM mode, but when the load is light enough, the pulse widths of the top and bottom MOSFETs will be adjusted by the load condition. The SC2542 employs a simple circuit to detect the load condition by monitoring the PHASE node of the circuit. The PHASE node will start to turn positive if the inductor current begins to reverse (I_L < 0) signaling a light-load condition.

If a light-load condition is detected the SC2542 will operate in SKIP mode. Similar to a buck converter in discontinuous conduction mode (DCM), the converter will try to reduce its duty cycle as the load decreases. For example, it would start out with continuous conduction mode (CCM) duty cycle values, but as the load decreases, the duty cycle would try to shrink to zero as shown in Figure 3. However, the SC2542 clamps the DCM duty cycle to a minimum percentage (set by the RMIN resistor) of the CCM value. If the DCM duty cycle falls below this percentage, SKIP mode will be active.

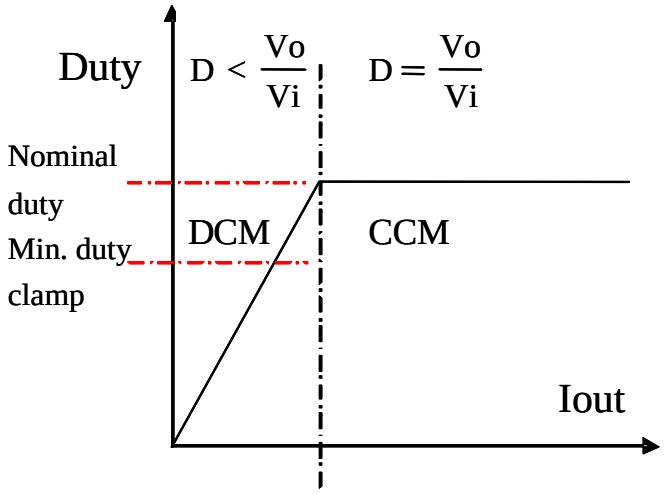


Figure 3. Conventional Buck converter duty cycle vs. load current.

Figure 4 further explains the basic theory of SKIP mode operation. When the load current falls from CCM to DCM, the duty cycle of DRVH (output of PWM comparator) will shrink. The programmed minimum pulse width of SC2542 with the DRVH signal to get the TG (top side MOSFET gate driver) pulse output. The TG output will maintain at least the programmed minimum pulse width. This TG pulse pumps up the output voltage causing the Error Amplifier output to decrease as the output voltage moves up. The PWM comparator may skip several cycles before sending another pulse when the output voltage drops down. The BG (bottom side MOSFET gate driver) output will terminate whenever the inductor current crosses zero.

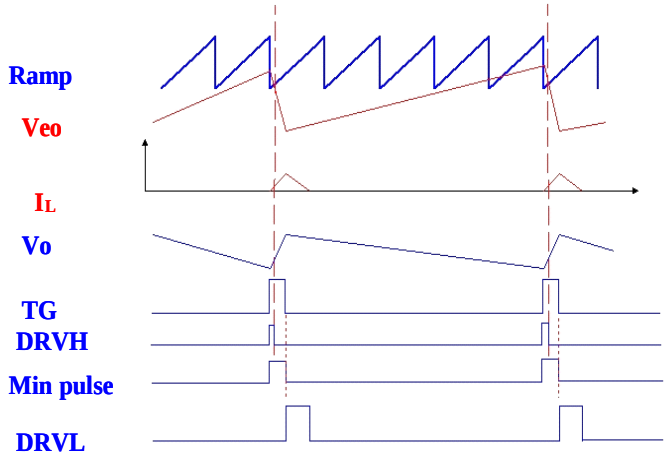


Figure 4. The waveforms of SKIP mode operation.

SKIP mode therefore leads to a reduction in the average switching frequency. MOSFET switching losses and driver losses, both of which are proportional to frequency, are significantly reduced at these light loads resulting in increased efficiency. SKIP mode also reduces the circulating currents associated with SPWM mode. The test result (Figure 5) shows the efficiency improvement in SKIP mode.

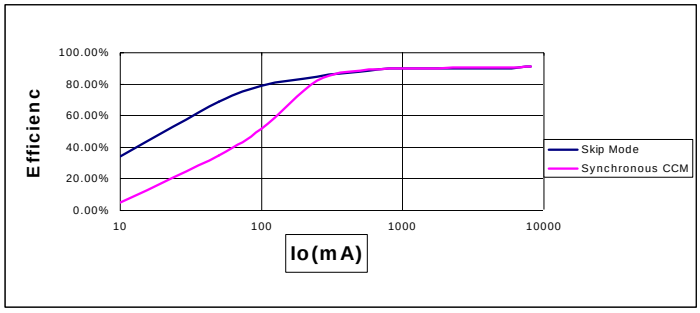
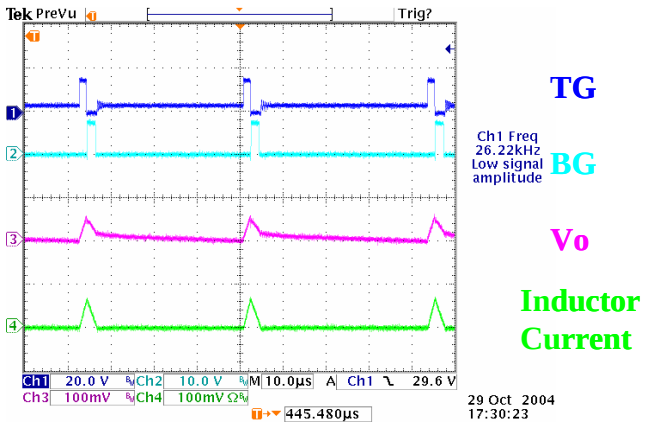
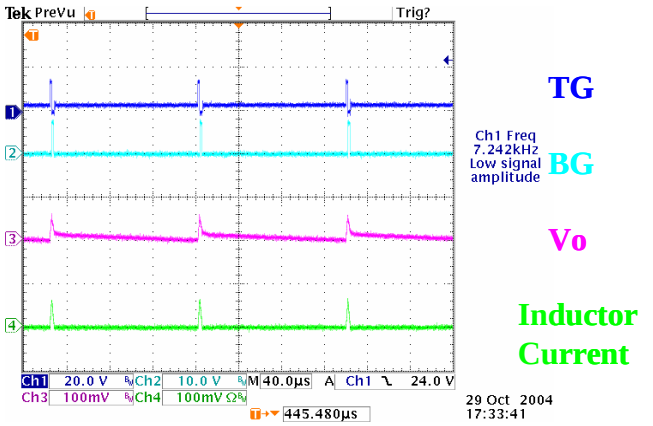


Figure 5. Skip mode improves light load efficiency.

Figure 6 (a) and (b) show typical waveforms of SKIP mode at different light load conditions. The frequency can actually fall very low at very light loads. When the switching frequency drops to the acoustic frequency range, very minor acoustic frequency noise might be generated, but the level of the noise is usually very low due to very small flux excursion in the magnetics. The acoustic noise can be totally avoided by using well constructed magnetics or by knowing the minimum system loads to program the SKIP mode operation accordingly.



(a)



(b)

Figure 6. Typical waveforms of SKIP mode.

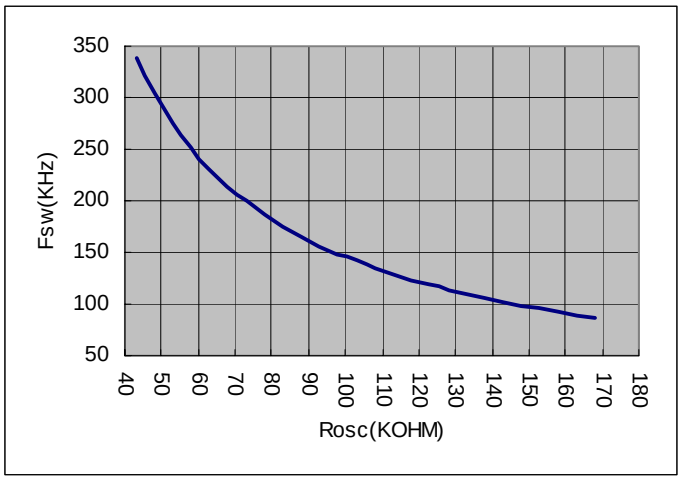


Figure 7. Switching frequency versus Rosc.

Frequency Setting

The frequency of the SC2542 is user- programmable. The oscillator of SC2542 can be programmed with an external resistor from the Rosc pin to ground. The step-down controller is capable of operating up to 300KHz. The relationship between oscillation frequency versus oscillation resistor is shown in Figure 7.
The advantages of using constant frequency operation include simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFETs/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging, and cost also need to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

Power on Sequence

After applying the input voltage and with STBY and EN inputs high, Vcc and 5VSTBY will rise. When Vcc rises above the UVLO threshold both switcher outputs will also ramp up. By pulling the SS pins low, the two switcher outputs can be disabled, with Vcc and 5VSTBY maintaining regulation. Vcc will turn off when STBY is pulled low, with 5VSTBY maintaining regulation. And finally 5VSTBY will turn off when EN is pulled low, and the device will be in shutdown mode.

Mode	Logic input
Normal Mode: Both PWM rails in regulation 5V STBY rail in regulation V_{CC} rail in regulation	 Setting EN pin to logic high Setting STBY pin to logic high No pull down of SS
Standby Mode: 5V STBY rail in regulation	Setting EN pin to logic high Setting STBY pin to logic high
Shutdown Mode:	Setting EN pin to logic low

Soft Start

During start-up, the reference voltage of the error amplifier equals 30% of the voltage on Css (soft-start capacitor) which is connected between the SS pin and ground. When the controller is enabled (by pulling EN pin or STBY

Applications Information (Cont.)

pin high), an internal 84uA current source, Iss, (soft start current) will charge the soft-start capacitor gradually. The PWM output starts pulsing when the soft start voltage reaches 1V.

This soft start scheme will ensure the duty cycle increases slowly, therefore limiting the in rush current into the output capacitor and also ensuring the inductor does not saturate. The soft start capacitor will eventually be charged up to 2.5V.

The soft-start sequence is initiated when EN pin or STBY pin is high and Vcc > 5.5V or during recovery from a fault condition (OCP, OVP, or UVLO).

The period of start up can be programmed by the soft start capacitor:

$$T_{SS} = \frac{C_{SS} \times 2.5V}{84\ \mu A}$$

Shutdown

When the EN pin or STBY pin is pulled low, an internal 15uA current source discharges the soft-start capacitor and DRVH/DRVL signals stop pulsing. The output voltage ramps down at a rate determined by the load condition.

The SC2542 can also be shutdown by pulling down directly on the SS pin. The designer needs to consider the slope of the SS pin voltage and choose a suitable pull down resistor to prevent the output from undershooting.

Shutdown can also be triggered under an OCP condition. When an OCP condition is detected, DRVH and DRVL will stop pulsing and enter a “tri-state shutdown” with the output voltage ramping down at a rate determined by the load condition. The internal 15uA current source will begin discharging the soft-start capacitor and when the soft-start voltage reaches 0.65V, DRVL will go high.

Over Current Protection (OCP)

The inductor current is sensed by using the low side MOSFET Rds(on). After low side MOSFET is turned on, the OCP comparator starts monitoring the voltage drop across the MOSFET. The OCP trip level is programmed by a resistor from the ILIM pin to the phase node. There is an internal current source that flows out of the ILIM pin which will generate a voltage drop on the setting resistor. When the sum of the setting resistor voltage and the MOSFET drain to source voltage is less then zero, the OCP condition will be flagged. This functionality is depicted in Figure 8.

The following formula is used to set the OCP level:

$$10\mu A \times R_{ILIM} = I_{L\_PEAK} \times R_{DS(ON)}$$

When OCP is tripped, both high side and low side MOSFETs will be turned off and this condition is latched. At the same time, the soft start cap will be discharged by the internal current source of 15uA. When the Vss drops bellow 0.65V, the DRVL pin will go high again.

To avoid switching noise during the phase node commutation, a 100nS blanking time is built in after the low side MOSFET is turned on, as shown in Fig. 9.

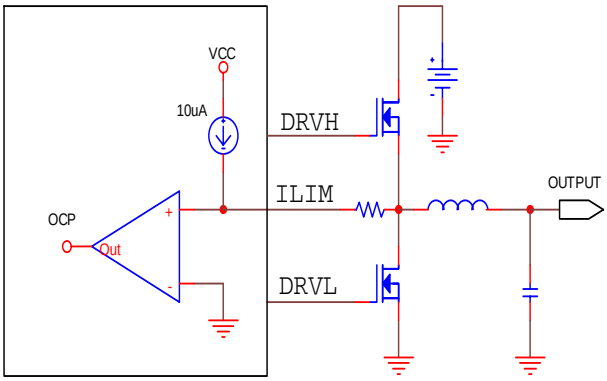


Figure 8. Block diagram of over current protection.

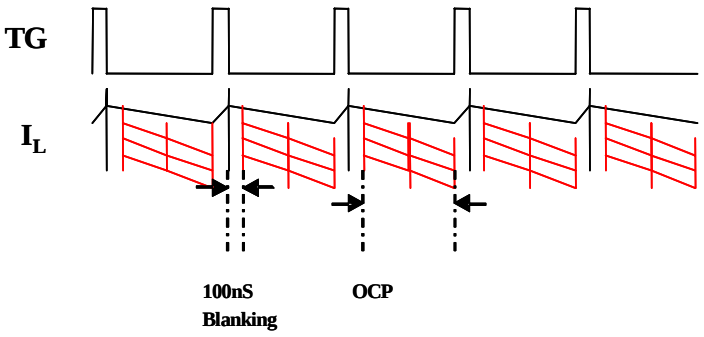


Figure 9. OCP comparator timing chart.

Under Voltage Lock Out (UVLO)

The UVLO circuitry monitors Vcc and the soft start begins once Vcc ramps up above 5.5V. There is a built in 400mV hysteresis voltage for the UVLO ramp down threshold. The gate driver output will be in "tri-state"(both high side and low side MOSFET off) once Vcc ramps down bellow 5.1V (typical), and the soft start cap will be discharged by internal 15uA current sink.

Over Voltage Protection (OVP)

The OVP circuitry monitors the feedback voltages, If either feedback voltage exceeds 0.89V, the OVP condition is registered. Under this condition, the DRVH pins will be pulled low, and the DRVL pins will be pulled high. This will create a "crow bar" condition for the input power rail in case the high side MOSFET is failed short. The crow bar operation may trip the input supply to prevent the load from seeing more voltage.

Minimum Pulse Width Setting

In skip mode operation, the top FET driver always sends out a pulse which is wider than the DCM pulse to keep the load in regulation. This forces the SC2542 to operate in skip mode and improves the light load efficiency. To set minimum pulse, one can use a simple formula:

$$Rmin(k\Omega) = \frac{Tpulse \bullet Vin}{150(pC)}$$

Setting Tpulse is 80% of normal pulse wide.

For example, with 24V input, 5V output and 200khz operating frequency. The normal pulse is 1.04 uS. To set Tpulse = 0.83uS, one can use:

$$Rmin = \frac{Tpulse \bullet Vin}{150(pC)} = \frac{0.83\mu S \text{ X } 24V}{150(pC)} = 133k\Omega$$

Power Good

The power good is an open collector output. The PWRGD pin is pulled low at start up if any of the two feedback voltages are below 90% of the regulation level. The ramp down threshold of the signal is 80% of the regulation target. External pull up is required for the PWRGD pin, and the pull up resistor should be chosen such that the pin does not sink more than 1mA when PWRGD is low.

Main Control Loop Design

The goal of compensation is to shape the frequency response of the buck converter to achieve a better DC accuracy and a faster transient response, while maintaining the loop stability.
The block diagram in Figure 10 represents the control loop of a buck converter designed with the SC2542. The control loop consists of a compensator, a PWM modulator, and an LC filter.

The LC filter and the PWM modulator represent the small signal model of the buck converter operating at fixed switching frequency. The transfer function of the model is given by:

$$\frac{V_O}{V_C} = \frac{V_{IN}}{V_m} \bullet \frac{1 + SR_{ESR}C}{1 + SL/R + S^2LC}$$

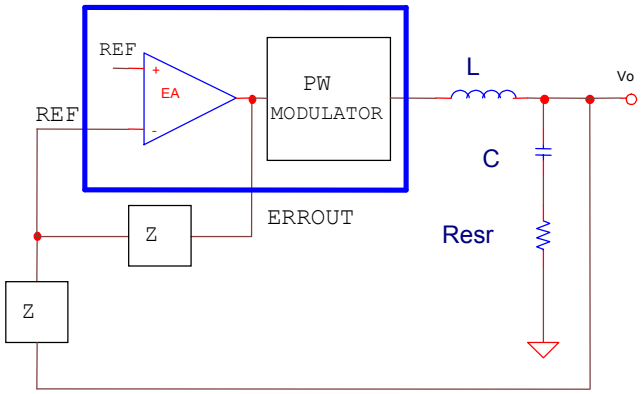


Figure 10. Block diagram of the control loop.

where V_{IN} is the input voltage, V_m is the amplitude of the internal ramp, and R is the equivalent load.

The model is a second order system with a finite DC gain, a complex pole pair at Fo, and an ESR zero at Fz, as shown in Figure 11. The locations of the poles and zero are determined by:

Applications Information (Cont.)

$$F_O = \frac{1}{2\pi\sqrt{LC_O}}$$

$$F_Z = \frac{1}{2\pi\, R_{ESR} C_O}$$

The compensator in Figure 10 includes an error amplifier and compensation networks Zf and Zs. It is implemented by the circuit in Figure 12. The compensator provides an integrator, double poles, and double zeros. As shown in Figure 11, the integrator is used to boost the gain at low frequency. Two zeros are introduced to compensate excessive phase lag at the loop gain crossover due to the integrator (-90deg) and the complex pole pair (-180deg). Two high frequency poles are designed to compensate the ESR zero and to attenuate high frequency noise.

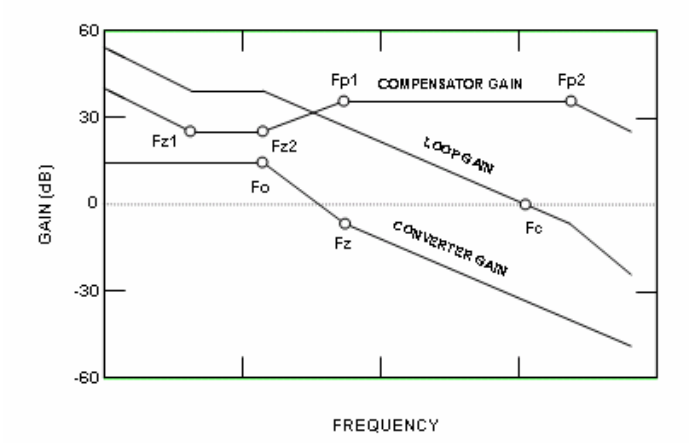


Figure 11. Bode plots for control loop design.

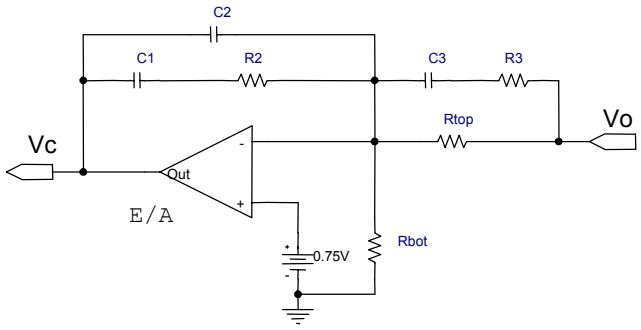


Figure 12. Compensation network.

A resistive divider is used to program the output voltage. The top resistor, Rtop, of the divider in Figure 12 can be chosen from 20kΩ to 30kΩ. Then the bottom resistor, Rbot, is found from:

$$R_{BOT} = \frac{0.75V}{V_O - 0.75V} * R_{TOP}$$

where 0.75V is the internal reference voltage of the SC2542.

The other components of the compensator can be calculated using following design procedure:

(1). Plot the converter gain, including LC filter and PWM modulator.
(2). Select the open loop crossover frequency Fc located at 10% to 20% of the switching frequency.
(3). Use the first compensator pole Fp1 to cancel the ESR zero.
(4). Have the second compensator pole Fp2 at half the switching frequency to attenuate the switching ripple and high frequency noise.
(5). Place the first compensator zero Fz1 at or below 50% of the power stage resonant frequency Fo.
(6). Place the second compensator zero Fz2 at or below the power stage resonant frequency Fo.

A MathCAD program is available upon request for the calculation of the compensation parameters.

Design Procedure for a Step-down Power Converter

Selection criteria and design procedures for the following parameters are described:

1) Output inductor (L) type and value
2) Output capacitor (Co) type and value
3) Input capacitor (Cin) type and value
4) Power MOSFETs
5) Current sensing and limiting circuit
6) Voltage sensing circuit
7) Loop compensation network

The following step-down converter specifications are needed:

Applications Information (Cont.)

Input voltage range: Vin,min and Vin,max
Input voltage ripple (peak-to-peak): DVin
Output voltage: Vo
Output voltage accuracy: e
Output voltage ripple (peak-to-peak): DVo
Nominal output (load) current: Io
Maximum output current limit: Io,max
Output (load) current transient slew rate: dIo/dt (A/s)
Circuit efficiency: η

Inductor (L) and Ripple Current

Both step-down controllers in the SC2542 operate in synchronous continuous-conduction mode (CCM) regardless except in light-load mode. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductance but it takes longer to change the inductor current during load transients. Conversely smaller inductance results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.
Assuming that the inductor current ripple (peak-to-peak) value is δ Io, the inductance value will then be:

$$L = \frac{V_O(1-D)}{\delta I_O F_S}$$

The peak current in the inductor becomes:

$$(1+\delta/2)*I_O$$

and RMS current is:

$$I_{L,rms} = I_O\sqrt{1+\frac{\delta^2}{12}}$$

The followings are to be considered when choosing inductors.
a) Inductor core material: For higher efficiency applications above 300 KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 300 KHz but with attendant higher core losses.
b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.
c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (Co) and Vout Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR and ESL as shown in Figure 13.

Figure 13. An equivalent circuit of output.

If the current through the branch is ib(t), the voltages across the terminals will then be:

$$V_O(t) = V_O + \frac{1}{Co}\int_0^t i_b(t)dt + Lesl\frac{di_b(t)}{dt} + \mathrm{Re}\,sri_b(t).$$

This basic equation illustrates the effects of ESR, ESL, and Co on the output voltage.

The first term is the DC voltage across Co at time t = 0. The second term is the voltage variation caused by the charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a vector sum of the last three terms. Since the inductor current is a triangular waveform with peak-to-peak value ä*Io, the ripple-voltage caused by inductor current ripples is:

$$\Delta V_C \approx \frac{\delta I_O}{8C_O f_s},$$

the ripple-voltage due to ESL is:

$$\Delta V_{ESL} = L_{esl} f_s \frac{\delta I_O}{D},$$

and the ESR ripple-voltage is:

$$\Delta V_{ESR} = R_{esr}\ \delta I_O$$

Applications Information (Cont.)

Aluminum capacitors (e.g. electrolytic) have high capacitances and low ESL. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR. Other types to choose are solid OS-CON, POSCAP, and tantalum.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To meet the steady state output ripple-voltage spec, the ESR should satisfy:

$$R_{ESR1} < \frac{\Delta V_O}{\delta I_O}$$

To limit the dynamic output voltage overshoot/undershoot within a (say 3%) of the steady state output voltage from no load to full load, the ESR value should satisfy:

$$R_{ESR2} < \frac{3\%V_O}{I_O}$$

Then, the required ESR value of the output capacitors should be:

Resr = min{Resr1,Resr2 }.

The voltage rating of aluminum capacitors should be at least 1.5Vo. The RMS current ripple rating should also be greater than: $\frac{\delta I_O}{2\sqrt{3}}$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple caused by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy:

$$C_O > \frac{10}{2\pi f_s R_{ESR}}$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant. For example, if a 10uF, 4mÙ ceramic capacitor is connected in parallel with 2x1500uF, 90mÙ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100uF, 2mÙ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100uF, 2mÙ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR either. Instead they should be calculated using the following formula.

$$C_{EQ(\omega)} = \frac{(R_{1A}+R_{1B})^2\omega^2 C_{1A}{}^2 C_{1B}{}^2 + (C_{1A}+C_{1B})^2}{(R_{1A}{}^2 C_{1A} + R_{1B}{}^2 C_{1B})\omega^2 C_{1A} C_{1B} + (C_{1A}+C_{1B})}$$

$$C_{EQ(\omega)} = \frac{R_{1A}R_{1B}(R_{1A}+R_{1B})\omega^2 C_{1A}{}^2 C_{1B}{}^2 + (R_{1B}C_{1B}{}^2 + R_{1A}C_{1A}{}^2)}{(R_{1A}+R_{1B})^2\omega^2 C_{1A}{}^2 C_{1B}{}^2 + (C_{1A}+C_{1B})^2}$$

where R1a and C1a are the ESR and capacitance of electrolytic capacitors, and R1b and C1b are the ESR and capacitance of the ceramic capacitors, respectively (Figure 13)

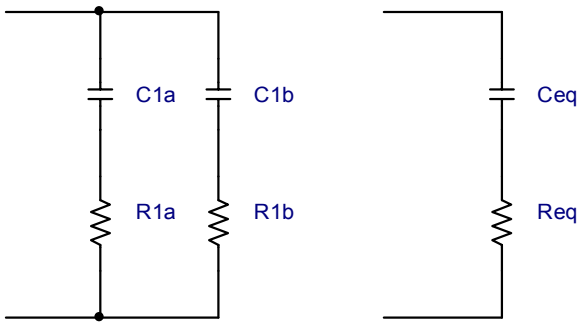


Figure 14. Equivalent RC branch.

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If R1a = R1b = R1 and C1a = C1b = C1, then Req and Ceq will be frequency-independent and

$$Req = 1/2\ R1 \text{ and } Ceq = 2C1.$$

Input Capacitor (Cin)

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 14.

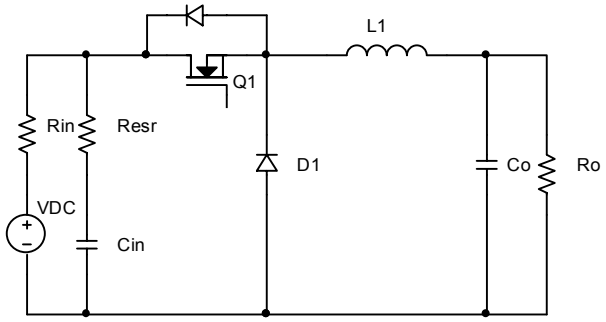


Figure 14. A simple model for the converter input.

In Figure 14 the DC input voltage source has an internal impedance Rin and the input capacitor Cin has an ESR of Resr. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 15.

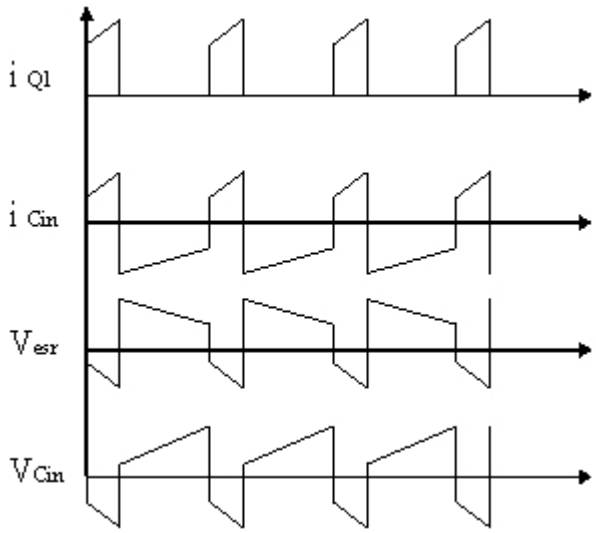


Figure 15. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFETs on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately:

$$I_{Cin} = I_O \sqrt{D\left[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + (1-D)\right]}$$

The power dissipated in the input capacitors is then:

$$P_{Cin} = I_{Cin}^{\ 2}\ R_{esr}$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. It is common practice that multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to

Applications Information (Cont.)

the ESR is:

$$\Delta V_{ESR} = R_{ESR}(1+\frac{\delta}{2})I_O$$

The peak-to-peak input voltage ripple due to the capacitor is:

$$\Delta V_C \approx \frac{DI_O}{C_{IN} f_S}$$

From these two expressions, CIN can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2542 operate at 180 degrees from each other. If both step-down channels in the SC2542 are connected to the same input rail, the input RMS currents will be reduced. Ripple cancellation effect of interleaving allows the use of smaller input capacitors.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the RMS value of the ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be D1, D2 and Io1, Io2, respectively.

If D1<0.5 and D2<0.5, then:

$$I_{CIN} \approx \sqrt{D_1 I_{O1}^2 + D_2 I_{O2}^2}$$

If D1>0.5 and (D1-0.5) < D2<0.5, then:

$$I_{CIN} \approx \sqrt{0.5 I_{O1} + (D_1 - 0.5)(I_{O1} + I_{O2})^2 + (D_2 - D_1 + 0.5) I_{O2}^2}$$

If D1>0.5 and D2 < (D1-0.5) < 0.5, then:

$$I_{CIN} \approx \sqrt{(D1 + D2 - 1)(I_{O1} + I_{O2})^2 + (1 - D_2) I_{O1}^2 + (1 - D_1) I_{O2}^2}$$

Choosing Power MOSFETs

Main considerations in selecting the MOSFETs are power dissipation, MOSFETs cost, and packaging. Switching losses and conduction losses of the MOSFET are directly related to the total gate charge (Cg) and channel on-resistance (Rds(on)). In order to judge the performance of MOSFET, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 16

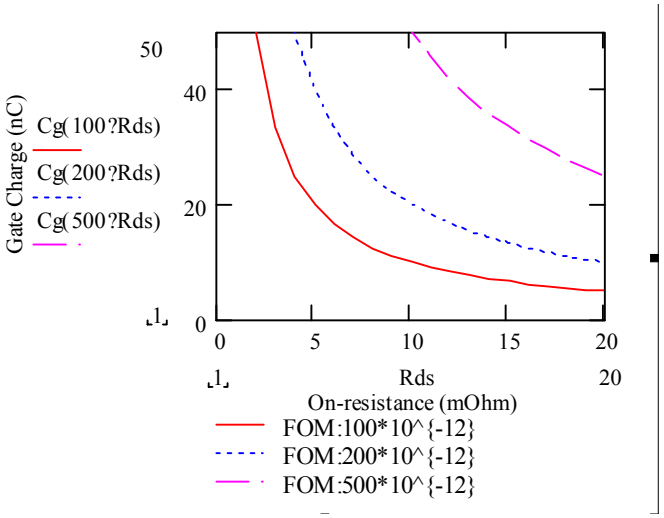


Figure 16. Figure of Merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFET with both low Cg and low Rds(on). Usually a trade-off between Rds(on)and Cg has to be made.
MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET with low Cg are used for the top switch and MOSFET with low Rds(on) are used for the bottom switch.

MOSFET power dissipation consists of:
a) conduction loss due to the channel resistance Rds(on);
b) switching loss due to the switch rise time tr and fall time tf; and
c) the gate loss due to the gate resistance RG.

Applications Information (Cont.)

Top Switch

The RMS value of the top switch current is calculated as:

$$I_{Q1,rms} = I_O \sqrt{D(1+\frac{\delta^2}{12})}$$

The conduction losses are then:

$$P_{TC} = I_{Q1,rms}{}^2 R_{DS(ON)}$$

Rds(on) varies with temperature and gate-source voltage. Curves showing Rds(on) variations can be found in manufacturers' data sheet. From the Si4860 datasheet, Rds (on) is less than 8mΩ when Vgs is greater than 10V. However Rds(on) increases by 50% as the junction temperature increases from 25°C to 110°C.

The switching losses can be estimated using the simple formula:

$$P_{TS} = \frac{1}{2}(t_r + t_f)(1+\frac{\delta}{2})I_O V_{IN} f_S$$

where tr is the rise time and tf is the fall time of the switching process. Different manufactures have different definitions and test conditions for tr and tf. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 17

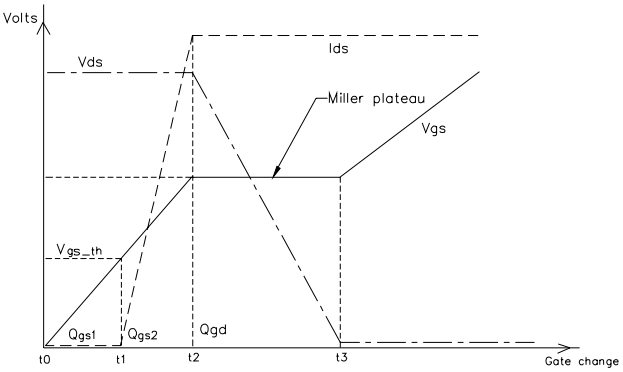


Figure 17. MOSFET switching characteristics

In Figure 17, Qgs1 is the gate charge needed to bring the gate-to-source voltage Vgs to the threshold voltage Vgs_th. Qgs2 is the additional gate charge required for the switch current to reach its full-scale value Ids,.and Qgd is the charge needed to charge gate-to-drain (Miller) capacitance when Vds is falling.

Switching losses occur during the time interval [t1, t3]. Defining tr = t3-t1 and tr can be approximated as:

$$T_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}$$

where Rgt is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance Rgi, external resistance Rge and the gate resistance Rg within the MOSFET:

$$R_{GT} = R_{GI} + R_{GE} + R_G$$

Vgsp is the Miller plateau voltage shown in Figure17.

Similarly an approximate expression for tf is:

$$T_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}$$

Only a portion of the total losses Pg = QgVccfs is dissipated in the MOSFET package. Here Qg is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is:

$$P_{TG} = \frac{R_G}{R_{GT}} Q_G V_{CC} f_S$$

The total bottom switch losses are then:

$$P_T = P_{TC} + P_{TS} + P_{TG}$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction losses are inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Bottom Switch

The RMS current in bottom switch is given by:

$$I_{Q2,rms} = I_O \sqrt{(1-D)(1+\frac{\delta^2}{12})}$$

The conduction losses are then:

Applications Information (Cont.)

$$P_{bc} = I_{Q2,RMS}{}^{2} R_{DS(ON)}$$

where Rds(on) is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g. Vin = 12V, Vo = 1.5V), the duty ratio D will be small. Since the bottom switch conducts with duty ratio (1-D), the corresponding conduction losses can be quite high. Due to non-overlapping conduction between the top and the bottom MOSFET, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss is negligible due to near zero-voltage switching.

The gate losses are estimated as:

$$P_{BG} = \frac{R_G}{R_{GT}} Q_G V_{CC} f_S$$

The total bottom switch losses are then:

$$P_B = P_{BC} + P_{BG}$$

Once the power losses for the top and bottom MOSFET are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature (Tj,max, usually 125°C) is not exceeded under the worst-case condition. The equivalent thermal impedance from junction to ambient (θ_{JA}) should satisfy:

$$\theta_{JA} \le \frac{T_{J,MAX} - T_{A,MAX}}{P_{LOSS}}$$

θ_{JA} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area, and the air flow condition (natural or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

Power Stage

1) Separate the power ground from the signal ground. In SC2542 design, use an isolated local ground plane for the controller and tie it to power grand.

2) Minimize the size of the high pulse current loop. Keep the top MOSFET, the bottom MOSFET and the input capacitors within a small area with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFETs to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node if the EMI is a concern for the system.

4) Shorten the gate drive trace. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFET. These inductances may also ring with the gate capacitance.

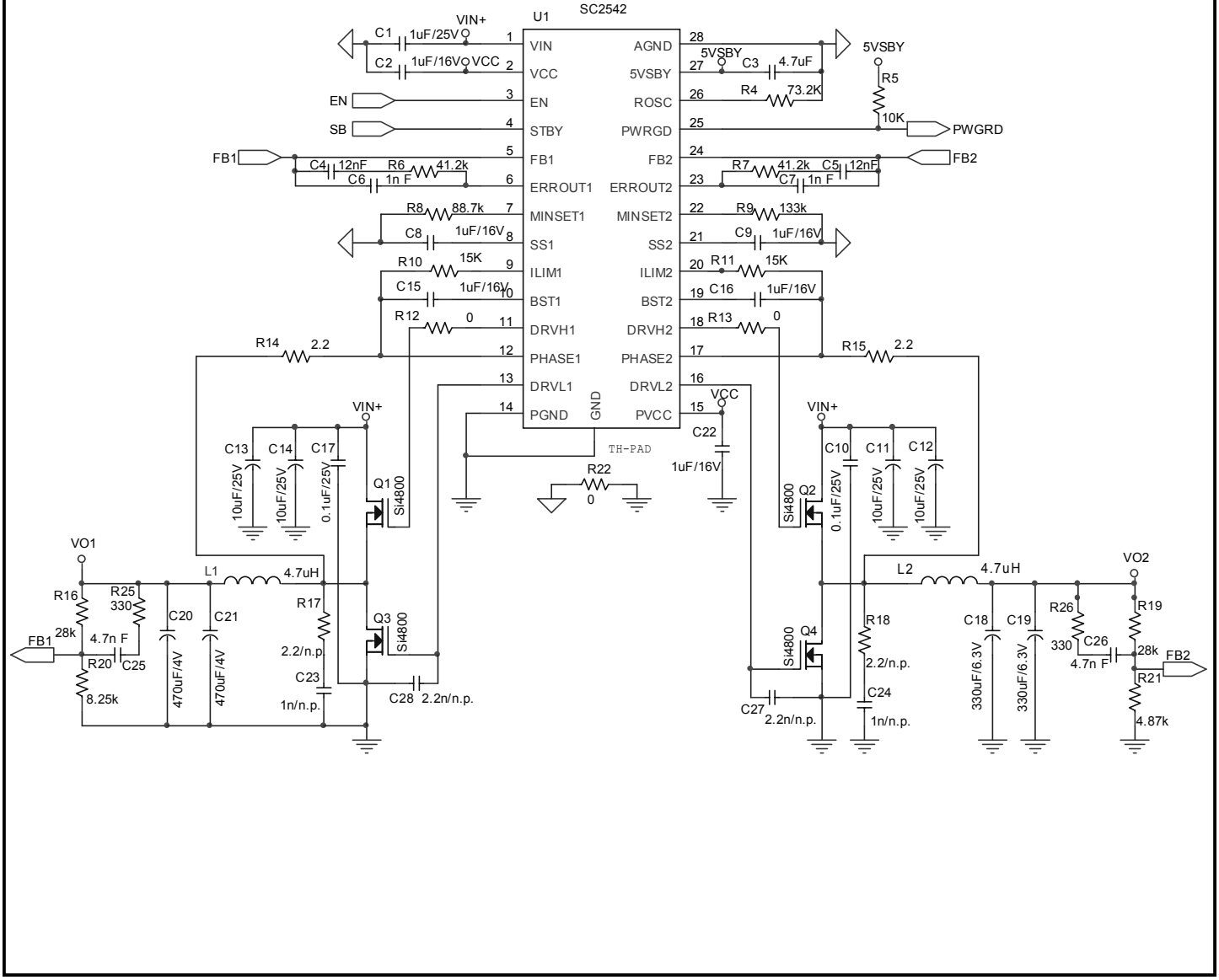
5) Put the decoupling capacitor for the gate drive power supplies (BST and PVCC) close to the IC and power ground.

Control Section

6) The frequency-setting resistor Rosc should be placed close to Pin 23. Trace length from this resistor to the analog ground should be minimized.

7) Place the bias decoupling capacitor right across the VCC and analog ground AGND.

Typical Applications Schematic

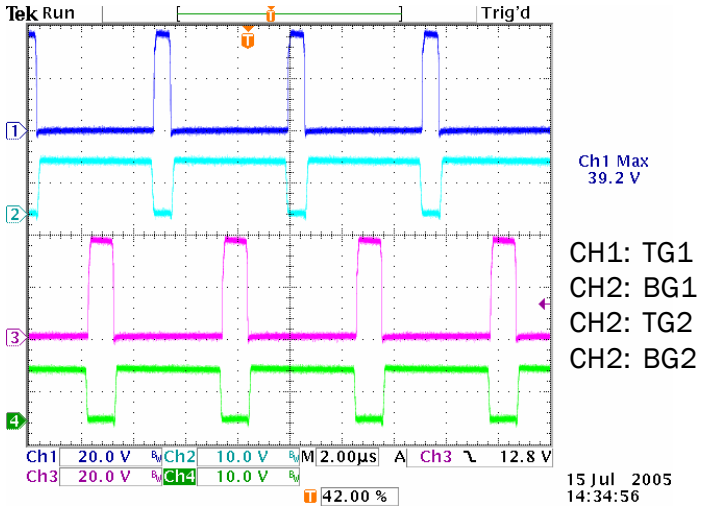


Typical Applications Schematic - BOM

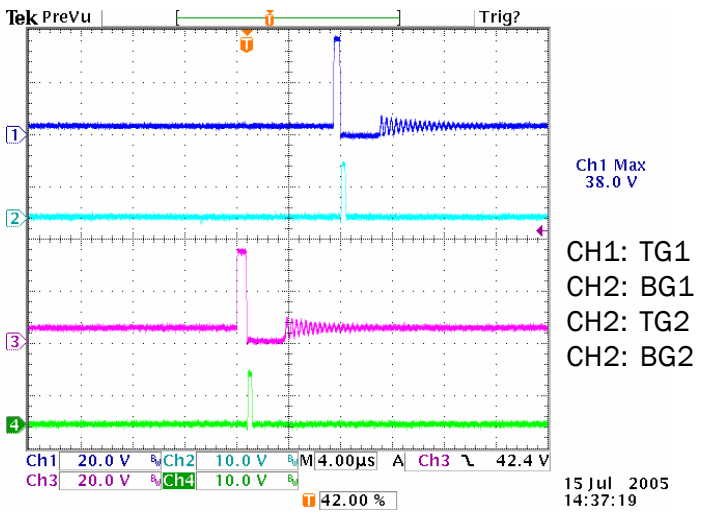
Ref	Qty	Reference	Part Number/Value	Manufacturer
1	1	C1	1uF, 25V, X5R, Ceramic, 0805	Any
2	6	C2,C8,C9,C15,C16,C22	1uF, 16V, X5R, Ceramic , 0805	Any
3	1	C3	4.7uF, 16V, X5R, Ceramic 1206	Any
4	2	C4,C5	12nF, Ceramic, 0603	Any
5	2	C6, C7	1nF, Ceramic 0603	Any
6	2	C10, C17	0.1nF, Ceramic 0603	Any
7	4	C11,C12, C13,C14	10uF, 25V, X5R, Ceramic, 1210	Panasonic, ECJ4YB1E106M
8	2	C18,C19	330uF, 6.3V, 18mohm, PosCap	Sanyo, 6TPE330MIL
9	2	C20,C21	470uF, 4V, 15mohm, PosCap	Sanyo, 4TPE470MFL
10	4	C23, C24, C27, C28	N.P.	
11	2	C25,C26	4.7nF, Ceramic, 0603	Any
12	2	L1, L2	4.7uH, 6.8A, 15mohm	Sumida, CDRH127
13	4	Q1, Q2, A3, Q4	Si4800	Vishay
14	1	R4	73.2K, 0603	Any
15	1	R5	10K, 0603	Any
16	2	R6, R7	41.2K, 0603	Any
17	1	R8	88.7K, 0603	Any
18	1	R9	133K, 0603	Any
19	2	R10,R11	15K, 0603	Any
20	3	R12, R13,R22	0	Any
21	2	R14, R15	2.2, 0603	Any
22	2	R16,R19	28K, 0603	Any
23	2	R17, R18	N.P.	
24	1	R20	8.25K, 0603	Any
25	1	R21	4.87K, 0603	Any
26	2	R25,R26	330, 0603	Any
27	1	U1	SC2542	Semtech

Typical Characteristics

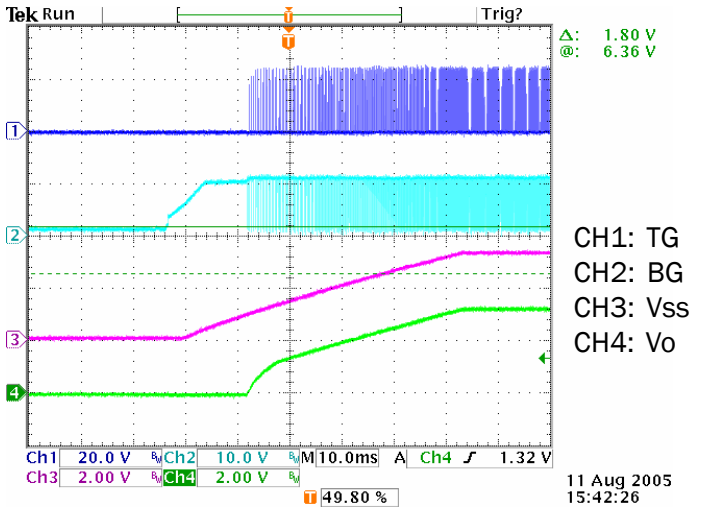
Gate waveform (SPWM Mode)



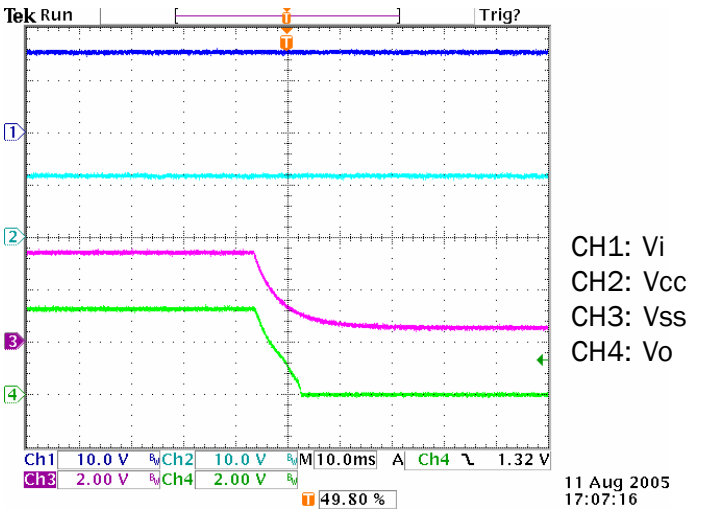
Gate waveform (SKIP Mode)



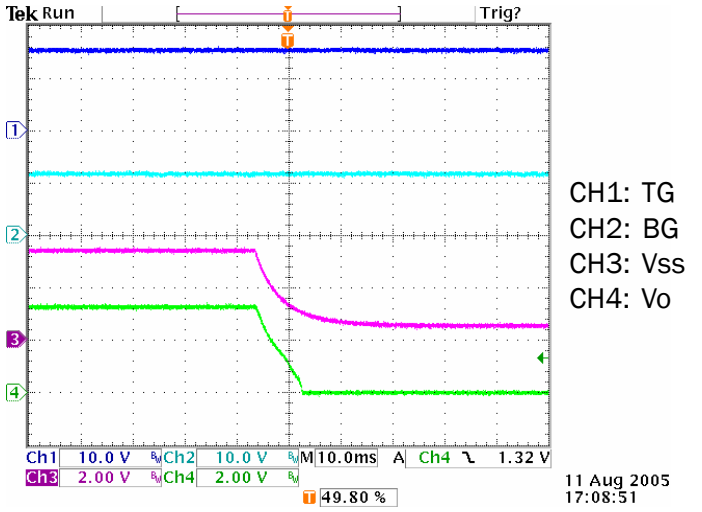
Start up



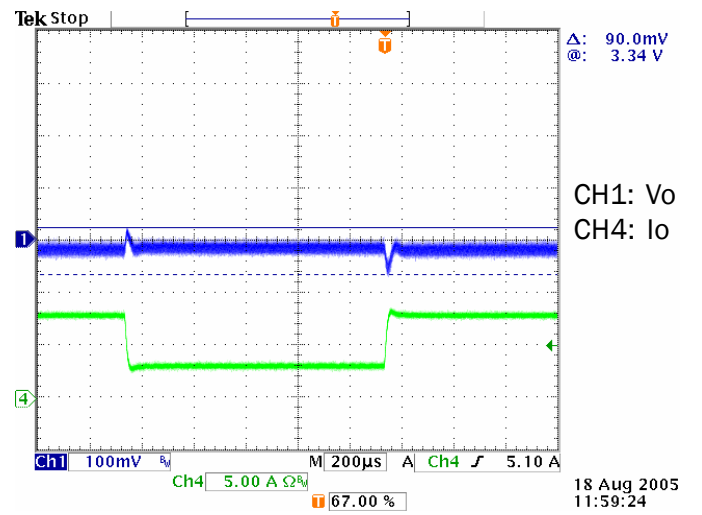
Shutdown by pulling down SS pin voltage



Shutdown by pulling down EN/STBY pin voltage

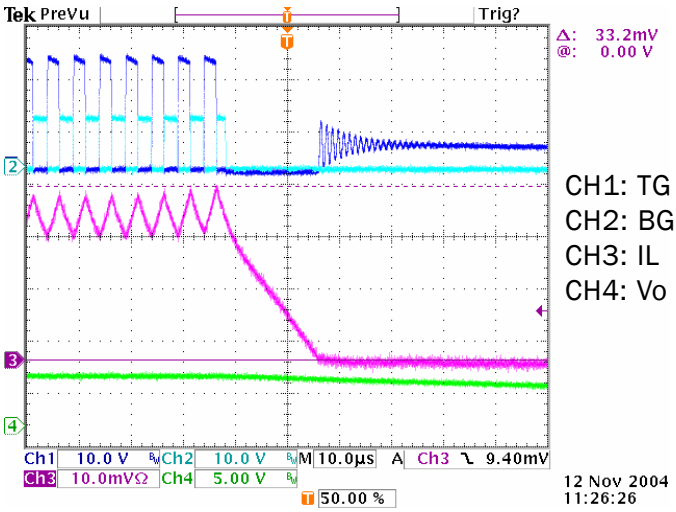


Transient response (3 ~ 8A

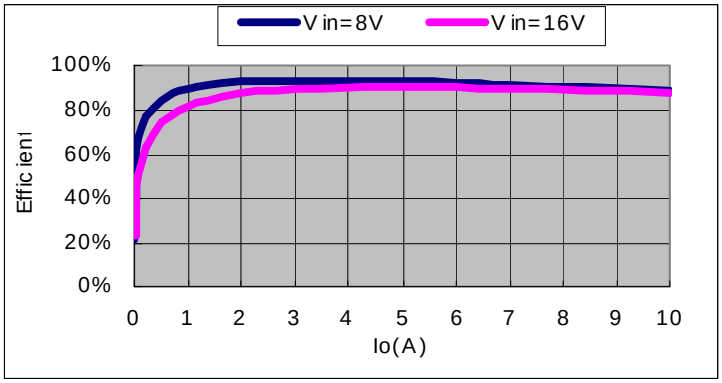


Typical Characteristics (Cont.)

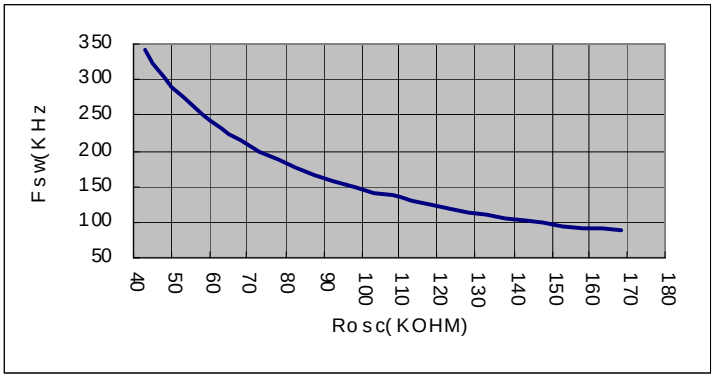
Over current protection (5A/10mV)



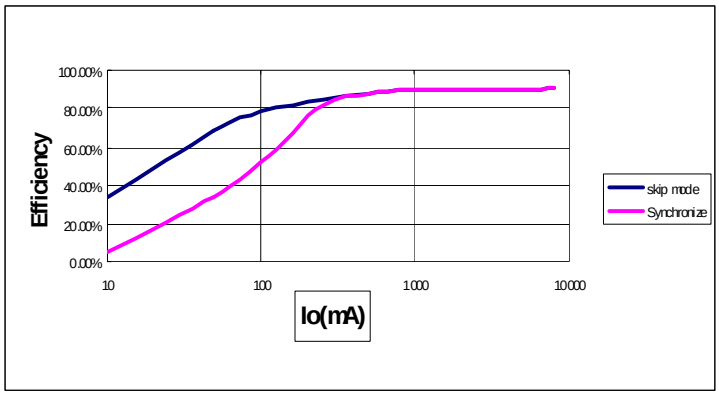
Efficiency curve for Vout = 3.3V



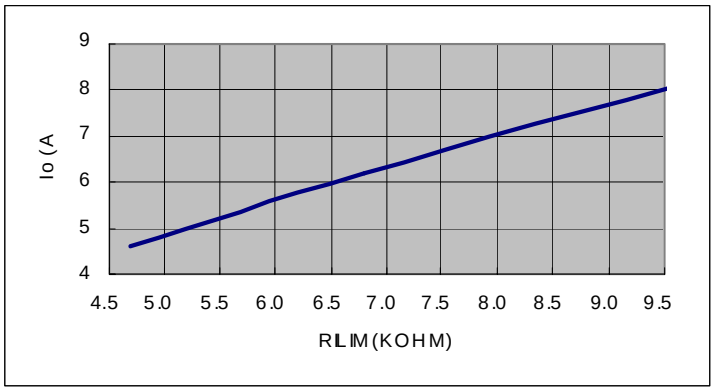
Operating frequency vs. Rosc



Efficiency curve for SPWM Mode vs. SKIP Mode

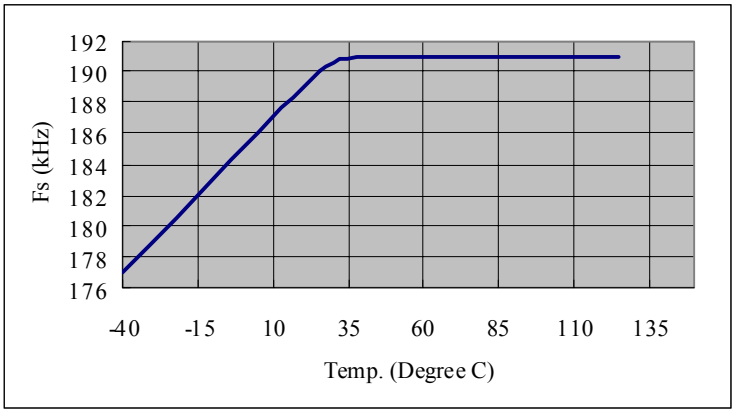


RILIM vs. OCP (Vin = 12V)

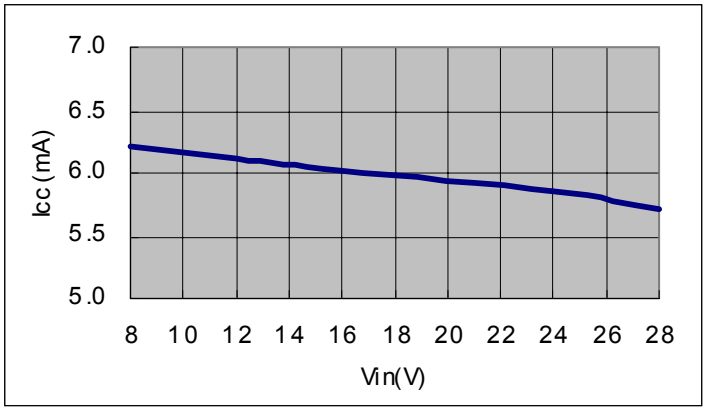


Typical Characteristics (Cont.)

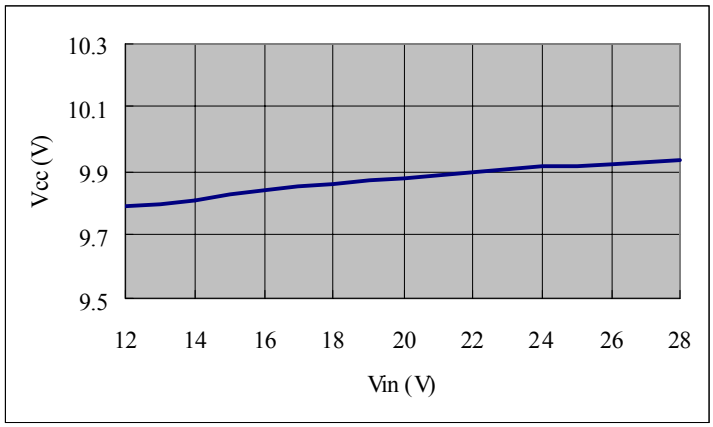
Frequency vs. Temp. (Rosc = 75kohm, Vin = 16V)



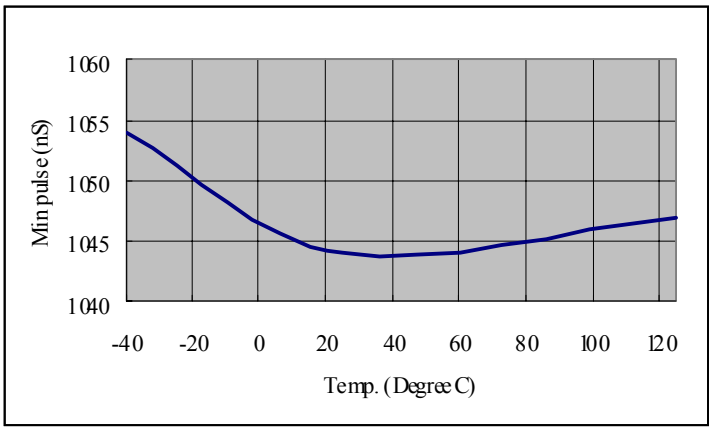
Icc vs. Vin (Ta = 25 Degree C)



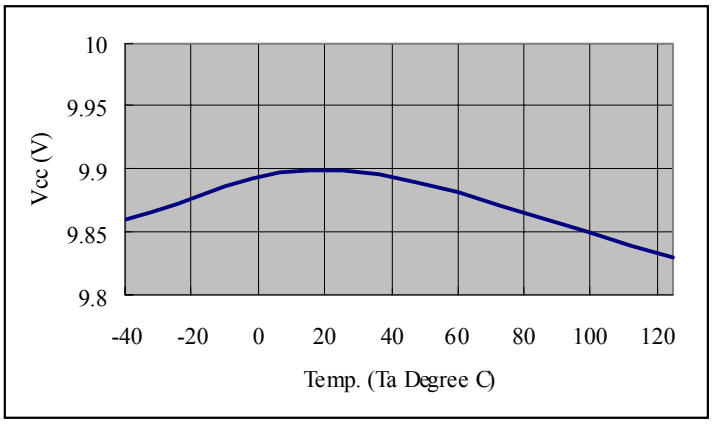
Vcc vs. Vin (Ta = 25 Degree C)



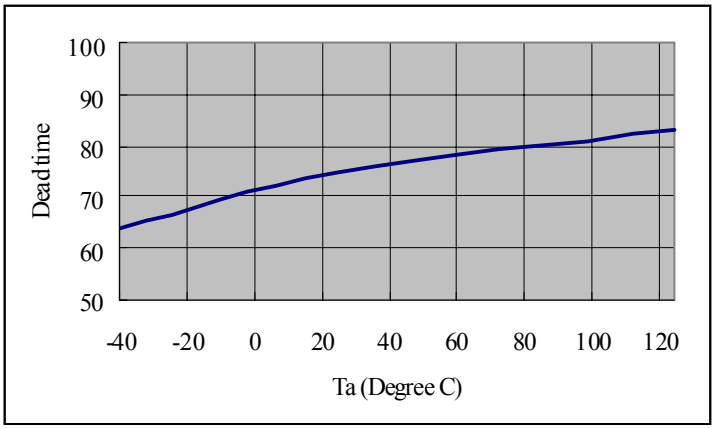
Minimum pulse width vs. Temp (Ta)



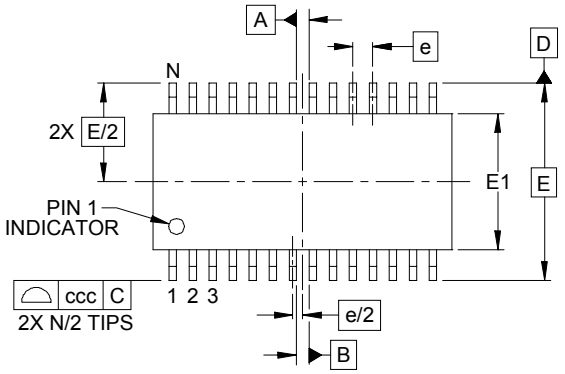
Vcc vs. Temp. (Ta = 25 Degree C)

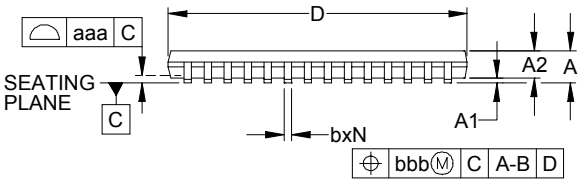


Dead time vs. Ta (Vin = 16V, DH falling to DL rising)

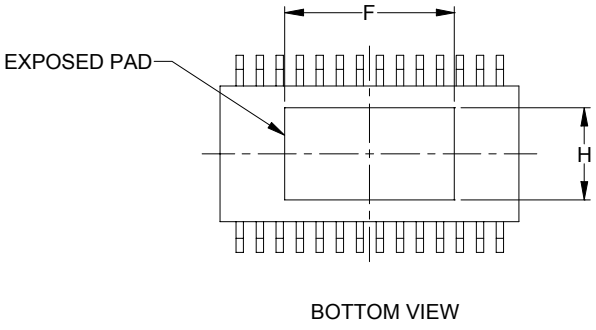


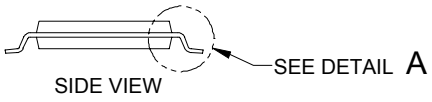
Outline Drawing - TSSOP-28-EDP

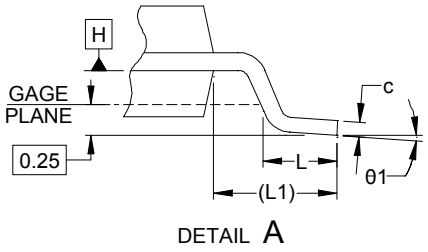




DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.000	-	.006	0.00	-	0.15
A2	.031	-	.041	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.008	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
F	.210	.216	.220	5.35	5.50	5.60
H	.112	.118	.122	2.85	3.00	3.10
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	28			28		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



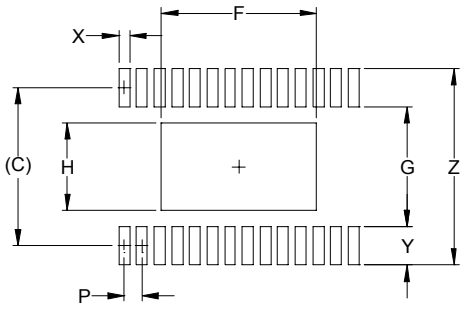




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AET.

Land Pattern - TSSOP-28-EDP



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.224	5.70
G	.161	4.10
H	.126	3.20
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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