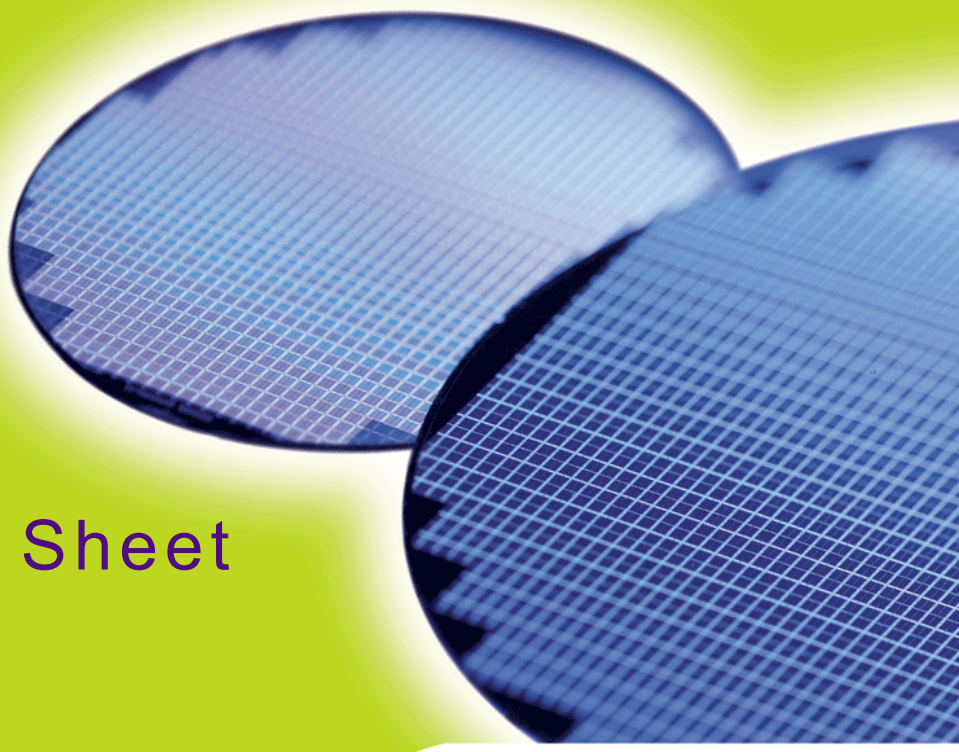
March 2007

HYS72T32000HR–[2.5/3/3S/3.7/5]–A
HYS72T64001HR–[2.5/3/3S/3.7/5]–A
HYS72T64020HR–[2.5/3/3S/3.7/5]–A

240-Pin Registered DDR2 SDRAM Modules
DDR2 SDRAM
RDIMM SDRAM
RoHS Compliant



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HYS72T32000HR–[2.5/3/3S/3.7/5]–A, HYS72T64001HR–[2.5/3/3S/3.7/5]–A, HYS72T64020HR–[2.5/3/3S/3.7/5]–A **Revision History: 2007-03, Rev. 1.21**	
Page	**Subjects (major changes since last revision)**
All	Qimonda update
All	Adapted internet edition
Previous Revision: 2005-09, Rev. 1.2	
Chapter 4	SPD Codes update: Byte 49 Bit 0 = 1 (HighT_SRFEntry) for all product types
Chapter 5	Package Outlines updated
Previous Revision: 2005-06, Rev. 1.1	

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1 Overview

This chapter gives an overview of the 240-pin Registered DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 240-pin PC2-6400, PC2-5300, PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for PC, Workstation and Server main memory applications
- One rank 32M x 72, 64M x 72 and two ranks 64M × 72 module organization and 32M × 8, 64M × 4 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- All Speed Grades faster than DDR2–400 comply with DDR2–400 timing specifications
- Built with 256-Mbit DDR2 SDRAMs in P-TFBGA-60 chipsize packages.
- Programmable CAS Latencies (3, 4, 5 & 6), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- RDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on Standard reference layouts Raw Card “A-F”, “B-G” & “C-H”
- RoHS compliant products[1)]

TABLE 1
Performance for –2.5 & –3 (S)

Product Type Speed Code			–2.5	–3	–3S	Unit
Speed Grade			PC2–6400 6–6–6	PC2–5300 4–4–4	PC2–5300 5–5–5	—
max. Clock Frequency	@CL6	f_{CK6}	400	333	333	
	@CL5	f_{CK5}	333	333	333	MHz
	@CL4	f_{CK4}	266	333	266	MHz
	@CL3	f_{CK3}	200	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	12	15	ns
min. Row Precharge Time		t_{RP}	15	12	15	ns
min. Row Active Time		t_{RAS}	45	45	45	ns
min. Row Cycle Time		t_{RC}	60	57	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 2
Performance for DDR2-533 and DDR2-400

Product Type Speed Code			–3.7	–5	Units
Speed Grade			**PC2–4200 4–4–4**	**PC2–3200 3–3–3**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	15	ns
Min. Row Precharge Time		t_{RP}	15	15	ns
Min. Row Active Time		t_{RAS}	45	40	ns
Min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The QIMONDA HYS72T[32/64]0xxHR–[2.5/3/3S/3.7/5]–A module family are Registered DIMM modules “RDIMMs” with 30 mm height based on DDR2 technology. DIMMs are available as ECC modules in 32M x 72 (256 MByte) and 64M x 72 (512 MByte) organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 256-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write-protected; the second 128 bytes are available to the customer.

green Product

TABLE 3
Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-6400			
HYS72T32000HR–2.5–A	256 MB 1R×8 PC2–6400R–666–12–F0	1 Rank, ECC	256 Mbit (×8)
HYS72T64001HR–2.5–A	512 MB 1R×4 PC2–6400R–666–12–H0	1 Rank, ECC	256 Mbit (×4)
HYS72T64020HR–2.5–A	512 MB 2R×8 PC2–6400R–666–12–G0	2 Rank, ECC	256 Mbit (×8)
PC2-5300			
HYS72T32000HR–3–A	256 MB 1R×8 PC2–5300R–444–12–F0	1 Rank, ECC	256 Mbit (×8)
HYS72T64001HR–3–A	512 MB 1R×4 PC2–5300R–444–12–H0	1 Rank, ECC	256 Mbit (×4)
HYS72T64020HR–3–A	512 MB 2R×8 PC2–5300R–444–12–G0	2 Rank, ECC	256 Mbit (×8)
HYS72T32000HR–3S–A	256 MB 1R×8 PC2–5300R–555–12–F0	1 Rank, ECC	256 Mbit (×8)
HYS72T64001HR–3S–A	512 MB 1R×4 PC2–5300R–555–12–H0	1 Rank, ECC	256 Mbit (×4)
HYS72T64020HR–3S–A	512 MB 2R×8 PC2–5300R–555–12–G0	2 Rank, ECC	256 Mbit (×8)
PC2–4200			
HYS72T32000HR–3.7–A	256 MB 1R×8 PC2–4200R–444–11–F0	1 rank, ECC	256 Mbit (×8)
HYS72T64001HR–3.7–A	512 MB 1R×4 PC2–4200R–444–11–H0	1 rank, ECC	256 Mbit (×4)
HYS72T64020HR–3.7–A	512 MB 2R×8 PC2–4200R–444–11–G0	2 rank, ECC	256 Mbit (×8)
PC2-3200			
HYS72T32000HR–5–A	256 MB 1R×8 PC2–3200R–333–11–F0	1 Rank, ECC	256 Mbit (×8)
HYS72T64001HR–5–A	512 MB 1R×4 PC2–3200R–333–11–H0	1 Rank, ECC	256 Mbit (×4)
HYS72T64020HR–5–A	512 MB 2R×8 PC2–3200R–333–11–G0	2 Rank, ECC	256 Mbit (×8)

1) All part numbers end with a place code, designating the silicon die revision. Example: HYS72T32000HR–5–A, indicating Rev. “A” dies are used for DDR2 SDRAM components. For all QIMONDA DDR2 module and component nomenclature see **Chapter 6** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200R–444–11–F0”, where 4200R means Registered DIMM modules with 4.26 GB/sec Module Bandwidth and “444-11” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card “F”

TABLE 4
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
256 MB	32M ×72	1	ECC	9	13/2/10	A-F
512 MB	64M ×72	1	ECC	18	13/2/11	C-H
512 MB	64M ×72	2	ECC	18	13/2/10	B-G

TABLE 5
Components on Modules

Product Type[1)]	DRAM Components[1)]	DRAM Density	DRAM Organization	Note[2)]
HYS72T32000HR	HYB18T256800AF	256 Mbit	32M × 8	—
HYS72T64001HR	HYB18T256400AF	256 Mbit	64M × 4	—
HYS72T64020HR	HYB18T256800AF	256 Mbit	32M × 8	—

1) Green Product
2) For a detailed description of all available functions of the DRAM components on these modules see the component data sheet.

2 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in **Table 6** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 7** and **Table 8** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 6
Pin Configuration of RDIMM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signal CK0, Complementary Clock Signal CK0**
186	$\overline{\text{CK0}}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enables 1:0**
171	CKE1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
Control Signals				
193	$\overline{\text{S0}}$	I	SSTL	**Chip Select Rank 1:0**
76	$\overline{\text{S1}}$	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
192	$\overline{\text{RAS}}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
74	$\overline{\text{CAS}}$	I	SSTL	
73	$\overline{\text{WE}}$	I	SSTL	
18	$\overline{\text{RESET}}$	I	CMOS	**Register Reset**
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0**
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	**Not Connected** Less than 1Gb DDR2 SDRAMS

Ball No.	Name	Pin Type	Buffer Type	Function
188	A0	I	SSTL	**Address Bus 12:0, Address Signal 10/AutoPrecharge**
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13**
	NC	NC	—	**Not Connected** *Note: Non CA parity modules based on 256 Mbit component*
174	A14	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module. Less than 1 GBit per DRAM die.*
173	A15	I	SSTL	**Address Signal 14** *Note: CA Parity module*
	NC	NC	—	**Not Connected** *Note: Non CA parity module. Less than 1 GBit per DRAM die.*

Ball No.	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
206	DQ39	I/O	SSTL	**Data Bus 63:0**
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bits				
42	CB0	I/O	SSTL	**Check Bits 7:0** Check Bit Input / Output pins *Note: NC on Non-ECC module*
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobes 17:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
125	DQS9	I/O	SSTL	
126	$\overline{\text{DQS9}}$	I/O	SSTL	
134	DQS10	I/O	SSTL	
135	$\overline{\text{DQS10}}$	I/O	SSTL	
146	DQS11	I/O	SSTL	
147	$\overline{\text{DQS11}}$	I/O	SSTL	
155	DQS12	I/O	SSTL	
156	$\overline{\text{DQS12}}$	I/O	SSTL	
202	DQS13	I/O	SSTL	
203	$\overline{\text{DQS13}}$	I/O	SSTL	
211	DQS14	I/O	SSTL	
212	$\overline{\text{DQS14}}$	I/O	SSTL	
223	DQS15	I/O	SSTL	
224	$\overline{\text{DQS15}}$	I/O	SSTL	
232	DQS16	I/O	SSTL	
233	$\overline{\text{DQS16}}$	I/O	SSTL	
164	DQS17	I/O	SSTL	
165	$\overline{\text{DQS17}}$	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
Data Mask				
125	DM0	I	SSTL	**Data Masks 8:0** *Note: x8 based module*
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock**
119	SDA	I/O	OD	**Serial Bus Data**
239	SA0	I	CMOS	**Serial Address Select Bus 2:0**
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Parity				
55	$\overline{\text{ERR\_OUT}}$	O	CMOS	**Parity bits**
	PAR_IN	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197	V_{DD}	PWR	—	**Power Supply**
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	—	**Ground Plane**

Ball No.	Name	Pin Type	Buffer Type	Function
Other Pins				
19, 55, 68, 102, 137, 138, 173, 220, 221	NC	NC	—	**Not connected**
195	ODT0	I	SSTL	**On-Die Termination Control 1:0**
77	ODT1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	*Note: 1-Rank modules*

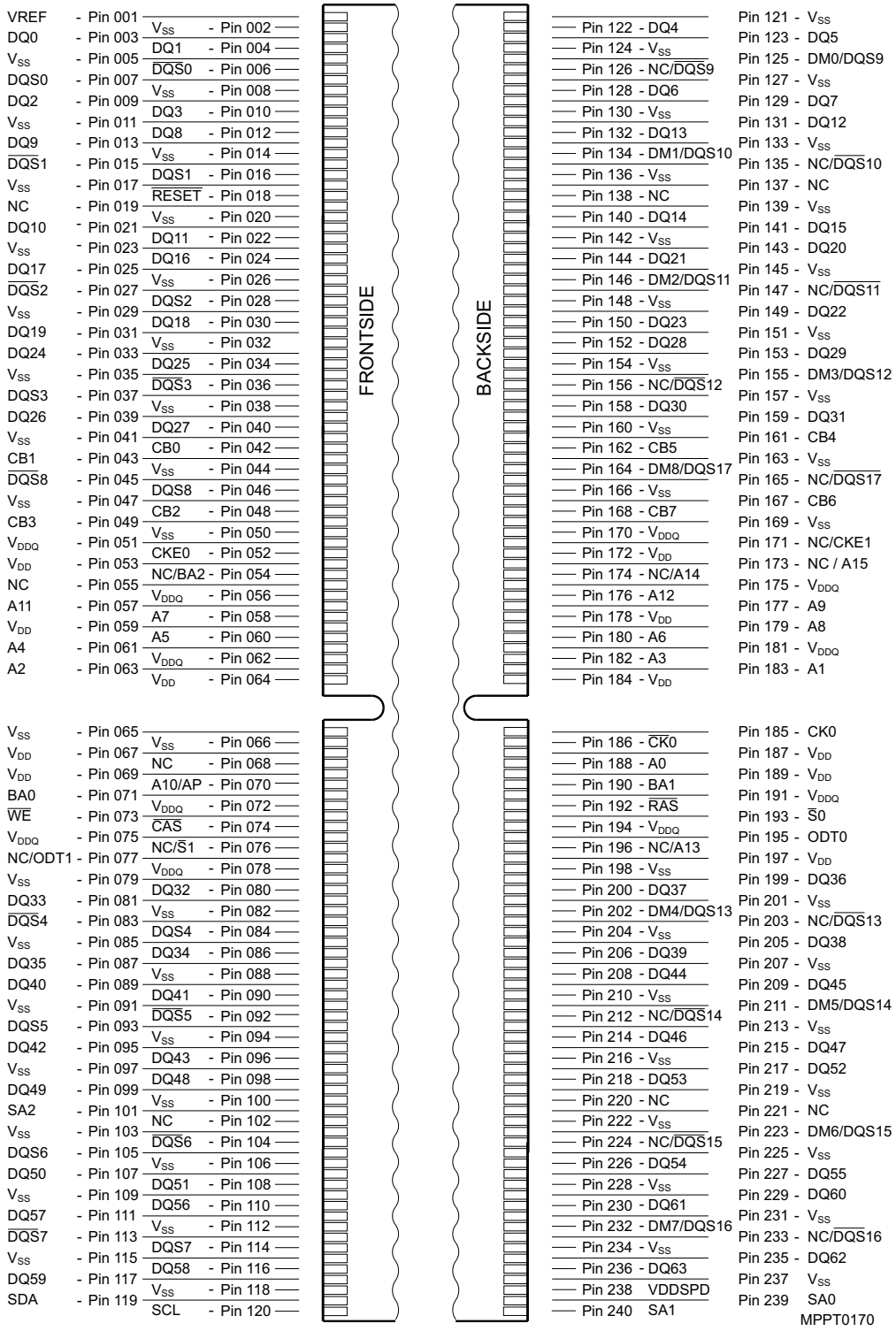
TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

TABLE 8
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

FIGURE 1
Pin Configuration for RDIMM (240 pins)



3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 9** at any time.

TABLE 9
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 10
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50 %

3.2 DC Operating Conditions

This chapter contains the DC operating conditions tables.

TABLE 11
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	—
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	—
Barometric Pressure (operating & storage)	P_{Bar}	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	—

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50 %.
5) Up to 3000 m.

TABLE 12
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	—
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	—
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	—
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	—
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 AC Characteristics

This chapter describes the AC characteristics.

3.3.1 Speed Grades Definitions

This chapter contains the Speed Grades Definitions tables.

TABLE 13
Speed Grade Definition Speed Bins for DDR2–800E

Speed Grade			DDR2–800E		Unit	Note
QAG Sort Name			–2.5			
CAS-RCD-RP latencies			6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 14
Speed Grade Definition Speed Bins for DDR2–667

Speed Grade			DDR2–667C		DDR2–667D		Unit	Note
QAG Sort Name			–3		–3S			
CAS-RCD-RP latencies			4–4–4		5–5–5		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 15
Speed Grade Definition Speed Bins for DDR2-533 and DDR2-400

Speed Grade			DDR2–533C		DDR2–400B		Unit	Note
QAG Sort Name			–3.7		–5			
CAS-RCD-RP latencies			4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) .
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 AC Timing Parameters

This chapter contains the AC Timing Parameters.

TABLE 16
Timing Parameter by Speed Grade - DDR2–800

Parameter	Symbol	DDR2–800		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–400	+400	ps	9)
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–350	+350	ps	9)
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	2500	8000	ps	10)11)
DQ and DM input setup time	$t_{DS.BASE}$	50	—	ps	12)13)14)
DQ and DM input hold time	$t_{DH.BASE}$	125	—	ps	12)13)15)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	—
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	—
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	9)16)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	200	ps	17)
CK half pulse width	t_{HP}	Min ($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	18)
DQ hold skew factor	t_{QHS}	—	300	ps	19)
DQ/DQS output hold time from DQS	t_{QH}	t_{HP} – t_{QHS}	—	ps	20)
Write command to DQS associated clock edges	WL	RL – 1		nCK	—
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	21)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	—
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	—
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	21)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	21)
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	—
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	—
Address and control input setup time	$t_{LS.BASE}$	175	—	ps	22)23)
Address and control input hold time	$t_{LH.BASE}$	250	—	ps	23)24)
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	25)26)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	25)27)
Active to precharge command	t_{RAS}	45	70000	ns	28)
Active to active command period for 1KB page size products	t_{RRD}	7.5	—	ns	28)
Active to active command period for 2KB page size products	t_{RRD}	10	—	ns	28)

Parameter	Symbol	DDR2–800		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
Four Activate Window for 1KB page size products	t_{FAW}	35	—	ns	28)
Four Activate Window for 2KB page size products	t_{FAW}	45	—	ns	28)
CAS to CAS command delay	t_{CCD}	2	—	nCK	—
Write recovery time	t_{WR}	15	—	ns	28)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	29)30)
Internal write to read command delay	t_{WTR}	7.5	—	ns	28)31)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	28)
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	28)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	—
Exit power down to read command	t_{XARD}	2	—	nCK	—
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	nCK	—
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	32)
ODT turn-on delay	t_{AOND}	2	2	nCK	—
ODT turn-on	t_{AON}	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7	ns	9)33)
ODT turn-on (Power down mode)	t_{AONPD}	$t_{AC.MIN}$ + 2	2 x $t_{CK.AVG}$ + $t_{AC.MAX}$ + 1	ns	—
ODT turn-off delay	t_{AOFD}	2.5	2.5	nCK	—
ODT turn-off	t_{AOF}	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6	ns	34)35)
ODT turn-off (Power down mode)	t_{AOFPD}	$t_{AC.MIN}$ + 2	2.5 x $t_{CK.AVG}$ + $t_{AC.MAX}$ + 1	ns	—
ODT to power down entry latency	t_{ANPD}	3	—	nCK	—
ODT to power down exit latency	t_{AXPD}	8		nCK	—
Mode register set command cycle time	t_{MRD}	2	—	nCK	—
MRS command to ODT update delay	t_{MOD}	0	12	ns	28)
OCD drive mode output delay	t_{OIT}	0	12	ns	28)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{LS} + $t_{CK.AVG}$ + t_{LH}	—	ns	—

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.

8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6\text{-}10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6\text{-}10PER).MIN}$ = – 272 ps and $t_{ERR(6\text{-}10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6\text{-}10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6\text{-}10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
12) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 2**.
13) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
14) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 2**.
16) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
17) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
18) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
19) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
20) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
21) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
22) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 3**.
23) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 3**.
25) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 1** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
26) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)}$ = $t_{RPRE.MIN}$ + $t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)}$ = $t_{RPRE.MAX}$ + $t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).

27) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).

28) For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{t_{PARAM} / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.

29) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

30) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.

31) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

32) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

33) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}.

34) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

35) When the device is operated with input clock jitter, this parameter needs to be derated by {–$t_{JIT.DUTY.MAX}$ – $t_{ERR(6\text{-}10PER).MAX}$} and {–$t_{JIT.DUTY.MIN}$ – $t_{ERR(6\text{-}10PER).MIN}$ } of the actual input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6\text{-}10PER).MIN}$ = – 272 ps, $t_{ERR(6\text{-}10PER).MAX}$ = + 293 ps, $t_{JIT.DUTY.MIN}$ = – 106 ps and $t_{JIT.DUTY.MAX}$ = + 94 ps, then $t_{AOF.MIN(DERATED)} = t_{AOF.MIN}$ + {– $t_{JIT.DUTY.MAX}$ – $t_{ERR(6\text{-}10PER).MAX}$} = – 450 ps + {– 94 ps – 293 ps} = – 837 ps and $t_{AOF.MAX(DERATED)} = t_{AOF.MAX}$ + {– $t_{JIT.DUTY.MIN}$ – $t_{ERR(6\text{-}10PER).MIN}$} = 1050 ps + {106 ps + 272 ps} = + 1428 ps. (Caution on the MIN/MAX usage!)

TABLE 17
Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	9)
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	9)
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	—
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	12)13)14)
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	13)14)15)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	—
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	—
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	9)16)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)16)
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	240	ps	17)
CK half pulse width	t_{HP}	Min ($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	18)
DQ hold skew factor	t_{QHS}	—	340	ps	19)
DQ/DQS output hold time from DQS	t_{QH}	t_{HP} – t_{QHS}	—	ps	20)
Write command to DQS associated clock edges	WL	RL–1		nCK	—

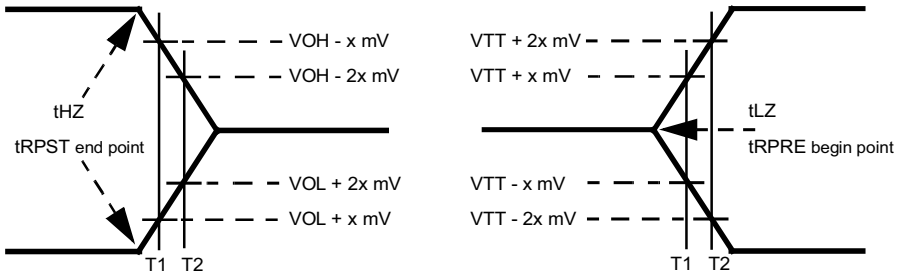
Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	21)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	—
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	—
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	21)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	21)
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	—
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	—
Address and control input setup time	$t_{LS.BASE}$	200	—	ps	22)23)
Address and control input hold time	$t_{LH.BASE}$	275	—	ps	23)24)
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	25)26)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	25)27)
Active to precharge command	t_{RAS}	45	70000	ns	28)
Active to active command period for 1KB page size products	t_{RRD}	7.5	—	ns	28)
Active to active command period for 2KB page size products	t_{RRD}	10	—	ns	28)
Four Activate Window for 1KB page size products	t_{FAW}	37.5	—	ns	28)
Four Activate Window for 2KB page size products	t_{FAW}	50	—	ns	28)
CAS to CAS command delay	t_{CCD}	2	—	nCK	—
Write recovery time	t_{WR}	15	—	ns	28)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	29)30)
Internal write to read command delay	t_{WTR}	7.5	—	ns	28)31)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	28)
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	28)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	—
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	—
Exit power down to read command	t_{XARD}	2	—	nCK	—
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	nCK	—
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	32)
ODT turn-on delay	t_{AOND}	2	2	nCK	—
ODT turn-on	t_{AON}	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7	ns	9)33)
ODT turn-on (Power down mode)	t_{AONPD}	$t_{AC.MIN}$ + 2	2 x $t_{CK.AVG}$ + $t_{AC.MAX}$ + 1	ns	—
ODT turn-off delay	t_{AOFD}	2.5	2.5	nCK	—
ODT turn-off	t_{AOF}	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6	ns	34)35)
ODT turn-off (Power down mode)	t_{AOFPD}	$t_{AC.MIN}$ + 2	2.5 x $t_{CK.AVG}$ + $t_{AC.MAX}$ + 1	ns	—

Parameter	Symbol	DDR2–667		Unit	Note[1)2)3)4)5)6)7)8)]
		Min.	Max.		
ODT to power down entry latency	t_{ANPD}	3	—	nCK	—
ODT to power down exit latency	t_{AXPD}	8		nCK	—
Mode register set command cycle time	t_{MRD}	2	—	nCK	—
MRS command to ODT update delay	t_{MOD}	0	12	ns	28)
OCD drive mode output delay	t_{OIT}	0	12	ns	28)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{LS} + t_{CK.AVG} + t_{LH}$	—	ns	—

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6\text{-}10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6\text{-}10PER).MIN}$ = – 272 ps and $t_{ERR(6\text{-}10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6\text{-}10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6\text{-}10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
12) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 2**.
13) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
14) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 2**.
16) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
17) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
18) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.

19) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
20) $t_{QH} = t_{HP} – t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
21) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
22) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 3**.
23) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 3**.
25) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 1** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
26) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN} = 0.9 \times t_{CK.AVG} – 72$ ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX} = 1.1 \times t_{CK.AVG} + 93$ ps = + 2843 ps. (Caution on the MIN/MAX usage!).
27) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN} = 0.4 \times t_{CK.AVG} – 72$ ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX} = 0.6 \times t_{CK.AVG} + 93$ ps = + 1592 ps. (Caution on the MIN/MAX usage!).
28) For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{$t_{PARAM} / t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{$t_{RP} / t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support t_{nRP} = RU{$t_{RP} / t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.
29) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
30) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
31) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.
32) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.
33) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}.
34) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.
35) When the device is operated with input clock jitter, this parameter needs to be derated by {$–t_{JIT.DUTY.MAX} – t_{ERR(6\text{-}10PER).MAX}$} and {$–t_{JIT.DUTY.MIN} – t_{ERR(6\text{-}10PER).MIN}$ } of the actual input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6\text{-}10PER).MIN}$ = – 272 ps, $t_{ERR(6\text{-}10PER).MAX}$ = + 293 ps, $t_{JIT.DUTY.MIN}$ = – 106 ps and $t_{JIT.DUTY.MAX}$ = + 94 ps, then $t_{AOF.MIN(DERATED)} = t_{AOF.MIN} + \{– t_{JIT.DUTY.MAX} – t_{ERR(6\text{-}10PER).MAX}\}$ = – 450 ps + {– 94 ps – 293 ps} = – 837 ps and $t_{AOF.MAX(DERATED)} = t_{AOF.MAX} + \{– t_{JIT.DUTY.MIN} – t_{ERR(6\text{-}10PER).MIN}\}$ = 1050 ps + {106 ps + 272 ps} = + 1428 ps. (Caution on the MIN/MAX usage!)

FIGURE 2
Method for calculating transitions and endpoint



tHZ,tRPST end point = 2*T1-T2

tLZ,tRPRE begin point = 2*T1-T2

FIGURE 3
Differential input waveform timing - t_{DS} and t_{DS}

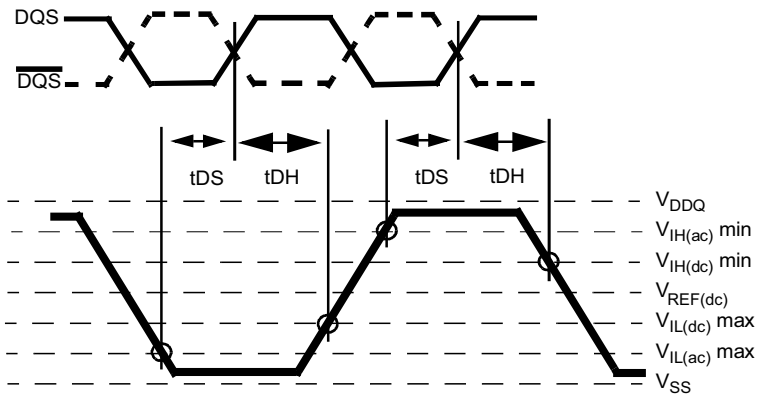


FIGURE 4
Differential input waveform timing - t_{IS} and t_{IH}

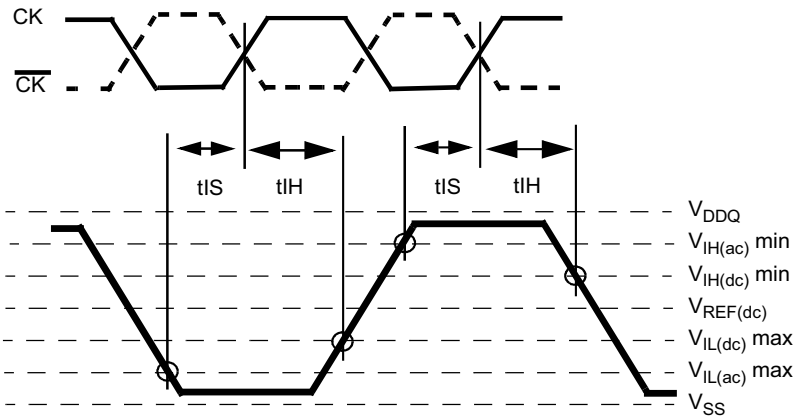


TABLE 18
Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	—
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Four Activate Window period	t_{FAW}	37.5	—	ns	—
		50	—	ns	13)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	375	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	t_{IS}(base)	250	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—	—	—

Parameter	Symbol	DDR2–533		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
Data hold skew factor	t_{QHS}	—	400	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
		—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	—
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	—
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	20)
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	22)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 3 "Ordering Information for RoHS Compliant Products" on Page 5**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
21) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.

TABLE 19
Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	—
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	—
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	—
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	—
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	—
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)22)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	9)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	10)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	—
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	—
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	—
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	—
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	11)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	11)

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	—
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	—
Four Activate Window period	t_{FAW}	37.5	—	ns	—
		50	—	ns	13)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	t_{IH}(base)	475	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	—
Address and control input setup time	t_{IS}(base)	350	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	—
OCD drive mode output delay	t_{OIT}	0	12	ns	—
Data output hold time from DQS	t_{QH}	t_{HP} –t_{QHS}	—	—	—
Data hold skew factor	t_{QHS}	—	450	ps	—
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
		—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	17)
Precharge-All (4 banks) command period	t_{RP}	t_{RP} + 1t_{CK}	—	ns	—
Precharge-All (8 banks) command period	t_{RP}	15 + 1t_{CK}	—	ns	—
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
		10	—	ns	16)20)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	—
Write preamble	t_{WPRE}	0.25 x t_{CK}	—	t_{CK}	—
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	—
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	20)
Internal Write to Read command delay	t_{WTR}	10	—	ns	21)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	22)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	22)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	—

Parameter	Symbol	DDR2–400		Unit	Note[1)2)3)4)5)6)7)]
		Min.	Max.		
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	—
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	—

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V. See notes 5)6)7)8)
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}.
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ($t_{HZ,}$ t_{RPST}), or begins driving ($t_{LZ,}$ t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C
16) 85 °C < T_{CASE} ≤ 95 °C
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 3 "Ordering Information for RoHS Compliant Products" on Page 5**.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
21) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
22) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.

3.3.3 ODT AC Electrical Characteristics

This chapter contains the ODT AC electrical characteristics tables.

TABLE 20
ODT AC Characteristics and Operating Conditions for DDR2-667 & DDR2-800

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	—
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	—
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	—
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	—

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

TABLE 21
ODT AC Characteristics and Operating Conditions for DDR2-533/DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	—
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	—
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	—
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	—
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	—

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

3.4 I_{DD} Specifications and Conditions

This chapter describes the I_{DD} Specifications and Conditions.

TABLE 22
I_{DD} Measurement Conditions

Parameter	Symbol	Note[1)2) 3)4)5)6)]
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = $CL_{.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}	
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN}$., Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	
Distributed Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	

Parameter	Symbol	Note[1)2) 3)4)5)6)]
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET is LOW. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{OUT} = 0 mA.	I_{DD7}	

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) Definitions for I_{DD} see **Table 23**
3) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
4) RESET signal is HIGH for all currents, except for I_{DD6} (Self Refresh)
5) All current measurements includes Register and PLL current consumption
6) For details and notes see the relevant QIMONDA component data sheet

TABLE 23
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	inputs are stable at a HIGH or LOW level
FLOATING	inputs are V_{REF} = V_{DDQ}/2
SWITCHING	inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.

TABLE 24

I_{DD} Specification HYS72T[32000/64001/64020]HR–2.5–A

Product Type	HYS72T32000HR–2.5–A	HYS72T64001HR–2.5–A	HYS72T64020HR–2.5–A	Unit	Note[1)]
Organization	256MB	512MB	512MB		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–2.5	–2.5	–2.5		
Symbol	Max.	Max.	Max.		
I_{DD0}	1110	1780	1150	mA	2)
I_{DD1}	1200	1960	1240	mA	2)
I_{DD2N}	880	1330	1330	mA	3)
I_{DD2P}	480	520	520	mA	3)
I_{DD2Q}	750	1060	1060	mA	3)
I_{DD3N}	880	1330	1330	mA	3)
$I_{DD3P(MRS= 0)}$	630	830	830	mA	3)
$I_{DD3P(MRS= 1)}$	480	520	520	mA	3)
I_{DD4R}	1560	2680	1600	mA	2)
I_{DD4W}	1650	2860	1690	mA	2)
I_{DD5B}	1290	2140	1330	mA	2)
I_{DD5D}	480	540	540	mA	3)4)
I_{DD6}	35	70	70	mA	3)4)
I_{DD7}	1830	3220	1870	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3) Both ranks are in the same I_{DD} mode
4) Values for 0 °C < T_{CASE} ≤ 85 °C

TABLE 25

I_{DD} Specification HYS72T[32000/64001/64020]HR–3–A

Product Type	HYS72T32000HR–3–A	HYS72T64001HR–3–A	HYS72T64020HR–3–A	Unit	Note[1]
Organization	256MB	512MB	512MB		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–3	–3	–3		
Symbol	Max.	Max.	Max.		
I_{DD0}	970	1770	1010	mA	2)
I_{DD1}	1060	1950	1100	mA	2)
I_{DD2N}	790	1410	1200	mA	3)
I_{DD2P}	430	680	470	mA	3)
I_{DD2Q}	660	1140	930	mA	3)
I_{DD3N}	790	1410	1200	mA	3)
$I_{DD3P(MRS=0)}$	560	940	730	mA	3)
$I_{DD3P(MRS=1)}$	430	690	480	mA	3)
I_{DD4R}	1380	2580	1420	mA	2)
I_{DD4W}	1420	2670	1460	mA	2)
I_{DD5B}	1240	2310	1280	mA	2)
I_{DD5D}	440	700	490	mA	3)4)
I_{DD6}	35	70	70	mA	3)4)
I_{DD7}	1690	3210	1730	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3) Both ranks are in the same I_{DD} mode
4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

TABLE 26

I_{DD} Specification HYS72T[32000/64001/64020]HR–3S–A

Product Type	HYS72T32000HR–3S–A	HYS72T64001HR–3S–A	HYS72T64020HR–3S–A	Unit	Note[1]
Organization	256MB	512MB	512MB		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–3S	–3S	–3S		
Symbol	Max.	Max.	Max.		
I_{DD0}	940	1710	980	mA	2)
I_{DD1}	1020	1870	1060	mA	2)
I_{DD2N}	790	1410	1200	mA	3)
I_{DD2P}	430	680	470	mA	3)
I_{DD2Q}	660	1140	930	mA	3)
I_{DD3N}	790	1410	1200	mA	3)
$I_{DD3P(MRS=0)}$	560	940	730	mA	3)
$I_{DD3P(MRS=1)}$	430	690	480	mA	3)
I_{DD4R}	1380	2580	1420	mA	2)
I_{DD4W}	1420	2670	1460	mA	2)
I_{DD5B}	1240	2310	1280	mA	2)
I_{DD5D}	440	700	490	mA	3)4)
I_{DD6}	35	70	70	mA	3)4)
I_{DD7}	1630	3080	1670	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3) Both ranks are in the same I_{DD} mode
4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

TABLE 27

I_{DD} Specification for HYS72T[32000/64001/64020]HR–3.7–A

Product Type	HYS72T32000HR–3.7–A	HYS72T64001HR–3.7–A	HYS72T64020HR–3.7–A	Unit	Note[1]
Organization	256MB	512MB	512MB		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–3.7	–3.7	–3.7		
Symbol	Max.	Max.	Max.		
I_{DD0}	830	1490	860	mA	2)
I_{DD1}	870	1580	910	mA	2)
I_{DD2N}	650	1130	960	mA	3)
I_{DD2P}	370	570	400	mA	3)
I_{DD2Q}	560	950	780	mA	3)
I_{DD3N}	650	1130	960	mA	3)
$I_{DD3P(MRS=0)}$	470	790	620	mA	3)
$I_{DD3P(MRS=1)}$	370	570	400	mA	3)
I_{DD4R}	1140	2120	1180	mA	2)
I_{DD4W}	1190	2210	1220	mA	2)
I_{DD5B}	1140	2120	1180	mA	2)
I_{DD5D}	380	610	440	mA	3)4)
I_{DD6}	35	70	70	mA	3)4)
I_{DD7}	1550	2930	1580	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3) Both ranks are in the same I_{DD} mode
4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

TABLE 28

I_{DD} Specification for HYS72T[32000/64001/64020]HR-5-A

Product Type	HYS72T32000HR–5–A	HYS72T64001HR–5–A	HYS72T64020HR–5–A	Unit	Note[1]
Organization	256MB	512MB	512MB		
	×72	×72	×72		
	1 Rank	1 Rank	2 Ranks		
	–5	–5	–5		
Symbol	Max.	Max.	Max.		
I_{DD0}	730	1310	760	mA	2)
I_{DD1}	770	1400	810	mA	2)
I_{DD2N}	530	910	780	mA	3)
I_{DD2P}	310	480	350	mA	3)
I_{DD2Q}	460	770	640	mA	3)
I_{DD3N}	550	950	820	mA	3)
$I_{DD3P(MRS=0)}$	390	640	510	mA	3)
$I_{DD3P(MRS=1)}$	310	480	350	mA	3)
I_{DD4R}	910	1670	940	mA	2)
I_{DD4W}	950	1760	990	mA	2)
I_{DD5B}	1040	1940	1080	mA	2)
I_{DD5D}	330	510	380	mA	3)4)
I_{DD6}	35	70	70	mA	3)4)
I_{DD7}	1400	2660	1440	mA	2)

1) Module I_{DD} is calculated on the basis of component I_{DD} and currents includes Registers and PLL. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3) Both ranks are in the same I_{DD} mode
4) Values for 0 °C ≤ T_{CASE} ≤ 85 °C

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 29
SPD Codes for PC2–6400R–666

Product Type		**HYS72T32000HR–2.5–A**	**HYS72T64001HR–2.5–A**	**HYS72T64020HR–2.5–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–6400R–666**	**PC2–6400R–666**	**PC2–6400R–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40
11	Error Correction Support (non-ECC, ECC)	02	02	02

Product Type		**HYS72T32000HR–2.5–A**	**HYS72T64001HR–2.5–A**	**HYS72T64020HR–2.5–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–6400R–666**	**PC2–6400R–666**	**PC2–6400R–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	70	70	70
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	17	17	17
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	25	25	25
34	$t_{DS.MIN}$ [ns]	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E

Product Type		HYS72T32000HR–2.5–A	HYS72T64001HR–2.5–A	HYS72T64020HR–2.5–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–6400R–666	PC2–6400R–666	PC2–6400R–666
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	4B	4B	4B
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
48	Psi(T-A) DRAM	82	82	82
49	ΔT_0 (DT0)	5B	5B	5B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	2B	2B	2B
51	ΔT_{2P} (DT2P)	29	29	29
52	ΔT_{3N} (DT3N)	29	29	29
53	$\Delta T_{3P.fast}$ (DT3P fast)	36	36	36
54	$\Delta T_{3P.slow}$ (DT3P slow)	19	19	19
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4E	4E	4E
56	ΔT_{5B} (DT5B)	17	17	17
57	ΔT_7 (DT7)	26	26	26
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	70	70	70
61	ΔT_{REG} (DTREG) / Toggle Rate	B0	B0	B0
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	F7	31	F9
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F

Product Type		HYS72T32000HR–2.5–A	HYS72T64001HR–2.5–A	HYS72T64020HR–2.5–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–6400R–666	PC2–6400R–666	PC2–6400R–666
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	32
80	Product Type, Char 8	30	31	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	52	52	52
83	Product Type, Char 11	32	32	32
84	Product Type, Char 12	2E	2E	2E
85	Product Type, Char 13	35	35	35
86	Product Type, Char 14	41	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	3x	3x	3x
92	Test Program Revision Code	xx	xx	xx

Product Type		**HYS72T32000HR–2.5–A**	**HYS72T64001HR–2.5–A**	**HYS72T64020HR–2.5–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–6400R–666**	**PC2–6400R–666**	**PC2–6400R–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 30
SPD Codes for PC2–5300R–444

Product Type		HYS72T32000HR–3–A	HYS72T64001HR–3–A	HYS72T64020HR–3–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–444	PC2–5300R–444	PC2–5300R–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	02	02	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	45

Product Type		HYS72T32000HR–3–A	HYS72T64001HR–3–A	HYS72T64020HR–3–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–444	PC2–5300R–444	PC2–5300R–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	30	30	30
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	30	30	30
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	39	39	39
42	$t_{RFC.MIN}$ [ns]	4B	4B	4B
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	52	52	52
48	Psi(T-A) DRAM	82	82	82
49	ΔT_0 (DT0)	47	47	47
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	25	25
51	ΔT_{2P} (DT2P)	29	29	29

Product Type		HYS72T32000HR–3–A	HYS72T64001HR–3–A	HYS72T64020HR–3–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–444	PC2–5300R–444	PC2–5300R–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
52	ΔT_{3N} (DT3N)	25	25	25
53	$\Delta T_{3P.fast}$ (DT3P fast)	2F	2F	2F
54	$\Delta T_{3P.slow}$ (DT3P slow)	19	19	19
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	44	44	44
56	ΔT_{5B} (DT5B)	17	17	17
57	ΔT_{7} (DT7)	24	24	24
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	68	68	68
61	ΔT_{REG} (DTREG) / Toggle Rate	94	94	94
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	A4	DE	A6
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30

Product Type		**HYS72T32000HR–3–A**	**HYS72T64001HR–3–A**	**HYS72T64020HR–3–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–5300R–444**	**PC2–5300R–444**	**PC2–5300R–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
79	Product Type, Char 7	30	30	32
80	Product Type, Char 8	30	31	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	52	52	52
83	Product Type, Char 11	33	33	33
84	Product Type, Char 12	41	41	41
85	Product Type, Char 13	20	20	20
86	Product Type, Char 14	20	20	20
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	6x	6x	6x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 31
SPD Codes for PC2–5300R–555

Product Type		HYS72T32000HR–3S–A	HYS72T64001HR–3S–A	HYS72T64020HR–3S–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–555	PC2–5300R–555	PC2–5300R–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45
11	Error Correction Support (non-ECC, ECC)	02	02	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	03	03	03
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D

Product Type		HYS72T32000HR–3S–A	HYS72T64001HR–3S–A	HYS72T64020HR–3S–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–555	PC2–5300R–555	PC2–5300R–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	4B	4B	4B
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	52	52	52
48	Psi(T-A) DRAM	82	82	82
49	ΔT_0 (DT0)	43	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	25	25

Product Type		**HYS72T32000HR–3S–A**	**HYS72T64001HR–3S–A**	**HYS72T64020HR–3S–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–5300R–555**	**PC2–5300R–555**	**PC2–5300R–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
51	ΔT_{2P} (DT2P)	29	29	29
52	ΔT_{3N} (DT3N)	25	25	25
53	$\Delta T_{3P.fast}$ (DT3P fast)	2F	2F	2F
54	$\Delta T_{3P.slow}$ (DT3P slow)	19	19	19
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	44	44	44
56	ΔT_{5B} (DT5B)	17	17	17
57	ΔT_{7} (DT7)	22	22	22
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	68	68	68
61	ΔT_{REG} (DTREG) / Toggle Rate	94	94	94
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	D1	0B	D3
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34

Product Type		HYS72T32000HR–3S–A	HYS72T64001HR–3S–A	HYS72T64020HR–3S–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–5300R–555	PC2–5300R–555	PC2–5300R–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	32
80	Product Type, Char 8	30	31	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	52	52	52
83	Product Type, Char 11	33	33	33
84	Product Type, Char 12	53	53	53
85	Product Type, Char 13	41	41	41
86	Product Type, Char 14	20	20	20
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	3x	3x	3x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 32
SPD Codes for PC2–4200R–444

Product Type		HYS72T32000HR–3.7–A	HYS72T64001HR–3.7–A	HYS72T64020HR–3.7–A
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50
11	Error Correction Support (non-ECC, ECC)	02	02	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	00	00	00
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D

Product Type		**HYS72T32000HR–3.7–A**	**HYS72T64001HR–3.7–A**	**HYS72T64020HR–3.7–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–4200R–444**	**PC2–4200R–444**	**PC2–4200R–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	4B	4B	4B
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	55	55	55
48	Psi(T-A) DRAM	82	82	82
49	ΔT_0 (DT0)	37	37	37
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	1F	1F	1F

Product Type		HYS72T32000HR–3.7–A	HYS72T64001HR–3.7–A	HYS72T64020HR–3.7–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–4200R–444	PC2–4200R–444	PC2–4200R–444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX	HEX
51	ΔT_{2P} (DT2P)	21	21	21
52	ΔT_{3N} (DT3N)	1D	1D	1D
53	$\Delta T_{3P.fast}$ (DT3P fast)	28	28	28
54	$\Delta T_{3P.slow}$ (DT3P slow)	14	14	14
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	2C	2C	2C
56	ΔT_{5B} (DT5B)	15	15	15
57	ΔT_{7} (DT7)	21	21	21
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	61	61	61
61	ΔT_{REG} (DTREG) / Toggle Rate	78	78	78
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	A8	E2	AA
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34

Product Type		HYS72T32000HR–3.7–A	HYS72T64001HR–3.7–A	HYS72T64020HR–3.7–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–4200R–444	PC2–4200R–444	PC2–4200R–444
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX	HEX
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	32
80	Product Type, Char 8	30	31	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	52	52	52
83	Product Type, Char 11	33	33	33
84	Product Type, Char 12	2E	2E	2E
85	Product Type, Char 13	37	37	37
86	Product Type, Char 14	41	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	4x	4x	4x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 33
SPD Codes for PC2–3200R–333

Product Type		HYS72T32000HR–5–A	HYS72T64001HR–5–A	HYS72T64020HR–5–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–3200R–333	PC2–3200R–333	PC2–3200R–333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	50	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60	60	60
11	Error Correction Support (non-ECC, ECC)	02	02	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	08	04	08
14	Error Checking SDRAM Width	08	04	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	00	00	00
20	DIMM Type Information	01	01	01
21	DIMM Attributes	04	05	05
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	50	50	50
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	60	60	60

Product Type		HYS72T32000HR–5–A	HYS72T64001HR–5–A	HYS72T64020HR–5–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–3200R–333	PC2–3200R–333	PC2–3200R–333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX	HEX
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28
31	Module Density per Rank	40	80	40
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37
42	$t_{RFC.MIN}$ [ns]	4B	4B	4B
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
48	Psi(T-A) DRAM	82	82	82
49	ΔT_0 (DT0)	2F	2F	2F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	19	19	19
51	ΔT_{2P} (DT2P)	21	21	21

Product Type		HYS72T32000HR–5–A	HYS72T64001HR–5–A	HYS72T64020HR–5–A
Organization		256MB	512MB	512MB
		×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)
Label Code		PC2–3200R–333	PC2–3200R–333	PC2–3200R–333
JEDEC SPD Revision		Rev. 1.1	Rev. 1.1	Rev. 1.1
Byte#	Description	HEX	HEX	HEX
52	ΔT_{3N} (DT3N)	19	19	19
53	$\Delta T_{3P.fast}$ (DT3P fast)	20	20	20
54	$\Delta T_{3P.slow}$ (DT3P slow)	14	14	14
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	26	26	26
56	ΔT_{5B} (DT5B)	14	14	14
57	ΔT_{7} (DT7)	1F	1F	1F
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	59	59	59
61	ΔT_{REG} (DTREG) / Toggle Rate	5C	5C	5C
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	D9	13	DB
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30

Product Type		**HYS72T32000HR–5–A**	**HYS72T64001HR–5–A**	**HYS72T64020HR–5–A**
Organization		**256MB**	**512MB**	**512MB**
		×72	**×72**	**×72**
		1 Rank (×8)	**1 Rank (×4)**	**2 Ranks (×8)**
Label Code		**PC2–3200R–333**	**PC2–3200R–333**	**PC2–3200R–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
79	Product Type, Char 7	30	30	32
80	Product Type, Char 8	30	31	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	52	52	52
83	Product Type, Char 11	35	35	35
84	Product Type, Char 12	41	41	41
85	Product Type, Char 13	20	20	20
86	Product Type, Char 14	20	20	20
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	4x	4x	4x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 5
Package Outline Raw Card A L-DIM-240-11

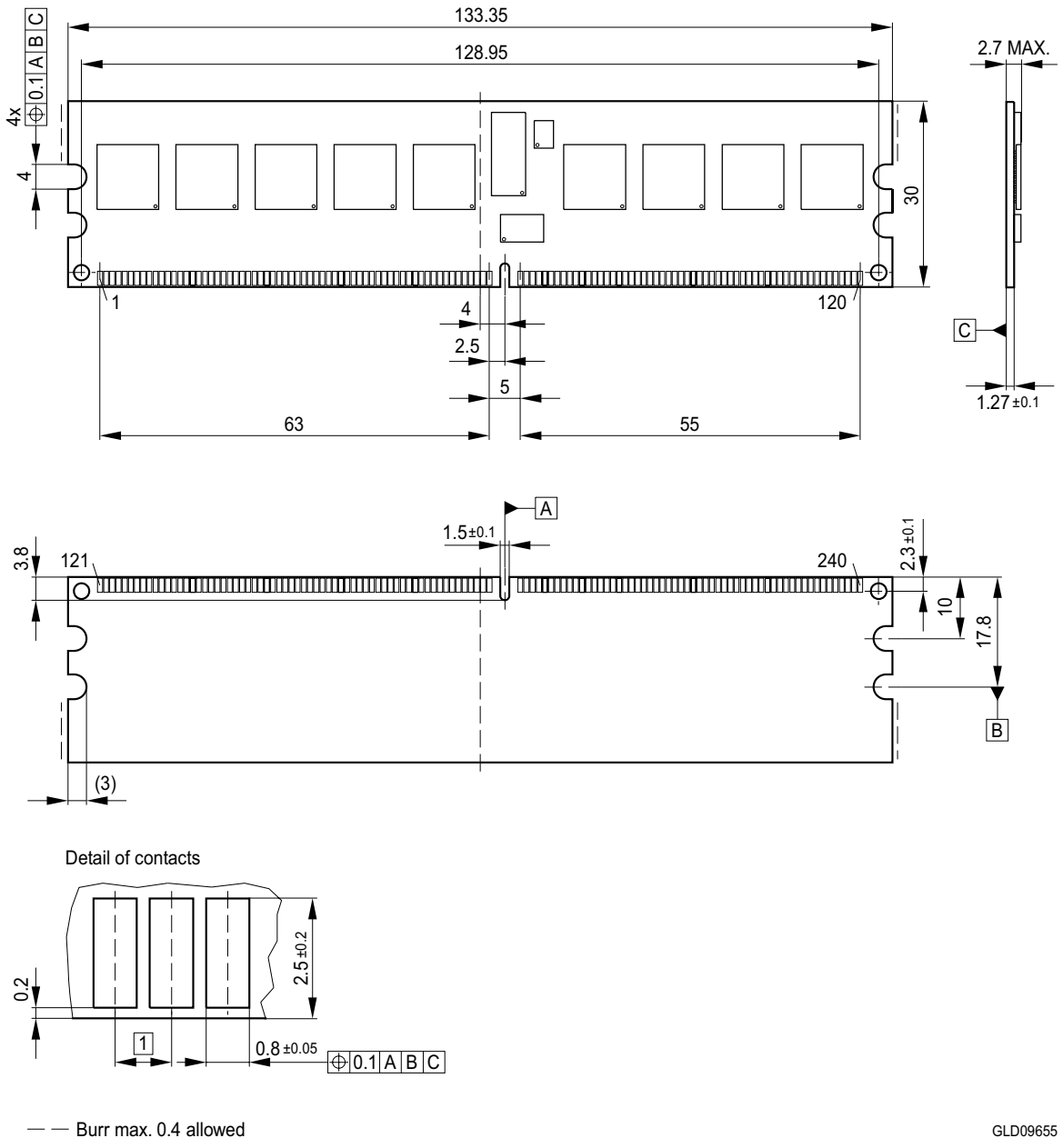


FIGURE 6
Package Outline Raw Card B-G L-DIM-240-12

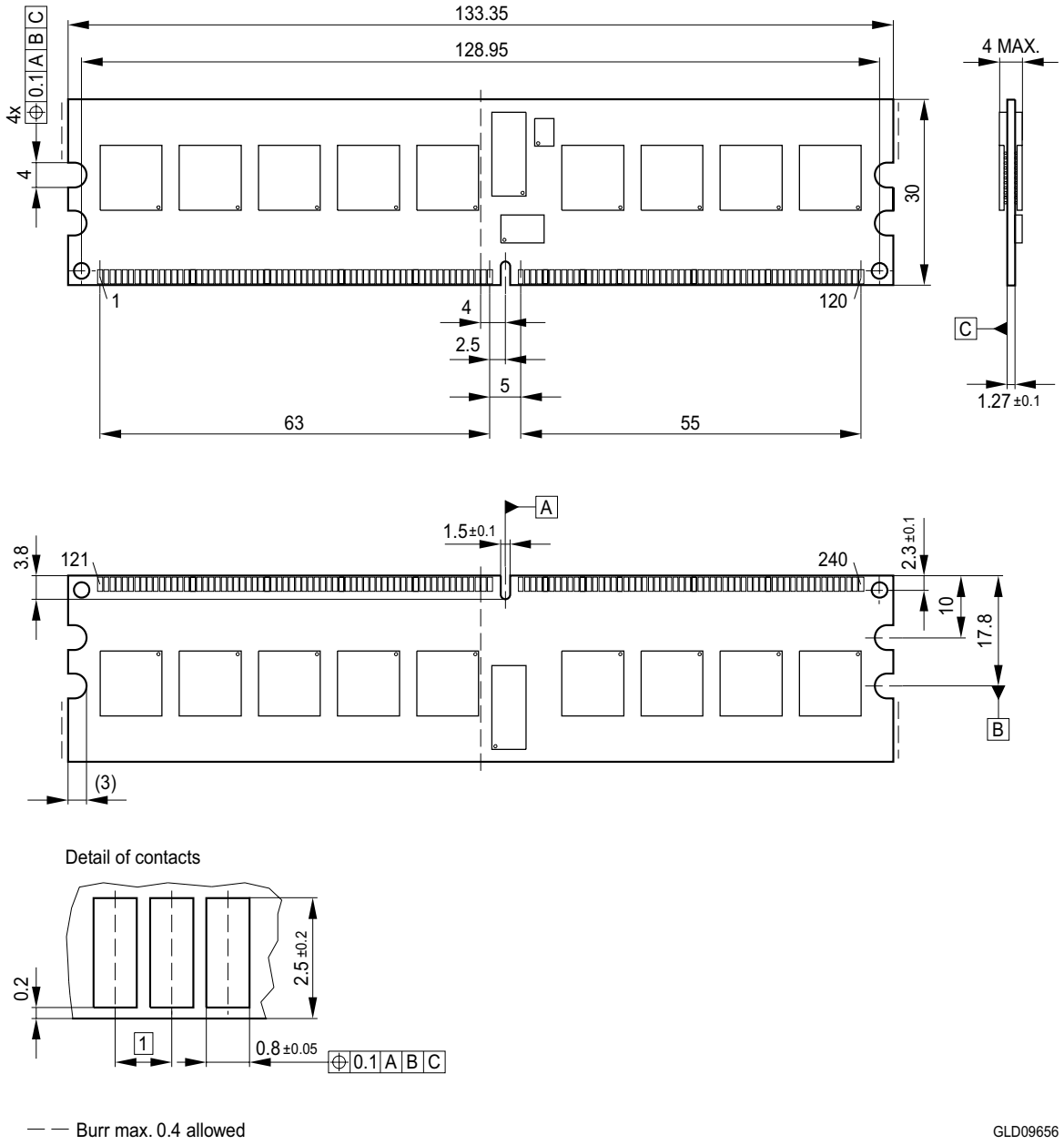
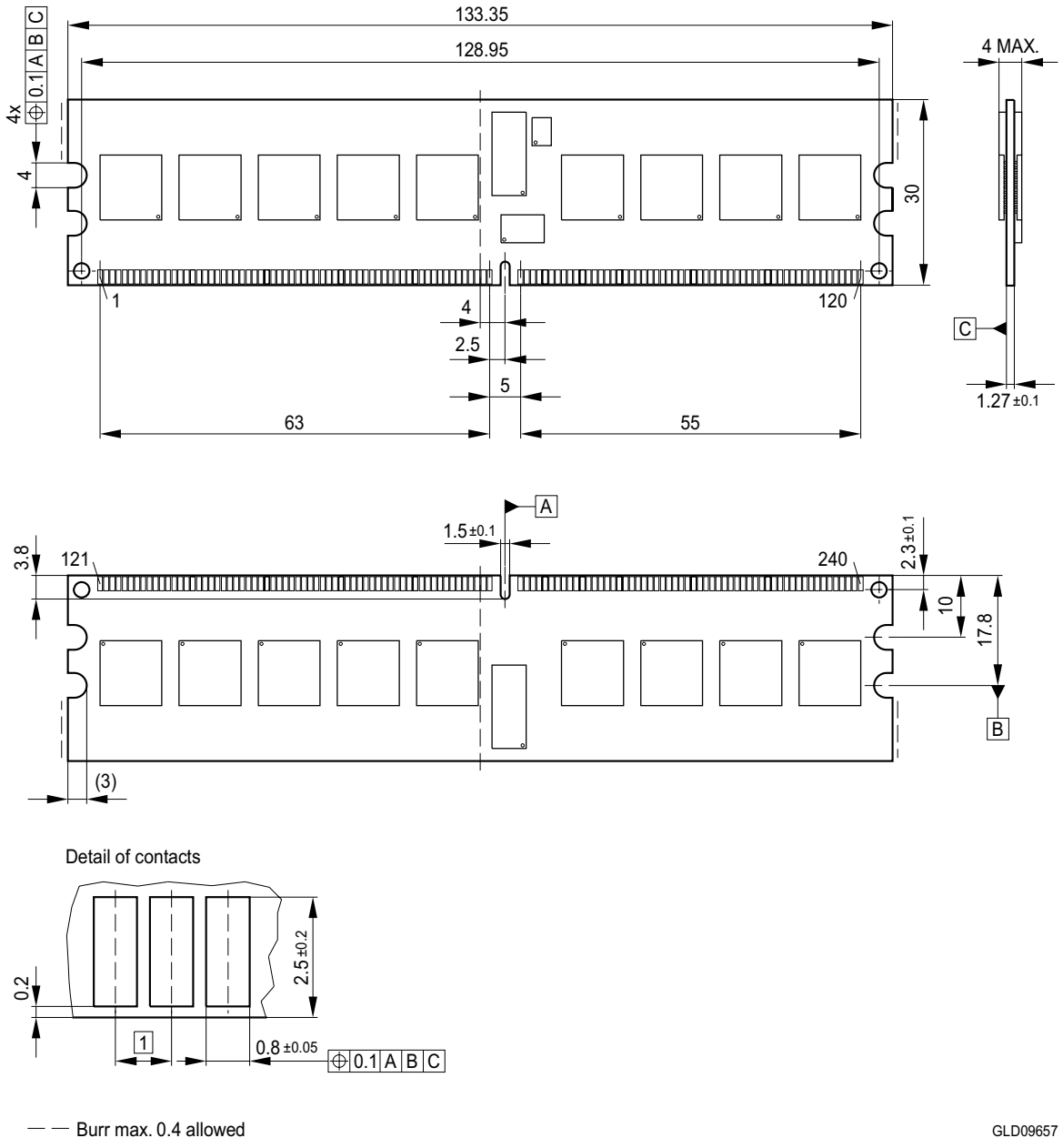


FIGURE 7
Package Outline Raw Card C L-DIM-240-13



6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some propriatory coding. **Table 34** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 35** and for components in **Table 36**.

TABLE 34
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	—

TABLE 35
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	QIMONDA Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 36
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	QIMONDA Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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