Honeywell

MIXED SIGNAL SOI GATE ARRAYS

HMX2000
FAMILY

Features

- Fabricated on Honeywell's RICMOS™ IV Silicon On Insulator (SOI) process
  - 0.8 µm Process (L_{eff} = .65 µm)
- HMX2000 supports 5V operation
- TTL, CMOS, Cold Spare compatible I/O
- 3 or 4 layer metal interconnect
- Compatible with existing HX2000 digital gate arrays
  - Sea-Of-Gates flow around embedded cells
  - Memory, A/D, D/A and other cores available
- Up to 275,000 gates useable
- Typical gate toggle power 0.6 µW/MHz/gate
- Analog on SOI provides 10dB lower substrate noise than bulk CMOS at 1GHz, 25dB lower at 100 MHz
- NMOS F_t = 15 GHz
- CrSi resistor, 2500Ω/square ± 20%
  - 300 ppm/°C temperature coefficient
- Linear Capacitors
  - 100ppm/Volt, 0.5fF/µm^2
- Vt~0.8V
- DMOS: NMOS AND PMOS > 20 Volts Breakdown
- Lateral Bipolar: β>20
- Inductors (Metal Spiral) Q~2-5, 2-5nH
- Body terminal fully oxide-isolated from substrate
- Ring Oscillator Speed ~ 150 psec/stage
- Total Dose Hardness > 1M Rad(Si)
- No Latchup

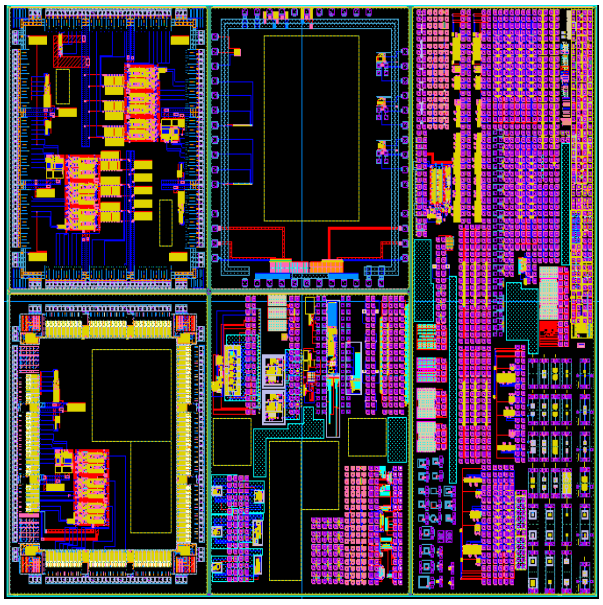
Future enhancements
- 3.3V digital supply and I/O

General Description

The HMX2000 family of arrays incorporate Mixed Signal capability as an extension of the available HX2000 Gate Array family, fabricated on Honeywell's RICMOS™ IV Silicon On Insulator (SOI) process. The SOI-IV process at Honeywell has performance advantages over bulk silicon CMOS in that 25% to 35% higher speeds can be obtained or up to 30% lower power. The SOI substrate can support a 6X improvement in static noise margins and significantly lower subthreshold leakage current.

Each HMX2000 array design is founded on our proven SOI ASIC library of SSI and MSI logic elements, available core IP (intellectual property), integratable passives, and selectable I/O pads. This family is fully compatible with Honeywell's range of high reliability screening, test and packaging options.

Designers can choose from a wide variety of I/O types. Output buffer options include 8 drive strengths, CMOS/TTL levels, IEEE 1149.1 boundry scan, pull-up/pull-down resistors, and tri-state capability. Input buffers can be selected for CMOS/TTL/Schmitt trigger levels, IEEE 1149.1 boundry scan and pull-up/pull-down resistors. Bi-directional buffers are also available.



Building blocks

- 8-bit, 8-channel A/D converter
- 12-bit current-output DAC
- Laser-trimmed precision voltage reference
- General purpose opamp, bias generators
- PLL, 2 versions, 50 –180 MHz
- Misc. Amplifiers
- Comparators
- Analog Output Buffer
- SPICE models, Custom Cell Design Services

SPECIFICATIONS

HMX2000 Characteristics	
Maximum gate count and I/O	275,000 useable gates and 388 signal I/O
Typical delay – 2 input NAND	270 ps @ 5.0V
I/O interface levels	TTL, CMOS, Schmitt trigger
Typical power consumption, µW/MHz/gate	0.6 @ 5.0V
Operating temperature range	-55°C to +125°C
Minimum Geometry	0.8 µm Drawn/ 0.65 µmL_{eff}
Analog supply level	5.0V
NMOS/PMOS V_t matching	NMOS - σ ~ 1.0 mV (large devices) PMOS - σ ~ 1.5 mV (large devices)
Poly resistor characteristics	250 ppm/°C, 250 µA/µm RMS current density, 100Ω/square ± 30%
P-well resistor characteristics	2500 ppm/°C, 20 µA/µm RMS current density, -2000 ppm/V, 2500Ω/square, ± 35%
Linear capacitor characteristics	-100 ppm/V, 0.5 fF/μm^2, 20 ppm/°C

The HMX2000 family has a cold sparing feature to allow a chip level power down mode, in which the associated busses connected to the chip can remain active. This high impedance off-state buffer feature allows users to power down portions of their system for power savings.

Honeywell's VDS™ design kit and SOI libraries provide the necessary guidance to achieve first pass design success. The VDS design kit supports industry leading Electronic Design Automation tools including those offered by Mentor Graphics, Synopsys, and Cadence. Honeywell can perform design translations to the HMX2000 ASIC family from other Computer Aided Design platforms. Customers may use familiar CAD tools and libraries to map existing designs to Honeywell library components.

Any analog tools capable of SPICE simulation can be used to design the analog part of the mixed mode design. Honeywell will provide SOI-IV Mixed Signal Design Guidelines to assist users in the design of analog functions. The basic technology parameters such as capacitance, sheet resistance, maximum operating voltage and electromigration limits along with BSIM device models are documented in the SOI-IV Electrical Rules and are available to designers.

Honeywell assigns a Customer Design Engineer to each ASIC program to provide technical assistance, telephone support, and to coordinate the design through mask release. A project manager is also assigned to communicate fab, test and package assembly status. The HMX2000 mixed mode ASIC family provides customers with an integration capability that can improve system performance while reducing power and provides system cost savings. To learn more about Honeywell's variety of custom and semi-custom IC products, call us at 763-954-2888.