Genesys Logic, Inc.

GL830

USB 2.0 to SATA Bridge Controller

Datasheet
Revision 1.02
Aug. 21, 2007

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Revision History

Revision	Date	Description
1.00	06/14/2007	First Formal Release
1.01	7/17/2007	Add 48 and 128pin description
1.02	08/21/2007	Modify LQFP48/64/128 description

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CHAPTER 1 GENERAL DESCRIPTION

The GL830 is a highly-compatible, low cost USB 2.0 to SATA bridge controller, which integrates Genesys Logic own design high speed UTMI (USB 2.0 Transceiver Macrocell Interface) transceiver/receiver and Serial ATA PHY. As a one-chip solution which complies with Universal Serial Bus specification rev. 2.0 and Serial ATA specification rev. 2.6. There are totally 4 endpoints in the GL830 controller, Control (0), Bulk In (1), Bulk Out (2), and Interrupt (3). By complies with the USB Storage Class specification ver.1.0 (Bulk only protocol), the GL830 can support not only plug and play but also Windows Vista/ XP/ 2000/ ME default driver. The GL830 uses 25MHz crystal and slew-rate controlled pads to reduce the EMI issue. With 64-pin LQFP (7mmX7mm) package, the GL830 is the best cost/ performance solution to fit different situations in the USB 2.0 high speed storage class applications such as SATA HDD and ODD.

CHAPTER 2 FEATURES

· Complies with Universal Serial Bus specification rev. 2.0.

· Complies with USB Storage Class specification ver.1.0. (Bulk only protocol)

· Operating system supported: Win Vista/ Win XP / 2000 / Me / 98 / 98SE; Mac OS 9.X / X.

· Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).

· Support 4 endpoints: Control (0) / Bulk Read (1) / Bulk Write (2) / Interrupt (3).

· 64 / 512 bytes Data Payload for full / high speed Bulk Endpoint.

· Complies with Serial ATA specification rev. 2.6.

· Support SATA hot-plug

· Support Spread Spectrum Clocking to reduce EMI

· Support Partial/Slumber power management

· Provide adjustable TX signal amplitude and pre-emphasis level

· Provide specified OOB signal detection and transmission

· Embedded Turbo 8051.

· ROM size: 12k words; RAM size: 1280 bytes. (Bulk Buffer: 512 words, MC RAM: 256 bytes)

· Supports Power Down mode and USB suspend indicator.

· Supports USB 2.0 TEST mode features.

· Supports 4 PIO and 4GPIO for programmable AP.

· Supports device power control for power on/off when running suspend mode.

· Provides LED indicator for Full Speed and High Speed .

· using 25 MHz external clock to provide better EMI.

· 3.3V power input; 5V tolerance pad.

· Supports Wakeup ability.

· Embedded Regulator (3.3V to 1.8V).

· Embedded Regulator (5V to 3.3V).

· Provides SPI interface for Finger Print (only for 64 pin package).

· Available in 48/64/128-pin LQFP.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

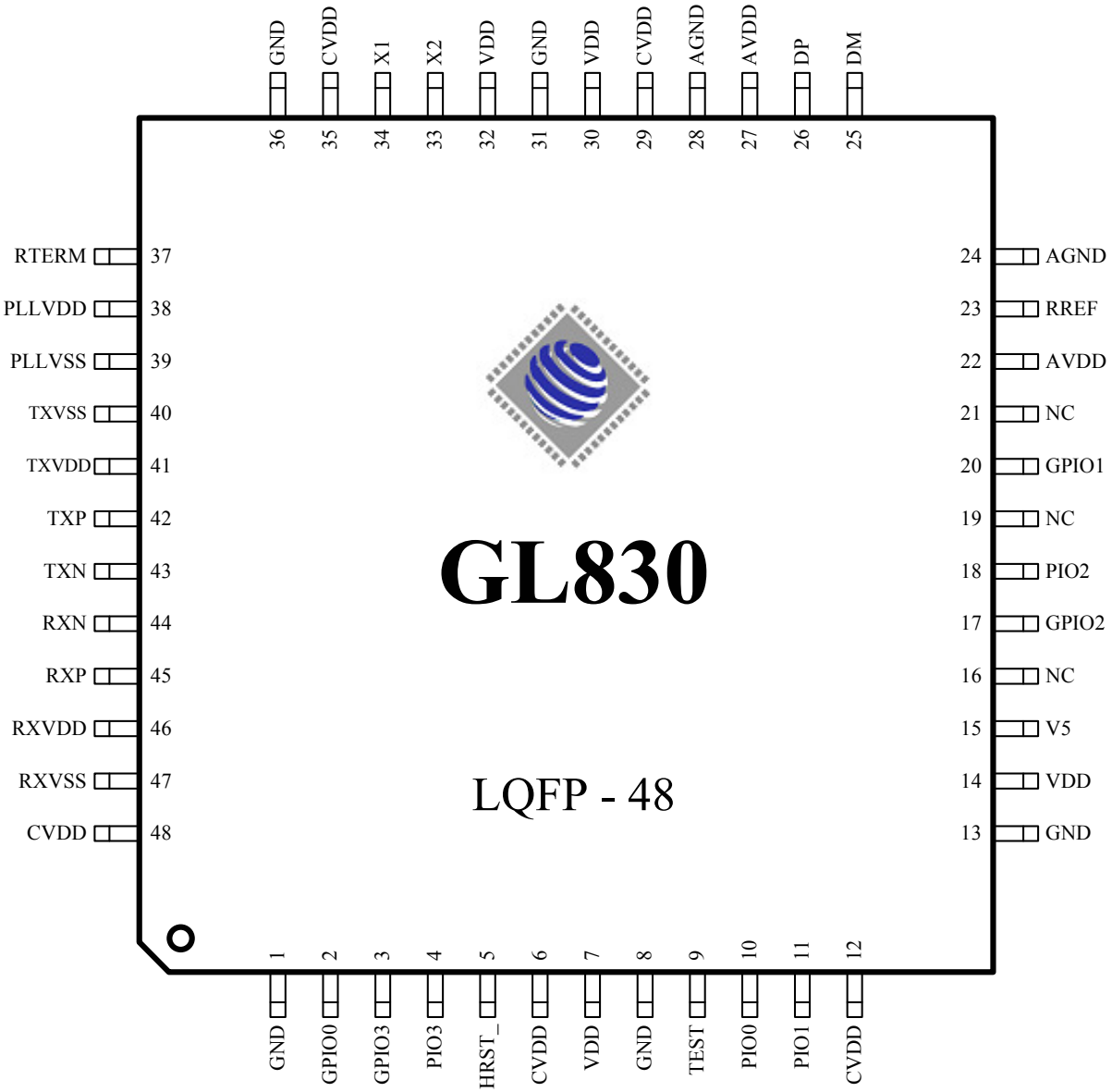


Figure 3.1 - 48 Pin LQFP Pinout Diagram

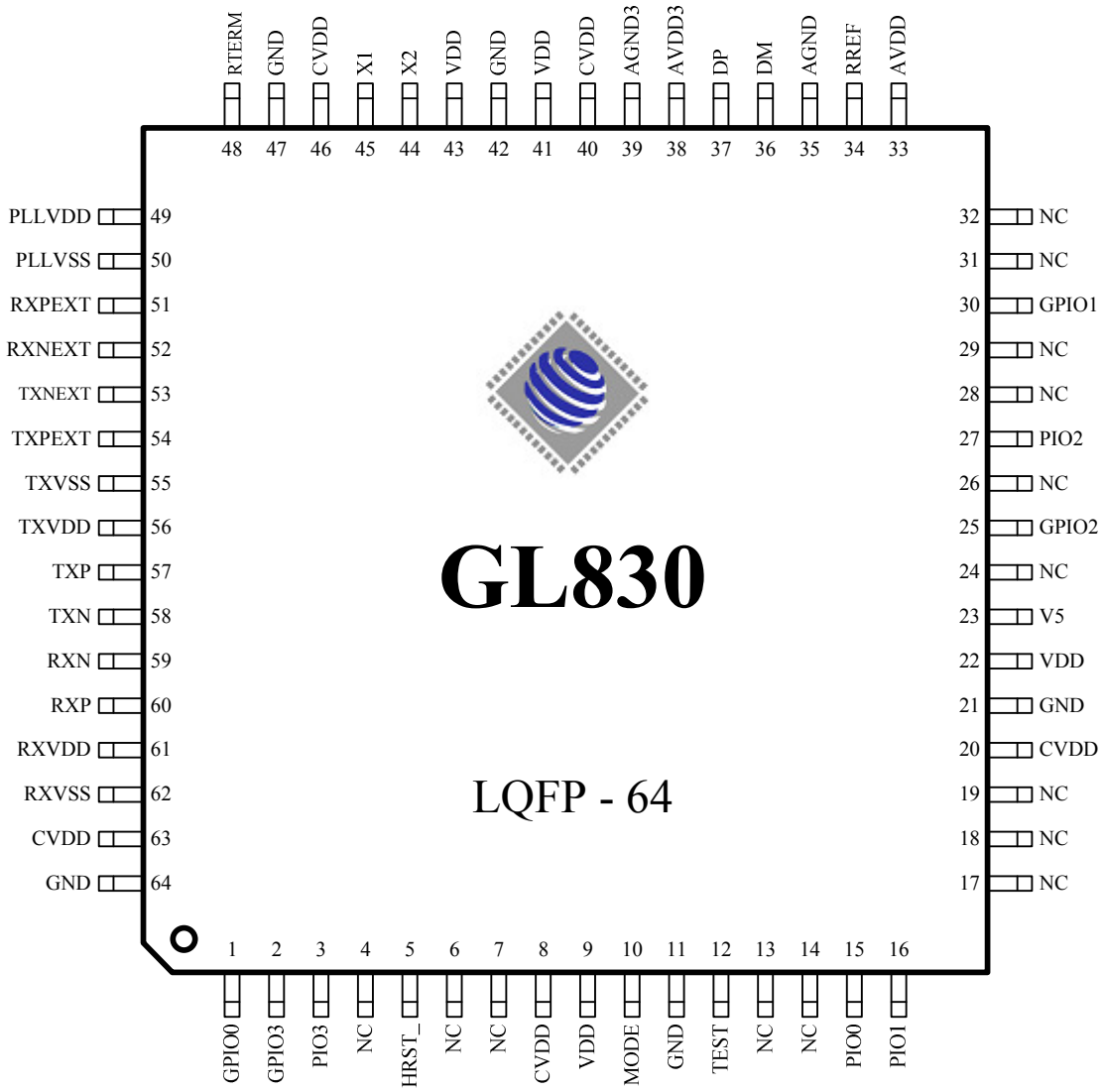


Figure 3.2 - 64 Pin LQFP Pinout Diagram

Figure 3.3 - 128 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1 – 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	GND	P	13	GND	P	25	DM	B	37	RTERM	A
2	GPIO0	B	14	VDD	P	26	DP	B	38	PLLVDD	P
3	GPIO3	B	15	V5	P	27	AVDD	P	39	PLLVSS	P
4	PIO3	B	16	NC	-	28	AGND	P	40	TXVSS	P
5	HRST_	I	17	GPIO2	B	29	CVDD	P	41	TXVDD	P
6	CVDD	P	18	PIO2	B	30	VDD	P	42	TXP	O
7	VDD	P	19	NC	-	31	GND	P	43	TXN	O
8	GND	P	20	GPIO1	B	32	VDD	P	44	RXN	I
9	TEST	I	21	NC	-	33	X2	B	45	RXP	I
10	PIO0	B	22	AVDD	P	34	X1	I	46	RXVDD	P
11	PIO1	B	23	RREF	A	35	CVDD	P	47	RXVSS	P
12	CVDD	P	24	AGND	P	36	GND	P	48	CVDD	P

Table 3.2 – 64 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	GPIO0	B	17	NC	-	33	AVDD	P	49	PLLVDD	P
2	GPIO3	B	18	NC	-	34	RREF	A	50	PLLVSS	P
3	PIO3	B	19	NC	-	35	AGND	P	51	RXPEXT	I
4	NC	-	20	CVDD	P	36	DM	B	52	RXNEXT	I
5	HRST_	I	21	GND	P	37	DP	B	53	TXNEXT	O
6	NC	-	22	VDD	P	38	AVDD3	P	54	TXPEXT	O
7	NC	-	23	V5	P	39	AGND3	P	55	TXVSS	P
8	CVDD	P	24	NC	-	40	CVDD	P	56	TXVDD	P
9	VDD	P	25	GPIO2	B	41	VDD	P	57	TXP	O
10	MODE	I	26	NC	-	42	GND	P	58	TXN	O
11	GND	P	27	PIO2	B	43	VDD	P	59	RXN	I
12	TEST	I	28	NC	-	44	X2	B	60	RXP	I
13	NC	-	29	NC	-	45	X1	I	61	RXVDD	P

14	NC	-	30	GPIO1	B	46	CVDD	P	62	RXVSS	P
15	PIO0	B	31	NC	-	47	GND	P	63	CVDD	P
16	PIO1	B	32	NC	-	48	RTERM	A	64	GND	P

Table 3.3 – 128 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	GPIO0	B	33	PIO0	B	65	AINTRQ	B	97	NC	-
2	GPIO3	B	34	PIO1	B	66	AVDD	P	98	NC	-
3	PIO4	B	35	ROM_A0	O	67	AVDD	P	99	NC	-
4	PIO3	B	36	DD2	B	68	RREF	A	100	NC	-
5	ROM_A5	O	37	ROM_D0	B	69	AGND	P	101	NC	-
6	DD7	B	38	DD13	B	70	AGND	P	102	NC	-
7	ROM_A11	O	39	ROM_D7	B	71	DM	B	103	NC	-
8	DD8	B	40	DD1	B	72	DP	B	104	PLLVDD	P
9	HRST_	I	41	ROM_D1	B	73	AVDD	P	105	PLLVDD	P
10	DD6	B	42	DD14	B	74	AGND	P	106	PLLVSS	P
11	ROM_A4	O	43	ROM_D6	B	75	GND	P	107	RXPEXT	I
12	DD9	B	44	DD0	B	76	GND	P	108	RXNEXT	I
13	ROM_A12	O	45	ROM_D2	B	77	CVDD	P	109	TXNEXT	O
14	DD5	B	46	DD15	B	78	DA1	B	110	TXPEXT	O
15	ROM_A3	O	47	CVDD	P	79	DA0	B	111	TXVSS	P
16	CVDD	P	48	GND	P	80	NC	-	112	TXVDD	P
17	CVDD	P	49	MODE1	I	81	DA2	B	113	TXP	O
18	VDD	P	50	VDD	P	82	ROM_D3	B	114	TXN	O
19	MOD0	I	51	VDD	P	83	CS0_	B	115	RXN	I
20	GND	P	52	V5	I	84	ROM_D4	B	116	RXP	I
21	DD10	B	53	ROM_D5	B	85	CS1_	B	117	RXVDD	P
22	ROM_A13	O	54	DMARQ	B	86	GND	P	118	RXVSS	P
23	TEST	I	55	GPIO2	B	87	VDD	P	119	CVDD	P
24	TXD	O	56	DIOW_	B	88	VDD	P	120	GND	P
25	RXD	B	57	PIO2	B	89	GND	P	121	NC	-

26	DD4	B	58	DIOR_	B	90	GND	P	122	ROM_A8	O
27	ROM_A2	O	59	T_ROM	I	91	VDD	P	123	ROM_A7	O
28	DD11	B	60	IORDY	B	92	X2	B	124	ROM_A9	O
29	ROM_A14	O	61	GPIO1	B	93	X1	I	125	ROM_A6	O
30	DD3	B	62	DMACK_	B	94	VDD	P	126	ROM_A10	O
31	ROM_A1	O	63	PHYRDY	O	95	GND	P	127	ARESET_	B
32	DD12	B	64	GPIO4	B	96	RTERM	A	128	SPDSEL	I

3.3 Pin Descriptions

Table 3.4 – 48 Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
RREF	23	A	Reference resistor
DM	25	B	HS D-
DP	26	B	HS D+
AVDD	22,27	P	USB Analog 3.3V power
AGND	24,28	P	USB Analog Ground

SATA Interface			
Pin Name	**Pin#**	**Type**	**Description**
RTERM	37	A	Reference resistor
PLLVDD	38	P	1.8V Power Supplies for internal PLL
PLLVSS	39	P	Ground for internal PLL
TXVSS	40	P	Ground for transceiver part
TXVDD	41	P	1.8V Power Supplies for transceiver part
TXP	42	O	SATA Differential Transmit TX+
TXN	43	O	SATA Differential Transmit TX-
RXN	44	I	SATA Differential Receive RX-
RXP	45	I	SATA Differential Receive RX+
RXVDD	46	P	1.8V Power Supplies for receiver part
RXVSS	47	P	Ground for receiver part

Digital Power and Ground			
Pin Name	**Pin#**	**Type**	**Description**

CVDD	6,12,29, 35,48	P	1.8V Digital Power
VDD	7,14 30, 32	P	3.3V Digital Power
GND	1,8,13, 31,36	P	Digital Ground
V5	15	p	5V Power Input

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
TEST	9	I (pd)	Test Mode Input
X2	33	B	Crystal Output
X1	34	I	Crystal Input
HRST_	5	I (pu)	Reset Pin
GPIO0~3	2,20,17,3	B (pu)	General Purpose I/O #0~#3
PIO0~3	10,11,18, 4	B (pd)	Programmable I/O #0~#3
NC	16,19,21	-	No connection

Table 3.5 – 64 Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
RREF	34	A	Reference resistor
DM	36	B	HS D-
DP	37	B	HS D+
AVDD	33,38	P	USB Analog 3.3V power
AGND	35,39	P	USB Analog Ground

SATA Interface			
Pin Name	**Pin#**	**Type**	**Description**
RTERM	48	A	Reference resistor
PLLVDD	49	P	1.8V Power Supplies for internal PLL
PLLVSS	50	P	Ground for internal PLL
RXPEXT	51	I	eSATA Differential Receive RX+
RXNEXT	52	I	eSATA Differential Receive RX-

TXNEXT	53	O	eSATA Differential Transmit TX-
TXPEXT	54	O	eSATA Differential Transmit TX+
TXVSS	55	P	Ground for transceiver part
TXVDD	56	P	1.8V Power Supplies for transceiver part
TXP	57	O	SATA Differential Transmit TX+
TXN	58	O	SATA Differential Transmit TX-
RXN	59	I	SATA Differential Receive RX-
RXP	60	I	SATA Differential Receive RX+
RXVDD	61	P	1.8V Power Supplies for receiver part
RXVSS	62	P	Ground for receiver part

Digital Power and Ground			
Pin Name	**Pin#**	**Type**	**Description**
CVDD	8,20,40, 46,63	P	1.8V Digital Power
VDD	9,22,41, 43	P	3.3V Digital Power
GND	11,21,42, 47,64	P	Digital Ground
V5	23	p	5V Power Input

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
TEST	12	I (pd)	Test Mode Input
X2	44	B	Crystal Output
X1	45	I	Crystal Input
HRST_	5	I (pu)	Reset Pin
MODE	10	I (pd)	Mode Select (0=> USB to SATA; 1=> eSATA to SATA)
GPIO0~3	1,30,25,2	B (pu)	General Purpose I/O #0~#3
PIO0~3	15,16,27, 3	B (pd)	Programmable I/O #0~#3
NC	4,6,7,13, 14,17,18, 19,24,26, 28,29,31, 32	-	No connection

Table 3.6 – 128 Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
RREF	68	A	Reference resistor
DM	71	B	HS D-
DP	72	B	HS D+
AVDD	66,67,73	P	USB Analog 3.3V power
AGND	69,70,74	P	USB Analog Ground

SATA Interface			
Pin Name	**Pin#**	**Type**	**Description**
RTERM	96	A	Reference resistor
PLLVDD	104,105	P	1.8V Power Supplies for internal PLL
PLLVSS	106	P	Ground for internal PLL
RXPEXT	107	I	eSATA Differential Receive RX+
RXNEXT	108	I	eSATA Differential Receive RX-
TXNEXT	109	O	eSATA Differential Transmit TX-
TXPEXT	110	O	eSATA Differential Transmit TX+
TXVSS	111	P	Ground for transceiver part
TXVDD	112	P	1.8V Power Supplies for transceiver part
TXP	113	O	SATA Differential Transmit TX+
TXN	114	O	SATA Differential Transmit TX-
RXN	115	I	SATA Differential Receive RX-
RXP	116	I	SATA Differential Receive RX+
RXVDD	117	P	1.8V Power Supplies for receiver part
RXVSS	118	P	Ground for receiver part

Digital Power and Ground			
Pin Name	**Pin#**	**Type**	**Description**
CVDD	16,17,47, 77,119	P	1.8V Digital Power
VDD	18,50,51 87,88,91, 94	P	3.3V Digital Power
GND	20,48,75, 76,86,89, 90,95, 120	P	Digital Ground

V5	52	p	5V Power Input

ATA/ ATAPI Interface (Host mode)			
Pin Name	**Pin#**	**Type**	**Description**
DD0~15	44,40,36, 30,26,14, 10,6,8,12, 21,28,32, 38,42,46	B	IDE Data Bus
ARESET_	127	I (pu)	Device Reset
CS1_, CS0_	85, 83	I (pu)	Chip Select #1,#0
DA0~2	79,78,81	I (pd)	IDE Address #2,#1,#0
INTRQ	65	O	IDE interrupt input
DMACK_	62	I (pu)	IDE Acknowledge
IORDY	60	O	IDE Ready
DIOR_	58	I (pu)	IDE read signal
DIOW_	56	I (pu)	IDE write signal
DMARQ	54	O	IDE request

ATA/ ATAPI Interface (Device mode)			
Pin Name	**Pin#**	**Type**	**Description**
DD0~15	44,40,36, 30,26,14, 10,6,8,12, 21,28,32, 38,42,46	B	IDE Data Bus
ARESET_	127	O	Device Reset
CS1_, CS0_	85, 83	O	Chip Select #1,#0
DA0~2	79,78,81	O	IDE Address #2,#1,#0
INTRQ	65	I (pd)	IDE interrupt input
DMACK_	62	O	IDE Acknowledge
IORDY	60	I (pu)	IDE Ready
DIOR_	58	O	IDE read signal
DIOW_	56	O	IDE write signal
DMARQ	54	I (pd)	IDE request

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
TEST	23	I (pd)	Test Mode Input
X2	92	B	Crystal Output
X1	93	I	Crystal Input
HRST_	9	I (pu)	Reset Pin
MODE0,1	19,49	I (pd)	Mode Select 00=> USB to SATA; 10=> eSATA to SATA; 01=> USB to PATA; 11=> SATA to PATA When MODE0,1=11, PIO1=0 is device mode. When MODE0,1=11, PIO1=1 is host mode.
GPIO0~4	1,61,55,2,64	B (pu)	General Purpose I/O #0~#4
PIO0~4	33,34,57,4,3	B (pd)	Programmable I/O #0~#4
TXD	24	O (pu)	8051 UART TXD
RXD	25	B (pu)	8051 UART RXD
SPDSEL	128	I (pd)	0 => force in 1.5G; 1 => negotiate interface speed with attached device (1.5G or 3G)
PHYRDY	63	O	SATA PHY ready
T_ROM	59	I (pd)	0 => Internal ROM; 1 => External ROM
ROM_A0~14	35,31,27,15,11,5,125,123,122,124,126,7,13,22,29	O	ROM Address #0~#14
ROM_D0~7	37,41,45,82,84,53,43,39	B (pd)	ROM Data #0~#7
NC	80,97,98,99,100,101,102,103	-	No connection

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog

SO	Automatic output low when suspend
pu	Internal pull up
pd	Internal pull down
odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

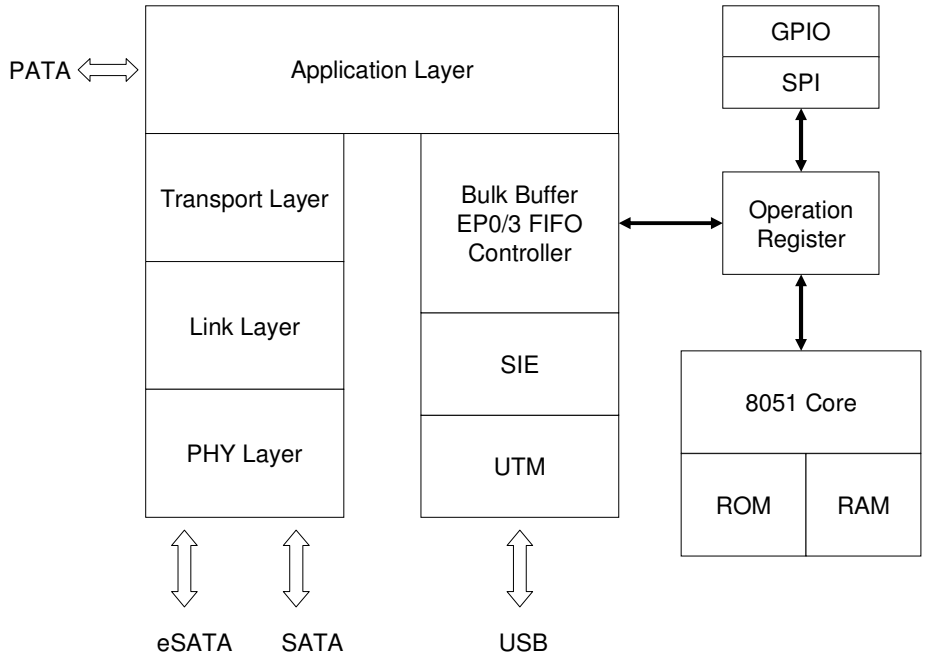


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0/EP3 FIFO and Bulk Buffer

Endpoint 0/3 FIFO: The Control and Interrupt FIFO. It is composed of TX03FIFO and RX03FIFO, with 64-byte FIFO each, and it is used for endpoint 0/3 data transfer.

Bulk Buffer: It is constructed in interleaved architecture and composed by two data buffers which is used to store data transferred between USB host and IDE device.

5.4 Operation Register

It is a register space to store status information and to control the functions of GL830 by 8051.

5.5 SPI Interface

The Serial Peripheral Interface is a serial, synchronous communication protocol. It is compatible with Motorola's SPI specifications.

5.6 PHY Layer

It has elastic buffer and supports receiver detection, data serialization and de-serialization.

5.7 Link Layer

The Link layer transmits and receives frames, transmits primitives based on control signals from the Transport layer, and receives primitives from the Phy layer which are converted to control signals to the Transport layer.

5.8 Transport Layer

The Transport layer constructs Frame Information Structures for transmission and decomposes received Frame Information Structure

5.9 Application Layer

The Application Layer translates the ATA operation onto internal protocols.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Digital I/O pad power supply voltage	3.0	3.3	3.6	V
Vcore	Digital power supply voltage	1.62	1.8	1.98	V
V_{AUSB}	Analog power supply voltage for USB PHY	3.0	3.3	3.6	V
V_{ASATA}	Analog power supply voltage for SATA PHY	1.62	1.8	1.98	V
V_{ESD}	Static discharge voltage	4000			V
T_A	Ambient Temperature	0		100	°C

6.2 Temperature Conditions

Table 6.2 - Temperature Conditions

Item	Value
Storage Temperature	-50°C ~ 150 °C
Operating Temperature	0 °C ~ 70 °C

6.3 DC Characteristics

6.3.1 I/O Type digital pins

Table 6.3 - I/O Type digital pins

Parameter	Min.	Typ.	Max.	Unit
Current sink @ V_{OL} = 0.4V	10.58	14.21	16.87	mA
Current output @ V_{OH} = 2.4V (TTL high)	14.74	27.46	43.0	mA
Falling slew rate at 30 pF loading capacitance	0.56	0.91	1.28	V/ns
Rising slew rate at 30 pF loading capacitance	0.58	0.91	1.72	V/ns
Schmitt trigger low to high threshold point	1.4	1.5	1.6	V
Schmitt trigger low to high threshold point	1.4	1.5	1.6	V
Pad internal pull up resister	37.87K	64.7K	108.11K	Ohms
Pad internal pull down resister	29.85K	59.45K	134.26K	Ohms

6.3.2 USB Interface DC Characteristics

The GL830 conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

6.3.3 SATA Interface DC Characteristics

The GL830 conforms to DC characteristics for Serial ATA specification rev. 2.6. Please refer to this specification for more information.

6.3.4 Reference Clock Input Requirement

Table 6.6 - Reference Clock Input Requirement

Parameter	Min.	Typ.	Max.	Unit
X1 crystal frequency		25		MHz
X1 cycle time		40		ns

6.3.5 Reference Resistor Requirement

Table 6.7 - Reference Resistor Requirement

Parameter	Min.	Typ.	Max.	Unit
USB Reference Resistor		680		Ohms
SATA Reference Resistor		5.1K		Ohms

6.4 AC Characteristics

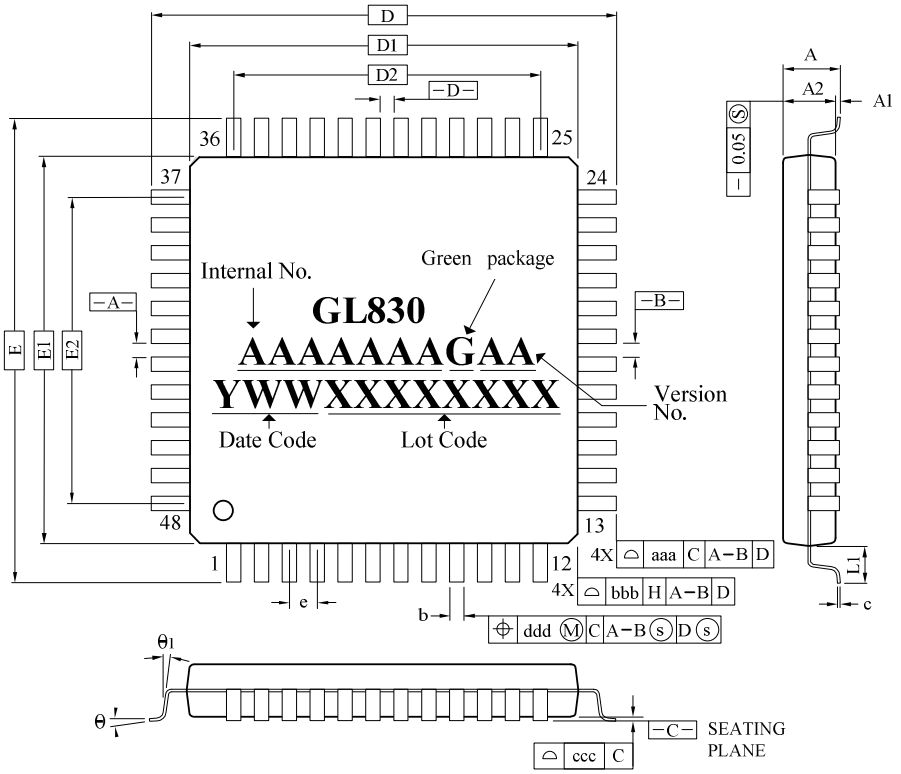
6.4.1 USB Interface AC Characteristics

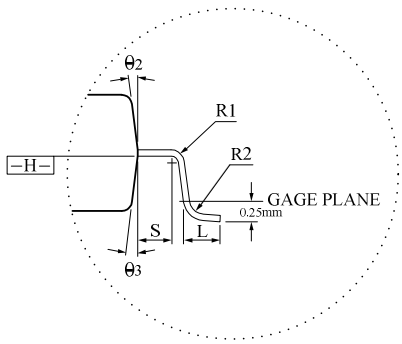
The GL830 conforms to all timing diagrams and specifications for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

6.4.2 SATA Interface AC Characteristics

The GL830 conforms to all timing diagrams and specifications for Serial ATA specification rev. 2.6. Please refer to this specification for more information.

CHAPTER 7 PACKAGE DIMENSION





NOTES :

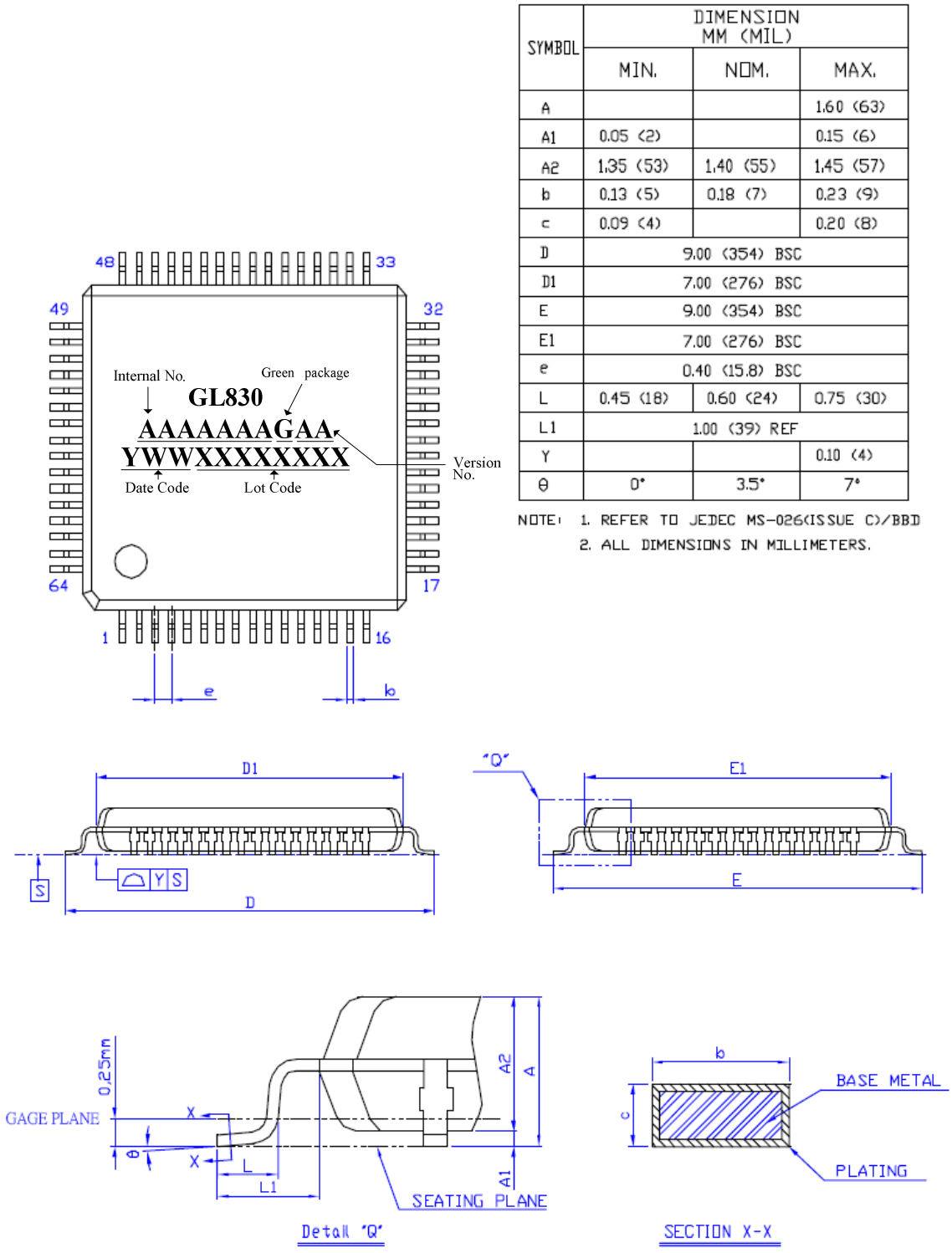
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

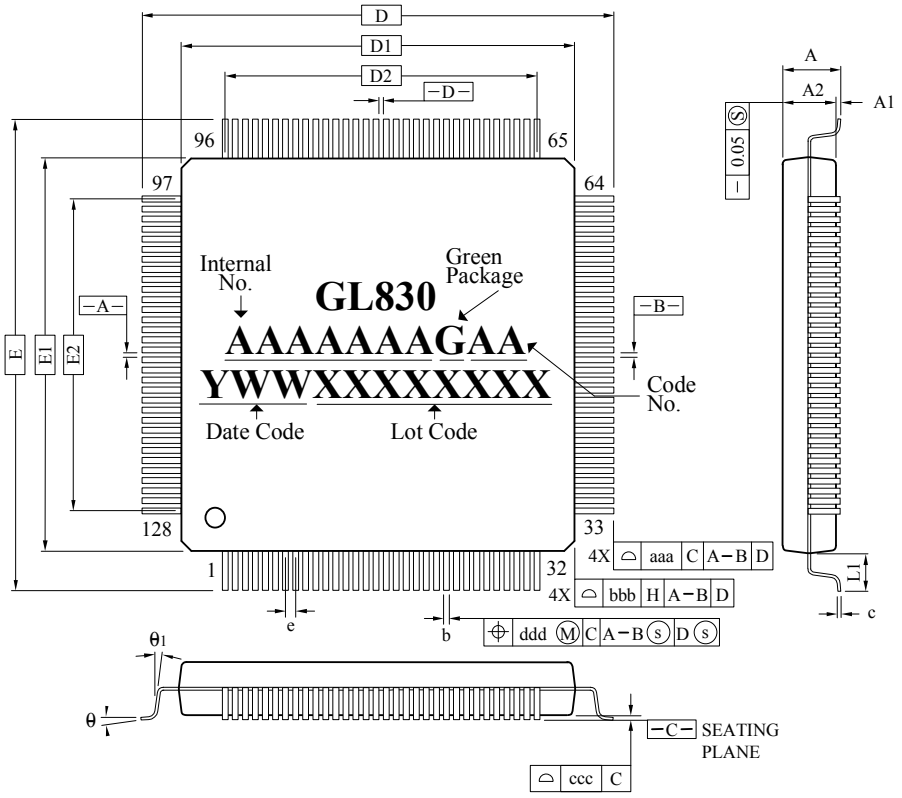
Figure 7.1 – GL830 48 Pin LQFP Package

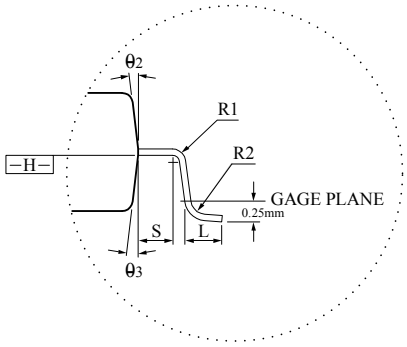


SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.13 (5)	0.18 (7)	0.23 (9)
c	0.09 (4)		0.20 (8)
D	9.00 (354) BSC		
D1	7.00 (276) BSC		
E	9.00 (354) BSC		
E1	7.00 (276) BSC		
e	0.40 (15.8) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026(ISSUE C)/BBD
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.2 - GL830 64 Pin LQFP Package





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 7.3 - GL830 128 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL830-MNGXX	48-pin LQFP	Green Package	XX	Available
GL830-MSGXX	64-pin LQFP	Green Package	XX	Available
GL830-MXGXX	128-pin LQFP	Green Package	XX	Available