High Speed, Integrated Ultrasound Driver IC

Features

- Drives two ultrasound transducer channels
- Generates 5-level waveform
- Drives 12 high voltage MOSFETs
- ±2.0A source and sink peak current
- Up to 20MHz output frequency
- 12V/ns slew rate
- ±3ns matched delay times
- Second harmonic is less than -40dB
- Two separate gate drive voltages
- 1.8V to 3.3V CMOS logic interface

Applications

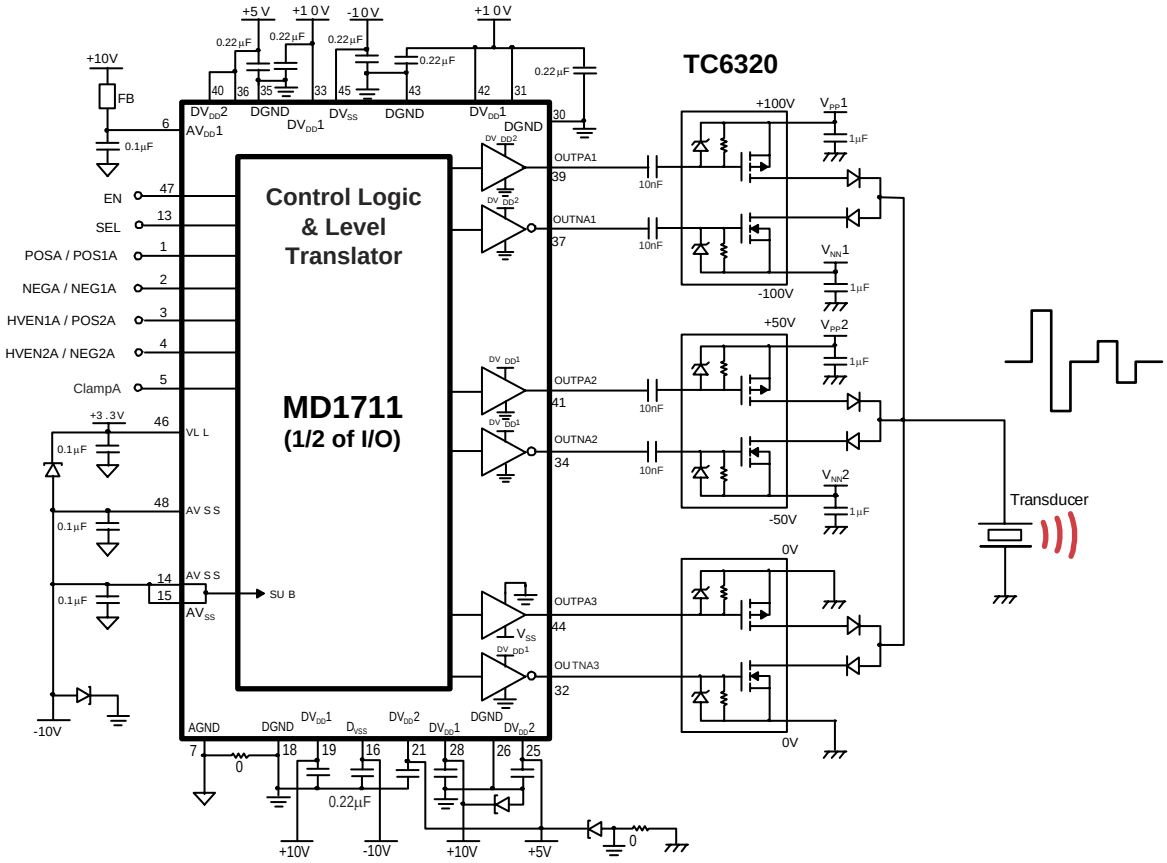
- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Metal flaw detection
- Nondestructive evaluation
- Sonar Transmitter

General Description

The Supertex MD1711 is an IC for a two-channel, 5-level, high voltage and high-speed transmitter driver. It is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, nondestructive evaluation, and driving piezoelectric transducers.

The MD1711 is a two-channel logic controller circuit with low impedance MOSFET gate drivers. There are two sets of control logic inputs, one for channel A and one for Channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of the Supertex TC6320. The MD1711 drives six TC6320s. Each pair an N-channel and a P-channel MOSFET. They are designed to have the same impedance and can provide peak currents of over 2.0 amps.

Typical Application Circuit (1 of 2 Channels)



Ordering Information

Package Option	Thermal Resistance
48-Lead LQFP/TQFP (1.4mm)	θ_{JA}
MD1711FG	50°C/W*
MD1711FG-G	

** 10z. 4-layer 3x4inch PCB*
-G indicates package is RoHS "Green" compliant

Absolute Maximum Ratings*

V_{LL}, Logic Supply	-0.5V to +5.5V
$AV_{DD}1$, $DV_{DD}1$, Positive Gate Drive Supply	-0.5V to +15V
$DV_{DD}2$, Positive Gate Drive Supply	-0.5V to +15V
AV_{SS}, DV_{SS} Negative Gate Drive Supply	-15V to +0.5V
Storage temperature	-65°C to 150°C
Junction temperature	125°C
Power Dissipation	1.2W

**Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

Operating Supply Voltages and Currents

(Over operating conditions unless otherwise specified, $AV_{DD}1 = DV_{DD}1 = DV_{DD}2 = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Note
V_{LL}	Logic Supply	+1.8	+3.3	+5.5	V	
$AV_{DD}1$	Positive Drive Bias Supply	+8.0	+10	+12.6	V	
$DV_{DD}1$	Positive Gate Drive Supply	+4.75		+12.6	V	
$DV_{DD}2$	Positive Gate Drive Supply	+4.75		+12.6	V	
AV_{SS}, DV_{SS}	Negative Gate Drive and Bias Supply	-12.0	-10	-8.0	V	
I_{VLL}	Logic Supply Current		2.0		mA	All channel on at 5.0Mhz, No load
I_{AVDD1}	Positive Bias Current		5.0		mA	
I_{AVSS} & I_{DVSS}	Negative Drive and Bias Supply Current		20		mA	
I_{DVDD1}	Positive Drive Current 1		55		mA	
I_{DVDD2}	Positive Drive Current 2		13		mA	$DV_{DD}2$ = 5.0V, All channel on at 5.0Mhz, No load
I_{AVDD1Q}	V_{AVDD1} quiescent current		2.0		mA	EN = low, All inputs low or high.
I_{AVSSQ}	V_{AVSS} quiescent current		0.75		mA	
I_{DVDD1Q}	V_{DVDD1} quiescent current			10	μA	
I_{DVDD2Q}	V_{DVDD2} quiescent current			10	μA	
I_{VLLQ}	Logic Supply Current		1.0		mA	

DC Electrical Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD}1 = DV_{DD}1 = DV_{DD}2 = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A =$ 0 to 70°C)

P-Channel Gate Driver Outputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance			6.0	Ω	I_{SINK} = 100mA
R_{SOURCE}	Output source resistance			6.0	Ω	I_{SOURCE} = 100mA
I_{SINK}	Peak output sink current		2.0		A	
I_{SOURCE}	Peak output source current		2.0		A	

N-Channel Gate Driver Outputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance			10	Ω	I_{SINK} = 100mA
R_{SOURCE}	Output source resistance			10	Ω	I_{SOURCE} = 100mA
I_{SINK}	Peak output sink current		1.5		A	
I_{SOURCE}	Peak output source current		1.5		A	

Logic Inputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	$0.8V_{LL}$		V_{LL}	V	
V_{IL}	Input logic low voltage	0		$0.2V_{LL}$	V	
I_{IH}	Input logic high current			1.0	µA	
I_{IL}	Input logic low current	-1.0			µA	

AC Electrical Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD}1 = DV_{DD}1 = DV_{DD}2 = 10V$, $AV_{SS} = DV_{SS} = -10V$, $V_{LL} = 3.3V$, $T_A =$ 0 to 70°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{OUT}	Output frequency range			20	MHz	
t_{PH}	Propagation delay when output is from low to high		19		ns	No load, See timing diagram
t_{PL}	Propagation delay when output is from high to low		19		ns	No load, See timing diagram
tr	Output rise time		8.0		ns	1000pF load, see timing diagram
tf	Output fall time		8.0		ns	1000pF load, see timing diagram
Δt_{dm}	Delay time matching			±3.0	ns	No load, From device to device
Δt_{DLAY}	Output jitter		30		ps	Standard deviation of t_d samples (1k)
SR	Output slew rate		12		V/ns	Measured at TC6320 output with 100Ω Load
HD2	2^{nd} harmonic distortion		-40		dB	

Power-Up Sequence

1	AV_{SS} , DV_{SS}	Negative Gate Drive Supply and Substrate Bias
2	V_{LL}, $AV_{DD}1$, $DV_{DD}1$ & $DV_{DD}2$	Logic Supply, Positive Gate Drive Supply and Bias

Truth Table for Channels A and B (For SEL = L)

Logic Control Inputs							$V_{PP}1$ to $V_{NN}1$ Output		$V_{PP}2$ to $V_{NN}2$ Output		$V_{PP}3$ to $V_{NN}3$ Output	
SEL	**EN**	**HVEN1/ POS2**	**HVEN2/ NEG2**	**Clamp**	**POS/ POS1**	**NEG/ NEG1**	**$HV_{OUT}P1$**	**$HV_{OUT}N1$**	**$HV_{OUT}P2$**	**HV_{OUT} N2**	**HV_{OUT} P3**	**$HV_{OUT}N3$**
0	1	0	0	0	0	0	OFF		OFF		ON	ON
0	1	0	0	0	0	1					ON	ON
0	1	0	0	0	1	0					ON	ON
0	1	0	0	0	1	1					OFF	OFF
0	1	0	0	1	0	0	OFF		OFF		OFF	
0	1	0	0	1	0	1						
0	1	0	0	1	1	0						
0	1	0	0	1	1	1						
0	1	0	1	0	0	0	OFF		OFF	OFF	ON	ON
0	1	0	1	0	0	1			OFF	ON	OFF	OFF
0	1	0	1	0	1	0			ON	OFF	OFF	OFF
0	1	0	1	0	1	1			OFF	OFF	OFF	OFF
0	1	0	1	1	0	0	OFF		OFF		OFF	
0	1	0	1	1	0	1						
0	1	0	1	1	1	0						
0	1	0	1	1	1	1						
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0	1	1	0	0	1	0	ON	OFF			OFF	OFF
0	1	1	0	0	1	1	OFF	OFF			OFF	OFF
0	1	1	0	1	0	0	OFF		OFF		OFF	
0	1	1	0	1	0	1						
0	1	1	0	1	1	0						
0	1	1	0	1	1	1						
0	1	1	1	0	0	0	OFF		OFF		OFF	
0	1	1	1	0	0	1						
0	1	1	1	0	1	0						
0	1	1	1	0	1	1						
0	1	1	1	1	0	0	OFF		OFF		OFF	
0	1	1	1	1	0	1						
0	1	1	1	1	1	0						
0	1	1	1	1	1	1						
0	0	X	X	X	X	X	OFF		OFF		OFF	

Truth Table for Channels A and B (For SEL = H)

Logic Control Inputs							$V_{PP}1$ to $V_{NN}1$ Output		$V_{PP}2$ to $V_{NN}2$ Output		$V_{PP}3$ to $V_{NN}3$ Output	
SEL	EN	Clamp	HVEN1/ POS2	HVEN2/ NEG2	POS/ POS1	NEG/ NEG1	$HV_{OUT}P1$	$HV_{OUT}N1$	$HV_{OUT}P2$	$HV_{OUT}N2$	$HV_{OUT}P3$	$HV_{OUT}N3$
1	1	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	
1	1	0	0	0	0	1	OFF	ON				
1	1	0	0	0	1	0	ON	OFF				
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1	1	0	0	1	1	0	ON	OFF				
1	1	0	0	1	1	1	ON	ON				
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1	1	0	1	0	1	0	ON	OFF				
1	1	0	1	0	1	1	ON	ON				
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1	1	1	0	0	1	0	ON	OFF				
1	1	1	0	0	1	1	ON	ON				
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1	1	1	0	1	0	1	OFF	ON				
1	1	1	0	1	1	0	ON	OFF				
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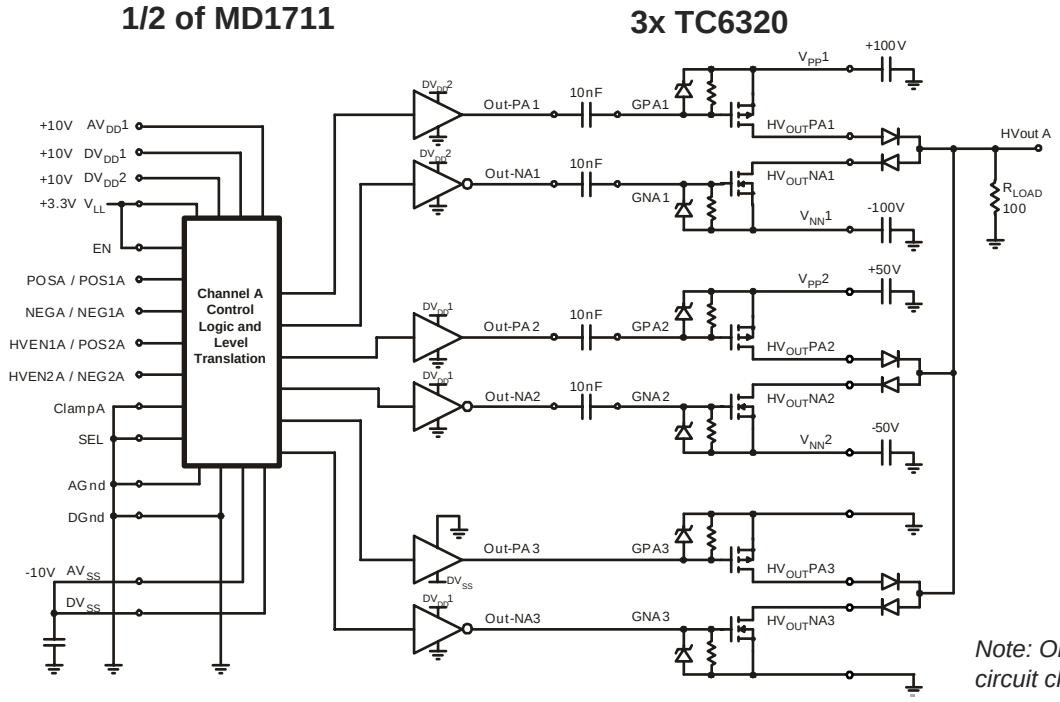
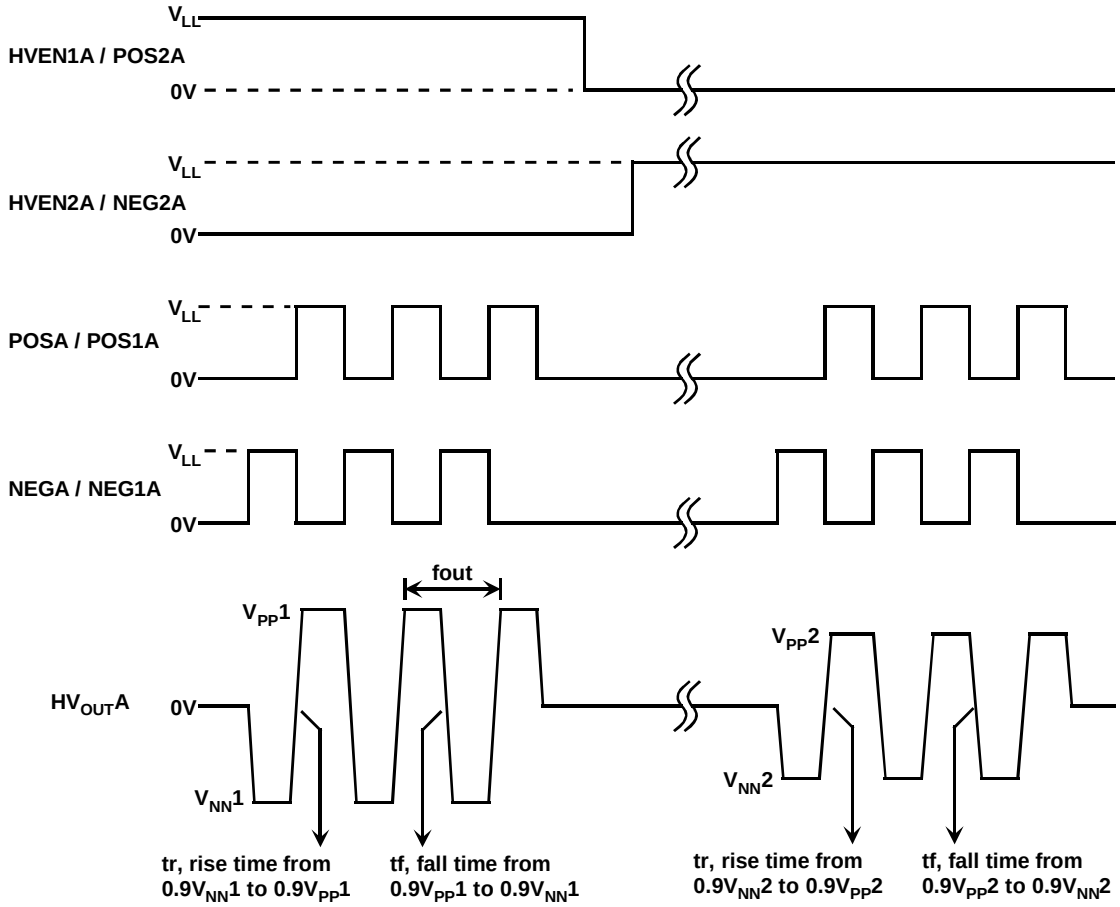
1	1	1	1	0	1	0	ON	OFF				
1	1	1	1	0	1	1	ON	ON				
1	1	1	1	1	0	0	OFF	OFF	ON	ON	ON	
1	1	1	1	1	0	1	OFF	ON				
1	1	1	1	1	1	0	ON	OFF				
1	1	1	1	1	1	1	ON	ON				
1	0	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	

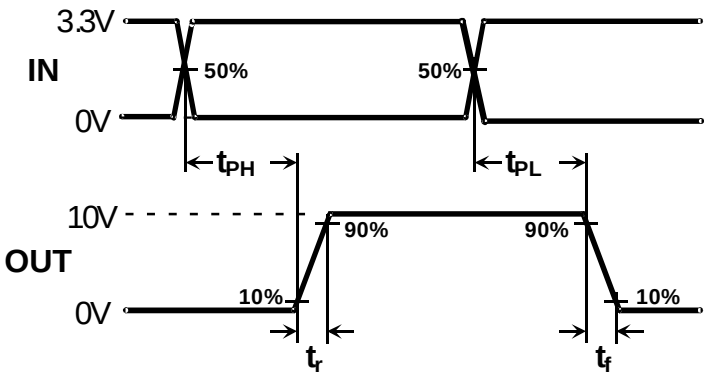
Test Circuit for Channel A



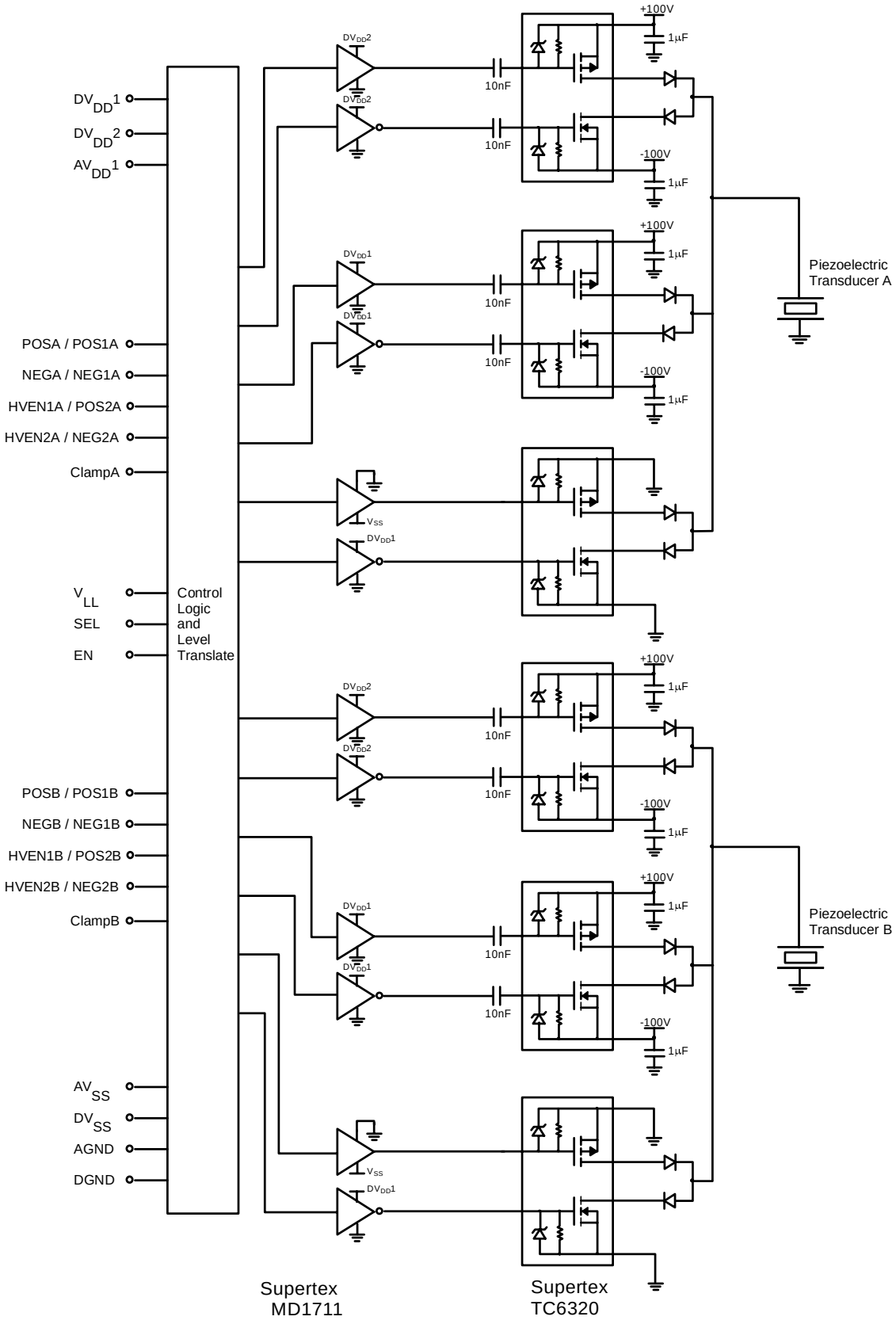
Note: Only one of the two circuit channels is shown.

Timing Diagram (EN = H, SEL = ClampA = L)





Block Diagram / Typical Application Circuit



MD1711: Pin Description

V_{LL}	Logic supply voltage.
$AV_{DD}1$	Supplies analog circuitry portion of the gate driver. Should be at the same potential as $DV_{DD}1$.
$DV_{DD}1$	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for Out-PA2, Out-NA2, Out-NA3, Out-PB2, Out-NB2, and Out-NB3. Should be at the same potential as $AV_{DD}1$.
$DV_{DD}2$	Gate drive supply voltage. Supplies digital circuitry portion of the gate driver and the main output stage for Out-PA1, Out-NA1, Out-PB1, and Out-NB1. Can be at a different potential than $DV_{DD}1$.
DV_{SS}	Gate drive supply voltage for Out-PA3 and Out-PB3. Supplies digital circuitry portion and the main output stage. Should be at the same potential as AV_{SS}.
AV_{SS}	Negative driver supply for Out-PA3, Out-PB3 and bias circuits. They are also connected to the IC substrate. They are required to connect to the most negative potential of voltage supplies.
DGND	Digital Ground.
AGND	Analog Ground.
POSA / POS1A	Logic input control for channel A. When SEL = L, the pin is POSA. When SEL = H, the pin is POS1A.
NEGA / NEG1A	Logic input control for channel A. When SEL = L, the pin is NEGA. When SEL = H, the pin is NEG1A.
HVEN1A / POS2A	Logic input control for channel A. When SE L= L, the pin is HVEN1A. When SEL = H, the pin is POS2A.
HVEN2A / NEG2A	Logic input control for channel A. When SEL = L, the pin is HVEN2A. When SEL = H, the pin is NEG2A.
CLAMPA	Used with SEL = H. Logic input control for Out-PA3 and Out-NA3. Connect to ground when SEL = L.
Out-PA1, Out-PA2, Out-PA3	Output P-Channel gate drivers for channel A
Out-NA1, Out-NA2, Out-NA3	Output N-Channel gate drivers for channel A
POSB / POS1B	Logic input control for channel B. When SEL = L, the pin is POSB. When SEL = H, the pin is POS1B.
NEGB / NEG1B	Logic input control for channel B. When SEL = L, the pin is NEGB. When SEL = H, the pin is NEG1B.
HVEN1B / POS2B	Logic input control for channel B. When SEL = L, the pin is HVEN1B. When SEL = H, the pin is POS2B.
HVEN2B / NEG2B	Logic input control for channel B. When SEL = L, the pin is HVEN2B. When SEL = H, the pin is NEG2B.
CLAMPB	Used with SEL = H. Logic input control for Out-PB3 and Out-NB3. Connect to ground when SEL = L.
SEL	Logic input select. See truth tables for SEL = L and SEL = H.
EN	Logic input enable control. When EN = L, all P-channel output drivers are high and all N-channel output drivers are low.
Out-PB1, Out-PB2, Out-PB3	Output P-Channel gate driver for channel B
Out-NB1, Out-NB2, Out-NB3	Output N-Channel gate driver for channel B

Pin Configuration
48-Lead LQFP/TQFP (1.4mm)

Pin	Function	Pin	Function
1	POSA/POS1A	25	$DV_{DD}2$
2	NEGA/NEG1A	26	DGND
3	HVEN1A/POS2A	27	Out-NB2
4	HVEN2A/NEG2A	28	$DV_{DD}1$
5	CLAMPA	29	Out-NB3
6	$AV_{DD}1$	30	DGND
7	AGND	31	$DV_{DD}1$
8	CLAMPB	32	Out-NA3
9	HVEN2B/NEG2B	33	$DV_{DD}1$
10	HVEN1B/POS2B	34	Out-NA2
11	NEGB/NEG1B	35	DGND
12	POSB/POS1B	36	$DV_{DD}2$
13	SEL	37	Out-NA1
14	AV_{SS}	38	N/C
15	AV_{SS}	39	Out-PA1
16	DV_{SS}	40	$DV_{DD}2$
17	Out-PB3	41	Out-PA2
18	DGND	42	$DV_{DD}1$
19	$DV_{DD}1$	43	DGND
20	Out-PB2	44	Out-PA3
21	$DV_{DD}2$	45	DV_{SS}
22	Out-PB1	46	V_{LL}
23	N/C	47	EN
24	Out-NB1	48	AV_{SS}

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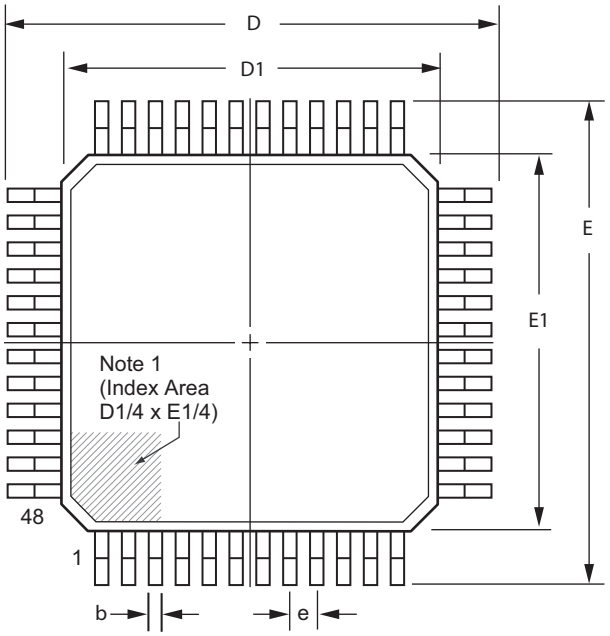
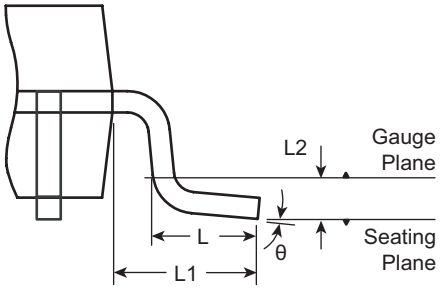
Doc. # DSFP-MD1711
A062806

48-Lead LQFP/TQFP Package Outline (FG)

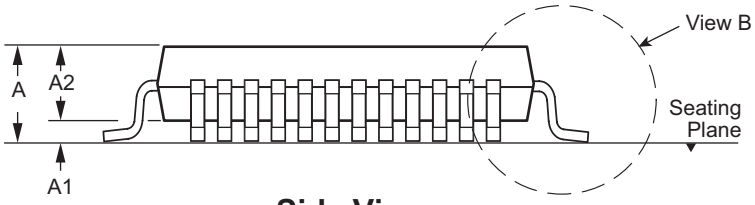
7x7x1.4mm body, 0.50mm pitch



Top View



View B



Side View

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40	0.05	1.35	0.17	8.80	6.80	8.80	6.80	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20	7.20	9.20	7.20		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

Drawings not to scale.

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