

IR2157

FULLY INTEGRATED BALLAST CONTROL IC

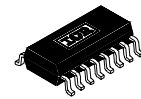
Features

- Programmable preheat time & frequency
- Programmable ignition ramp
- Protection from failure-to-strike
- Lamp filament sensing & protection
- Protection from operation below resonance
- Protection from low-line condition & automatic restart (mimics a magnetic ballast)
- Thermal overload protection
- Programmable deadtime
- Integrated 600V level-shifting gate driver
- Internal 15.6V zener clamp diode on VCC
- True micropower startup (150uA)
- Latch immunity protection on all leads
- ESD protection on all leads

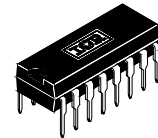
Description

The IR2157 is a fully integrated, fully protected 600V ballast control IC designed to drive virtually all types of rapid start fluorescent lamp ballasts. Externally programmable features such as preheat time & frequency, ignition ramp characteristics, and running mode operating frequency provide a high degree of flexibility for the ballast design engineer. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, low dc bus conditions, thermal overload, or lamp failure during normal operation, as well as an automatic restart function, have been included in the design. The heart of this control IC is a variable frequency oscillator with externally programmable deadtime. Precise control of a 50% duty cycle is accomplished using a T-flip-flop. The IR2157 is available in both 16 pin DIP and 16 pin narrow body SOIC packages.

Packages

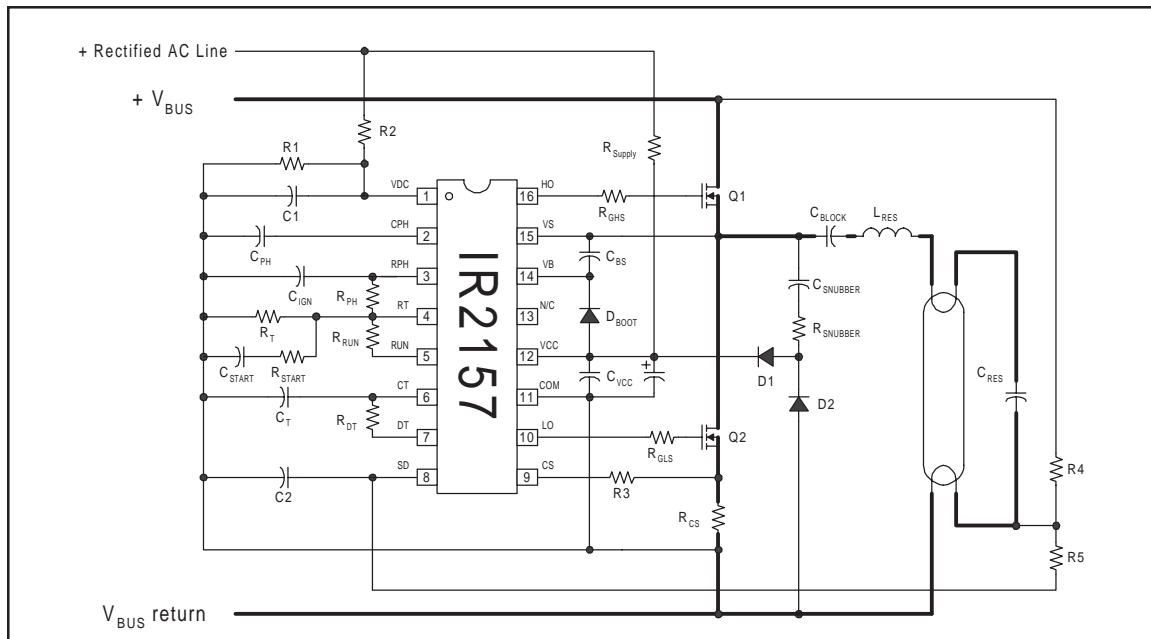


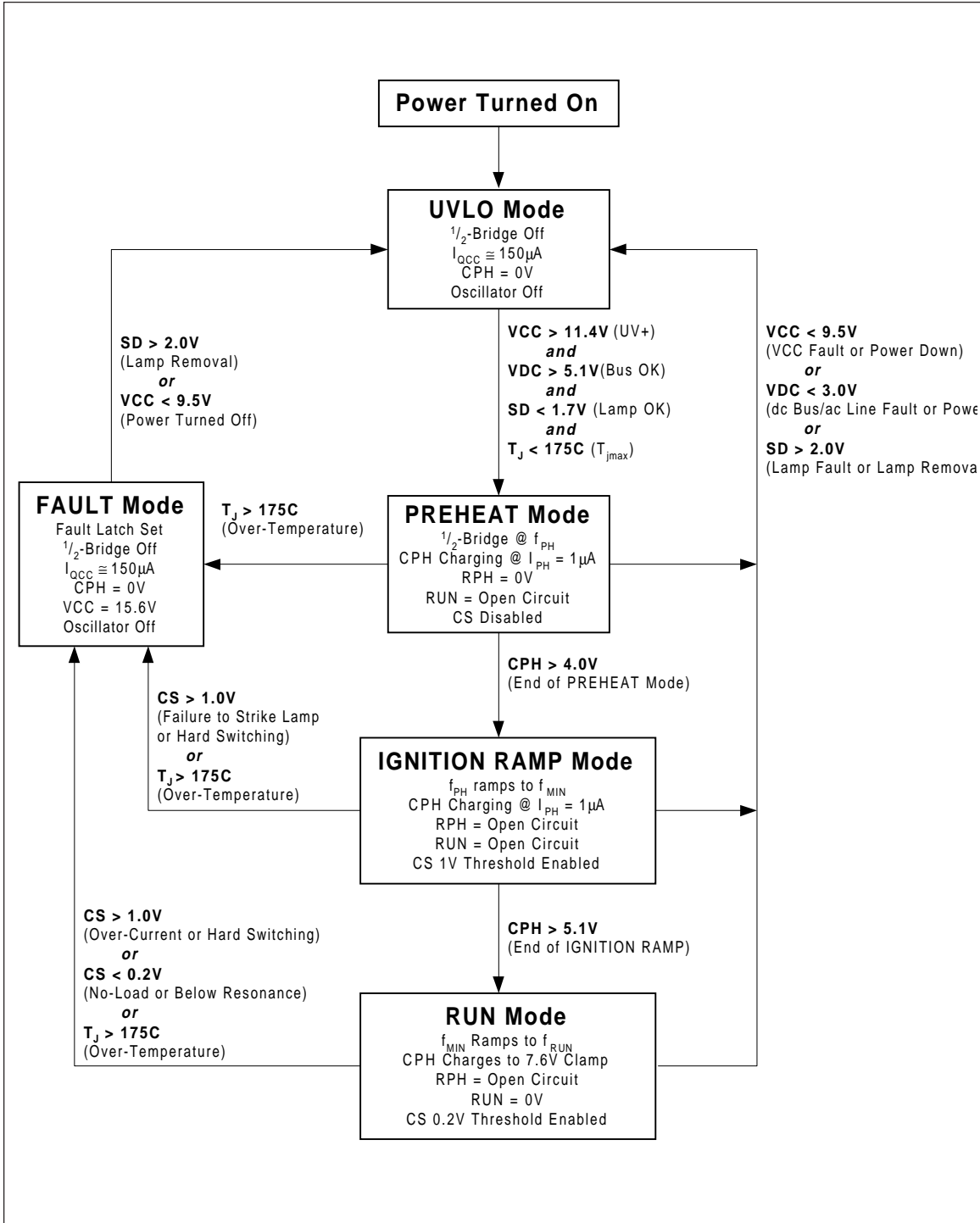
16 Lead SOIC
(narrow body)



16 Lead PDIP

Typical Connection





Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|-------------------|---|----------------------|-----------------------|-------|------|
| V _B | High side floating supply voltage | -0.3 | 625 | V | |
| V _S | High side floating supply offset voltage | V _B - 25 | V _B + 0.3 | | |
| V _{HO} | High side floating output voltage | V _S - 0.3 | V _B + 0.3 | | |
| V _{LO} | Low side output voltage | -0.3 | V _{CC} + 0.3 | | |
| I _{OMAX} | Maximum allowable output current due to miller effect | -500 | 500 | mA | |
| I _{RT} | R _T pin current | -5 | 5 | | |
| V _{CT} | C _T pin voltage | -0.3 | V _{CC} + 0.3 | V | |
| I _{CPH} | CPH pin current | -5 | 5 | mA | |
| V _{RPH} | RPH pin voltage | -0.3 | V _{CC} + 0.3 | V | |
| V _{RUN} | RUN pin voltage | -0.3 | V _{CC} + 0.3 | | |
| V _{DT} | Deadtime pin voltage | -0.3 | 5.5 | | |
| V _{CS} | Current sense pin voltage | -0.3 | 5.5 | | |
| V _{SD} | Shutdown pin voltage | -0.3 | 5.5 | | |
| I _{CC} | Supply current (note 1) | — | 20 | | mA |
| dV/dt | Allowable offset voltage slew rate | -50 | 50 | V/ns | |
| P _D | Package power dissipation @ T _A ≤ +25°C | (16 lead PDIP) | — | 1.60 | |
| | | (16 lead SOIC) | — | 1.25 | |
| R _{thJA} | Thermal resistance, junction to ambient | (16 lead PDIP) | — | 75 | °C/W |
| | | (16 lead SOIC) | — | 100 | |
| T _J | Junction temperature | -55 | 150 | | |
| T _S | Storage temperature | -55 | 150 | °C | |
| T _L | Lead temperature (soldering, 10 seconds) | — | 300 | | |

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

| Symbol | Definition | Min. | Max. | Units |
|------------------|---|-----------------------|--------------------|-------|
| V _{BS} | High side floating supply voltage | V _{CC} - 0.7 | V _{CLAMP} | V |
| V _S | Steady state high side floating supply offset voltage | -3.0 | 600 | |
| V _{CC} | Supply voltage | V _{CCUV+} | V _{CLAMP} | |
| I _{CC} | Supply current | note 2 | 10 | mA |
| V _{DC} | V _{DC} lead voltage | 0 | V _{CC} | V |
| C _T | C _T lead capacitance | 220 | — | pF |
| R _{DT} | Deadtime resistance | 1.0 | — | kΩ |
| I _{RT} | R _T lead current (note 3) | -500 | -50 | uA |
| I _{RPH} | RPH lead current (note 3) | 0 | 450 | uA |
| I _{RUN} | RUN lead current (note 3) | 0 | 450 | uA |
| I _{SD} | Shutdown lead current | -1 | 1 | mA |
| I _{CS} | Current sense lead current | -1 | 1 | mA |
| T _J | Junction temperature | -40 | 125 | °C |

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS} = 15V +/- 0.25V, R_T = 40.0kΩ, C_T = 470 pF, RPH and RUN leads no connection, V_{CPH} = 0.0V, R_{DT} = 6.1kΩ, V_{CS} = 0.5V, V_{SD} = 0.0V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

| Supply Characteristics | | | | | | |
|------------------------|--|------|------|------|-------|--|
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| V _{CCUV+} | V _{CC} supply undervoltage positive going threshold | — | 11.4 | — | V | V _{CC} rising from 0V |
| V _{CCUV-} | V _{CC} supply undervoltage positive going threshold | — | 9.6 | — | | V _{CC} falling from 15V |
| V _{HYSTUV} | V _{CC} supply undervoltage lockout hysteresis | — | 1.8 | — | | |
| I _{QCCUV} | UVLO mode quiescent current | — | 150 | — | μA | V _{CC} = 10V rising |
| I _{QCCFLT} | Fault-mode quiescent current (undervoltage lockout, shutdown, over-current, over-temp) | — | 200 | — | | |
| I _{QCC} | Quiescent V _{CC} supply current | — | 3.8 | — | mA | R _T no connection, C _T connected to COM |
| I _{QCC50K} | V _{CC} supply current, f= 50kHz | — | 4.5 | — | | R _T =36kΩ, R _{DT} = 5.6kΩ, C _T =220pF |
| V _{CLAMP} | V _{CC} zener clamp voltage | — | 15.6 | — | V | I _{CC} = 10mA |

Note 2: Enough current should be supplied into the V_{CC} lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage.

Note 3: Due to the fact that the RT input is a voltage-controlled current source, the total RT pin current is sum of all of the parallel current sources connected to that pin. For optimum oscillator current mirror performance, this total current should be kept between 50mA and 500mA. During the preheat mode, the total current flowing out of the RT pin consists of the RPH pin current plus the current due to the RT resistor. During the run mode, the total RT pin current consists of the RUN pin current plus the the current due to the RT resistor.

Electrical Characteristics (cont.)

| Floating Supply Characteristics | | | | | | |
|---------------------------------|--|------|------|------|-------|---|
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| I _{QBS0} | Quiescent V _{BS} supply current | — | 0 | — | μA | V _{HO} = V _S |
| I _{QBS1} | Quiescent V _{BS} supply current | — | 30 | — | | V _{HO} = V _B |
| V _{BSMIN} | Minimum required VBS voltage for proper HO functionality | — | 4 | 5 | V | |
| I _{LK} | Offset supply leakage current | — | — | 50 | μA | V _B = V _S = 600V |
| Oscillator I/O Characteristics | | | | | | |
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| f _{osc} | Oscillator frequency | — | 30 | — | kHz | R _T = 32kΩ, R _{DT} = 6.1kΩ, C _T = 470pF |
| | | — | 100 | — | | R _T = 6.1kΩ, R _{DT} = 6.1kΩ, C _T = 470pF |
| df/dV | Oscillator frequency voltage stability | — | 0.5 | — | %/V | V _{CCUV+} < V _{CC} < 15V |
| df/dT | Oscillator frequency temperature stability | — | 0.02 | — | %/C | -40°C < T _J < 125°C |
| d | Oscillator duty cycle | — | 50 | — | % | |
| V _{CT+} | Upper C _T ramp voltage threshold | — | 4.0 | — | V | |
| V _{CT-} | Lower C _T ramp voltage threshold | — | 2.0 | — | V | |
| V _{CTFLT} | Fault-mode C _T pin voltage | — | 0 | — | mV | SD = 5V, CS = 2V, or T _J > TSD |
| V _{RT} | R _T pin voltage | — | 2.0 | — | V | |
| V _{RTFLT} | Fault-mode R _T pin voltage | — | 0 | — | mV | SD = 5V, CS = 2V, or T _J > TSD |
| td _{lo} | LO output deadtime | — | 2.0 | — | μsec | |
| to _{ho} | HO output deadtime | — | 2.0 | — | μsec | |
| dtd/dV | Deadtime voltage stability | — | 0.5 | — | %/V | V _{CCUV+} < V _{CC} < 15V |
| dtd/dT | Deadtime temperature stability | — | 0.02 | — | %/C | -40°C < T _J < 125°C |
| Preheat Characteristics | | | | | | |
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| I _{CPH} | CPH pin charging current | — | 1.0 | — | μA | V _{CPH} = 0V |
| V _{CPHIGN} | CPH pin Ignition mode threshold voltage | — | 4.0 | — | V | |
| V _{CPHRUN} | CPH pin run mode threshold voltage | — | 5.15 | — | | |
| V _{CPHCLMP} | CPH pin clamp voltage | — | 7.6 | — | V | I _{CPH} = 1mA |
| V _{CPHFLT} | Fault-mode CPH pin voltage | — | 0 | — | mV | SD = 5V, CS = 2V, or T _J > TSD |

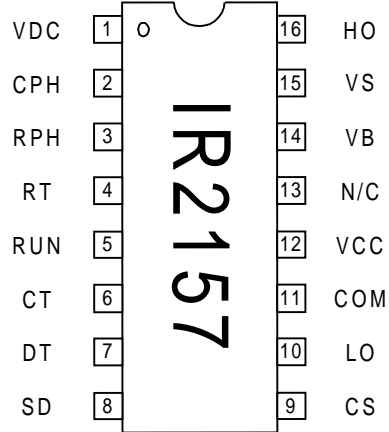
Electrical Characteristics (cont.)

| RPH Characteristics | | | | | | |
|--------------------------------------|---|------|------|------|--------------------|---|
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| I_{RPHLK} | Open circuit RPH pin leakage current | — | 0.1 | — | μA | $V_{RPH} = 5\text{V}, V_{RPHFLT} = 5\text{V}$ $SD = 5\text{V}, CS = 2\text{V},$ or $T_j > T_{SD}$ |
| V_{RPHFLT} | Fault-mode RPH pin voltage | — | 0 | — | mV | |
| RUN Characteristics | | | | | | |
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| I_{RUNLK} | Open circuit RUN pin leakage current | — | 0.1 | — | μA | $V_{RUN} = 5\text{V}$ |
| V_{RUNFLT} | Fault-mode RUN pin voltage | — | 0 | — | mV | $SD = 5\text{V}, CS = 2\text{V},$ or $T_j > T_{SD}$ |
| Protection Circuitry Characteristics | | | | | | |
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| V_{SDTH+} | Rising shutdown pin threshold voltage | — | 2.0 | — | V | |
| V_{SDHYS} | Shutdown pin threshold hysteresis | — | 150 | — | mV | |
| V_{CSTH+} | Over-current sense threshold voltage | — | 1.0 | — | V | |
| V_{CSTH-} | Under-current sense threshold voltage | — | 0.2 | — | | |
| T_{CS} | Over-current sense propagation delay | — | 160 | — | nsec | Delay from CS to LO or HO |
| V_{DC+} | Low V_{BUS} /rectified line input upper threshold | — | 5.15 | — | V | |
| V_{DC-} | Low V_{BUS} /rectified line input lower threshold | — | 3.0 | — | | |
| T_{SD} | Thermal shutdown junction temperature | — | 175 | — | $^{\circ}\text{C}$ | |
| Gate Driver Output Characteristics | | | | | | |
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| V_{OL} | Low-level output voltage | — | 0 | 100 | mV | $I_o = 0$ |
| V_{OH} | High level output voltage | — | 0 | 100 | | $V_{BIAS} - V_O, I_o = 0$ |
| t_r | Turn-on rise time | — | 85 | 150 | nsec | |
| t_f | Turn-off fall time | — | 45 | 100 | | |

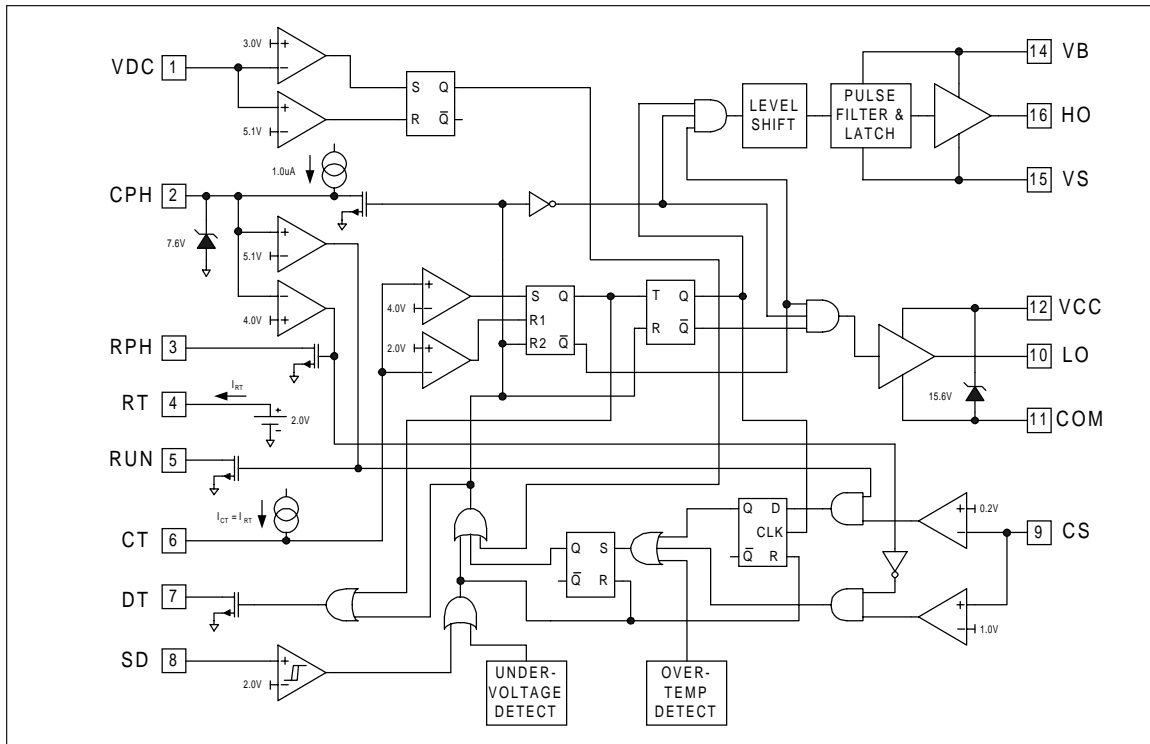
Note 4: When the IC senses an overtemperature condition ($T_j > 175^{\circ}\text{C}$), the IC is latched off. In order to reset this Fault Latch, the SD pin must be cycled high and then low, or the VCC supply to the IC must be cycled below the falling undervoltage lockout threshold (V_{CCUV-}).

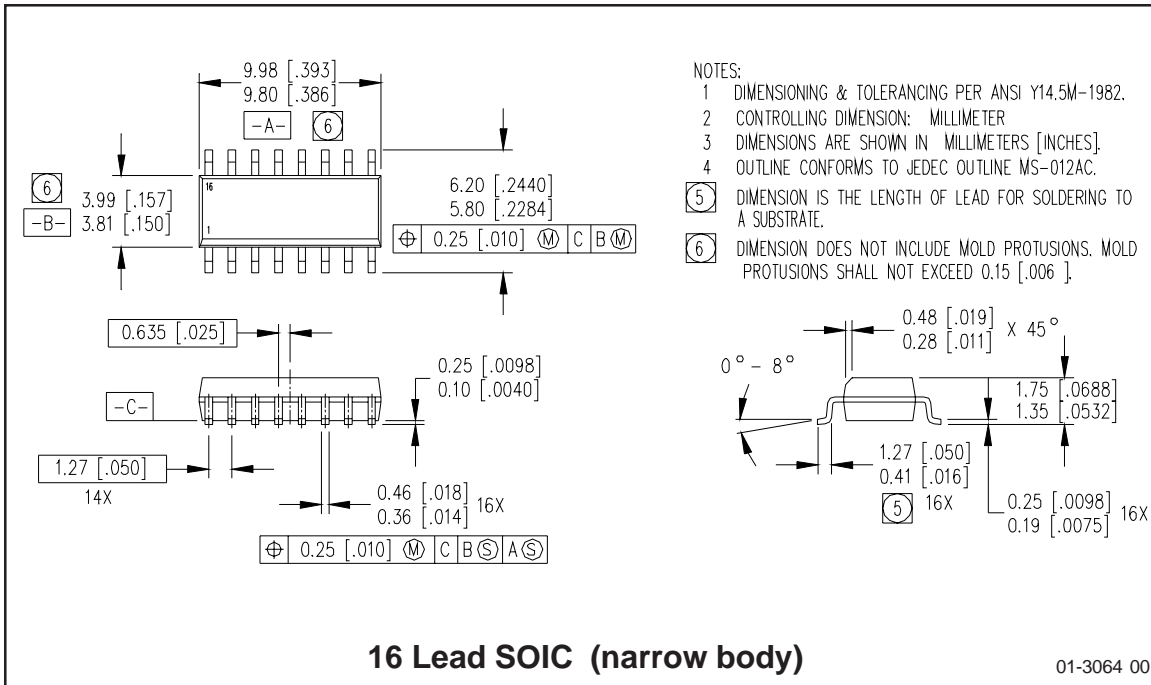
Lead Assignments & Definitions

| Lead # | Symbol | Description |
|--------|-----------------|---|
| 1 | V _{DC} | DC bus sensing input |
| 2 | C _{PH} | Preheat timing capacitor |
| 3 | R _{PH} | Preheat frequency resistor & ignition capacitor |
| 4 | R _T | Oscillator timing resistor |
| 5 | R _{UN} | Run frequency resistor |
| 6 | C _T | Oscillator timing capacitor |
| 7 | D _T | Deadtime programming |
| 8 | SD | Shutdown input |
| 9 | CS | Current sensing input |
| 10 | LO | Low-side gate driver output |
| 11 | COM | IC Power & signal ground |
| 12 | V _{CC} | Logic & low-side gate driver supply |
| 13 | N/C | Unused |
| 14 | V _B | High-side gate driver floating supply |
| 15 | V _S | High voltage floating return |
| 16 | HO | High-side gate driver output |

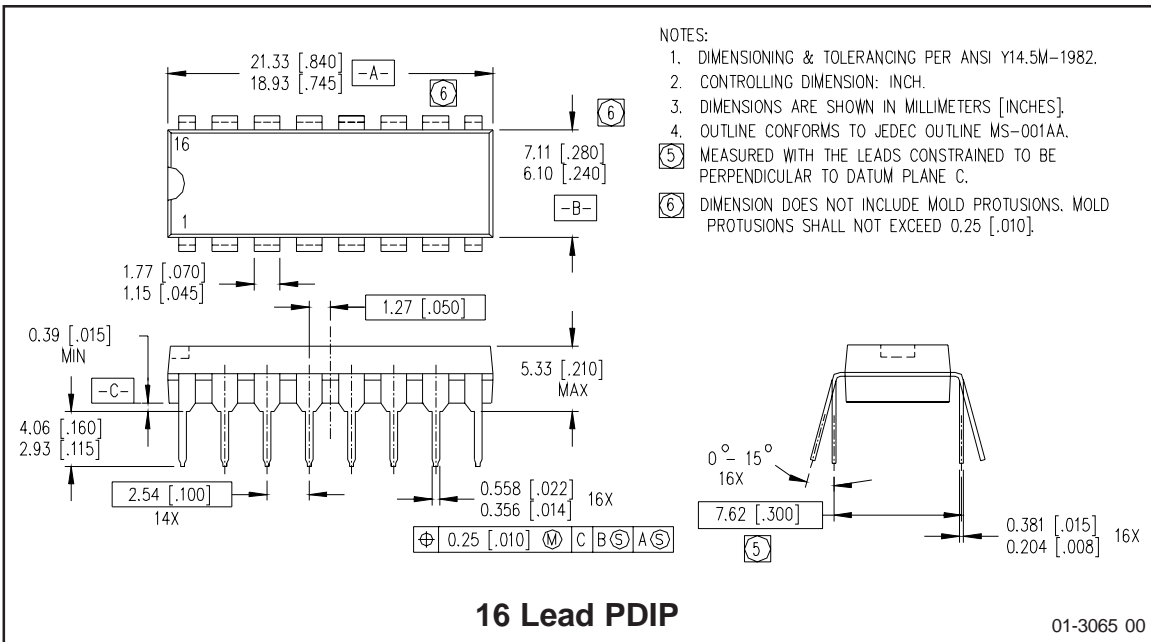


Functional Block Diagram





- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 - 2 CONTROLLING DIMENSION: MILLIMETER
 - 3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 - 4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.
 - 5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
 - 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

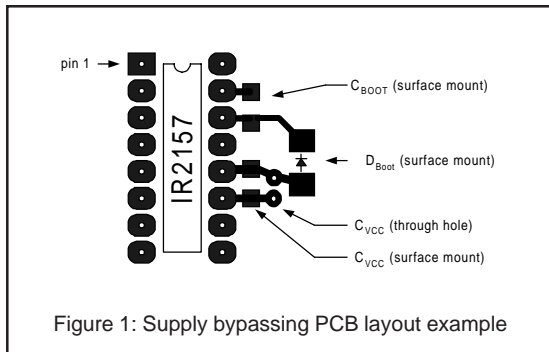


- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
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 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
 - 5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
 - 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

Description of Operation & Component Selection Tips

Supply Bypassing and PC Board Layout Rules

Component selection and placement on the pc board is extremely important when using power control ICs VCC should be bypassed to COM as close to the IC terminals as possible with a low ESR/ESL capacitor, as shown in Figure 1 below.

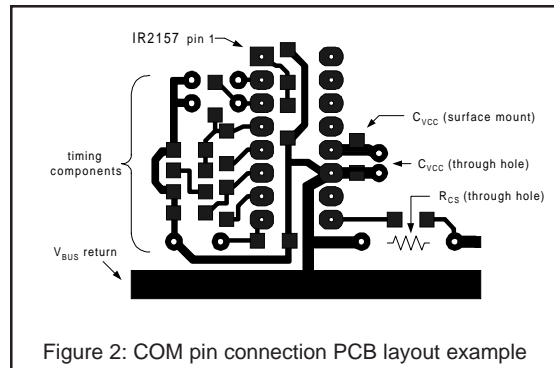


A rule of thumb for the value of this bypass capacitor is to keep its minimum value at least 2500 times the value of the total input capacitance (C_{iss}) of the power transistors being driven. This decoupling capacitor can be split between a higher valued electrolytic type and a lower valued ceramic type connected in parallel, although a good quality electrolytic (e.g., 10mF) placed immediately adjacent to the VCC and COM terminals will work well.

In a typical application circuit, the supply voltage to the IC is normally derived by means of a high value startup resistor (1/4W) from the rectified line voltage, in combination with a charge pump from the output of the half-bridge. With this type of supply arrangement, the internal 15.6V zener clamp diode from VCC to COM will determine the steady state IC supply voltage.

Connecting the IC Ground (COM) to the Power Ground

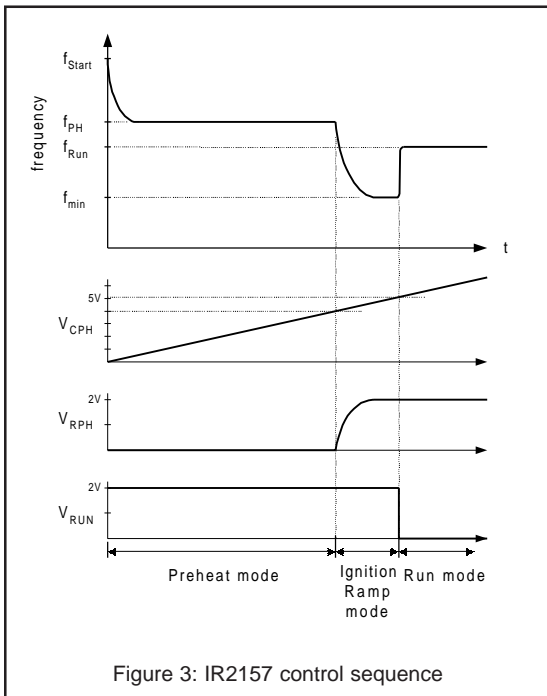
Both the low power control circuitry and low side gate driver output stage grounds return to this pin within the IC. The COM pin should be connected to the bottom terminal of the current sense resistor in the source of the low side power MOSFET using an individual pc board trace, as shown in Figure 2. In addition, the ground return path of the timing components and VCC decoupling capacitor should be connected directly to the IC COM pin, and not via separate traces or jumpers to other ground traces on the board.



These connection technique prevents high current ground loops from interfering with sensitive timing component operation, and allows the entire control circuit to reject common-mode noise due to output switching.

The Control Sequence & Timing Component Selection

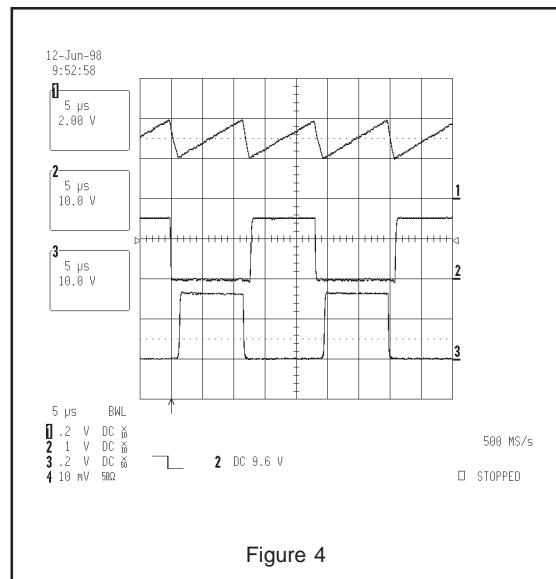
The IR2157 uses the following control sequence (Figure 3) to drive rapid start fluorescent lamps.



The control sequence used in the IR2157 allows the Run Mode operating frequency of the ballast to be higher than the ignition frequency (i.e., $f_{start} > f_{ph} > f_{run} > f_{ign}$). This control sequence is recommended for lamp types where the ignition frequency is too close to the run frequency to ensure proper lamp striking for all production resonant LC component tolerances (please note that it is possible to use the IR2157 in systems where $f_{start} > f_{ph} > f_{run}$, simply by leaving the RUN pin open).

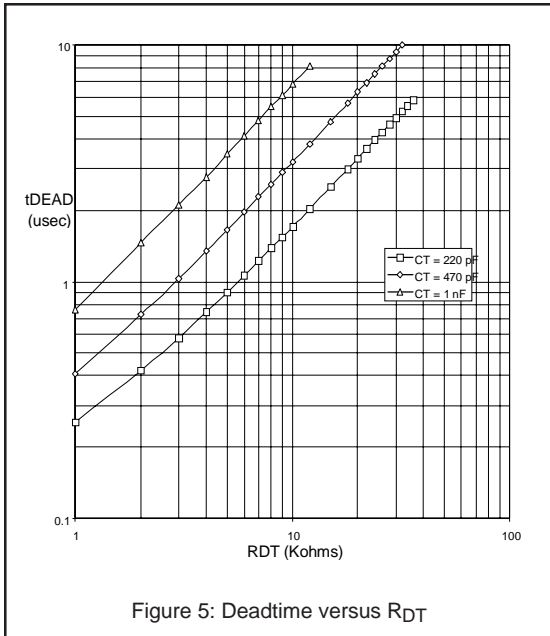
Six pins in the IC are used to control the **Startup**, **Preheat**, **Ignition Ramp**, and **Run** modes of operation, and to allow ballast and lamp engineers the flexibility to optimize their designs for virtually any lamp type.

The heart of this controller is an oscillator which resembles those found in many popular PWM voltage regulator ICs. In its simplest form, this oscillator consists of a timing resistor and capacitor connected to ground. The voltage across the timing capacitor CT is a sawtooth, where the rising portion of the ramp is determined by the current in the RT pin, and the falling portion of the ramp is determined by an external deadtime resistor RDT. The oscillograph in Figure 4 illustrates the relationship between the oscillator capacitor waveform and the gate driver outputs.



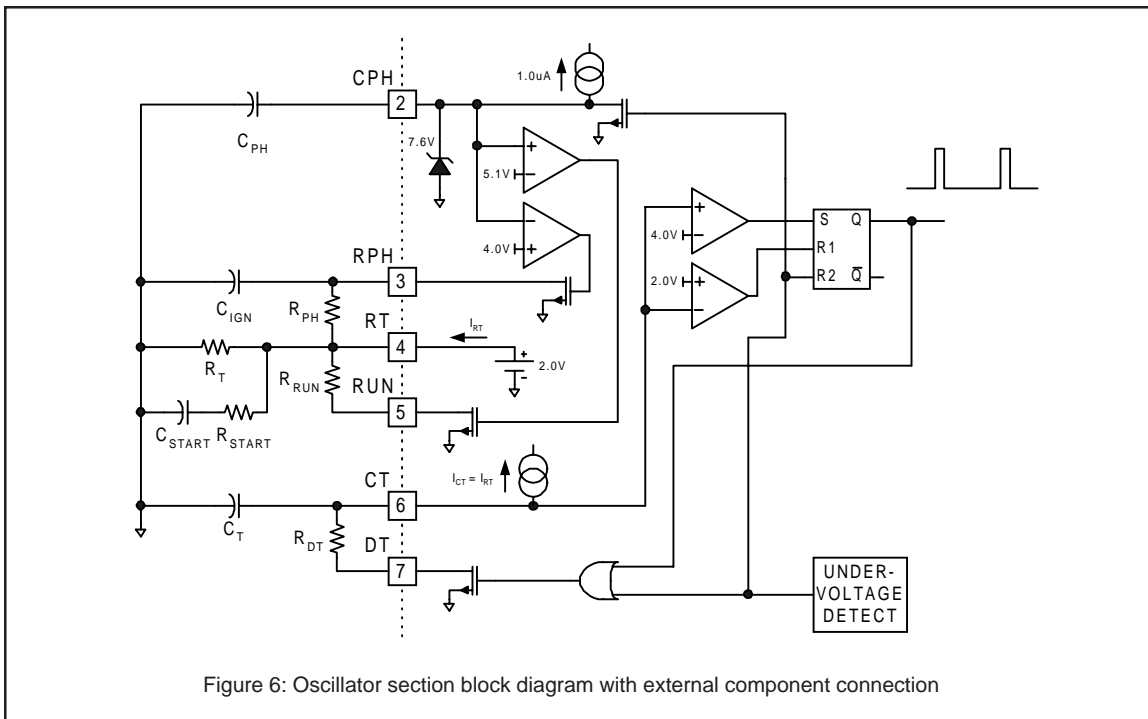
The deadtime can be programmed by means of the external RDT resistor, given a certain range of CT capacitor values, using the graph shown in Figure 5.

The RT input is a voltage-controlled current source, where the voltage is regulated to be approximately 2.0V. In order to maintain proper linearity between the RT pin current and the CT capacitor charging current, the value of the RT pin current should be kept between $50\mu A$ and $500\mu A$. The RT pin can also be used as a feedback point for closed loop control.



During the **Startup Mode**, the operating frequency is determined by the parallel combination of R_{PH} , R_{START} , and R_T , combined with the values of C_{START} , C_T and R_{DT} , as shown in Figure 6. This frequency is normally chosen to ensure that the instantaneous voltage across the lamp during the first few cycles of operation does not exceed the strike potential of the lamp. As the voltage across C_{START} charges up to the R_T pin voltage, the output frequency exponentially decays to the preheat frequency.

During the Preheat Mode, the operating frequency is determined by the parallel combination of R_{PH} and R_T , combined with the value of C_T and R_{DT} . This frequency, along with the Preheat Time, is normally chosen to ensure that adequate heating of the lamp filaments occurs. Typically, a 4.5:1 ratio of



the hot filament-to-cold filament resistance is desired for maximum lamp life, as shown in Figure 7

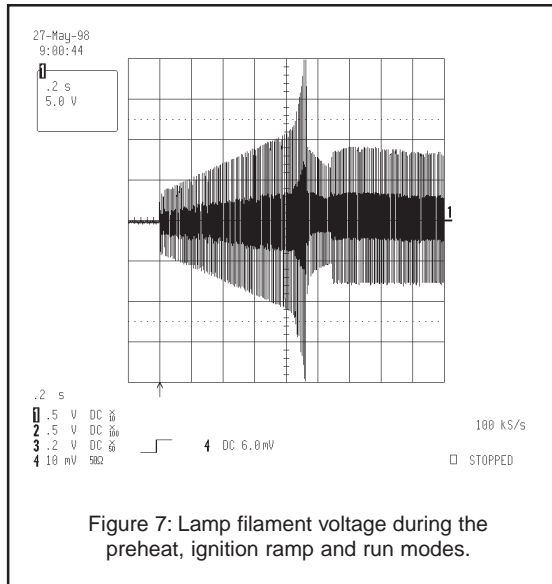


Figure 7: Lamp filament voltage during the preheat, ignition ramp and run modes.

The Preheat Time is programmed by means of the preheat capacitor, C_{PH}, an internal 1mA current source, and an internal threshold on the CPH pin of 4.0V, according to the following formula:

$$t_{PH} = 4E6 \cdot C_{PH}, \quad \text{OR}$$

$$C_{PH} = 250E-9 \cdot t_{PH}$$

At the end of the Preheat Time, the internal, open-drain transistor holding the RPH pin to ground turns off, and the voltage on this pin charges exponentially up to the RT pin potential. During this Ignition Ramp Mode, the output frequency exponentially decays to a minimum value. The rate of decay of this frequency is a function of the RPH * CPH time constant. Because the Ignition Ramp Mode ends when the voltage on the CPH pin reaches 5.15V, the ignition ramp is always 1/4th as long as the preheat time.

When the CPH pin reaches 5.15V, an open-drain transistor on the RUN pin turns on, and the external RRUN resistor is then in parallel with the RT resistor. The Run Mode operating frequency is therefore a function of the parallel combination of RRUN and RT, and this means that the operating power of the lamp can be programmed by means of RRUN.

The following graphs, Figures 8 and 9, illustrate the relationship between the effective RT resistance (i.e., the parallel combination of resistors which programs the CT capacitor charging current) and the operating frequency.

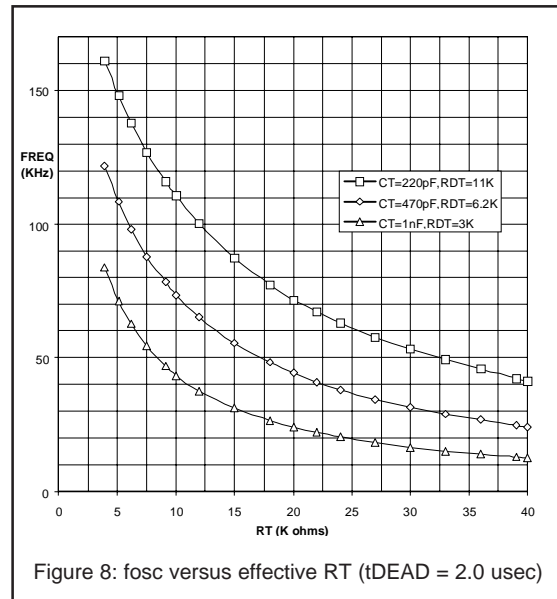


Figure 8: fosc versus effective RT (tDEAD = 2.0 usec)

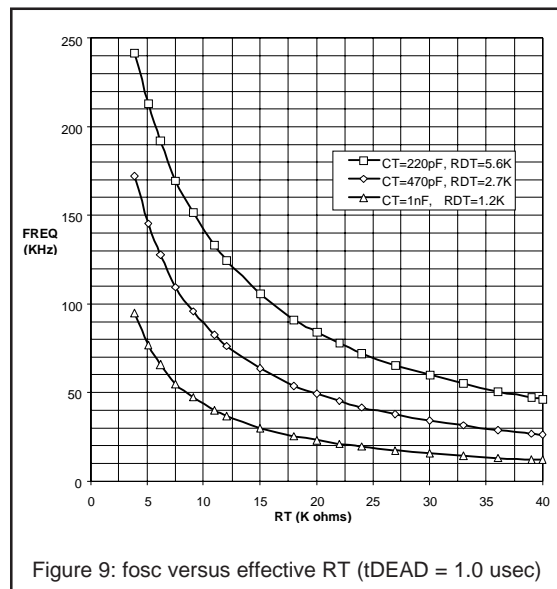
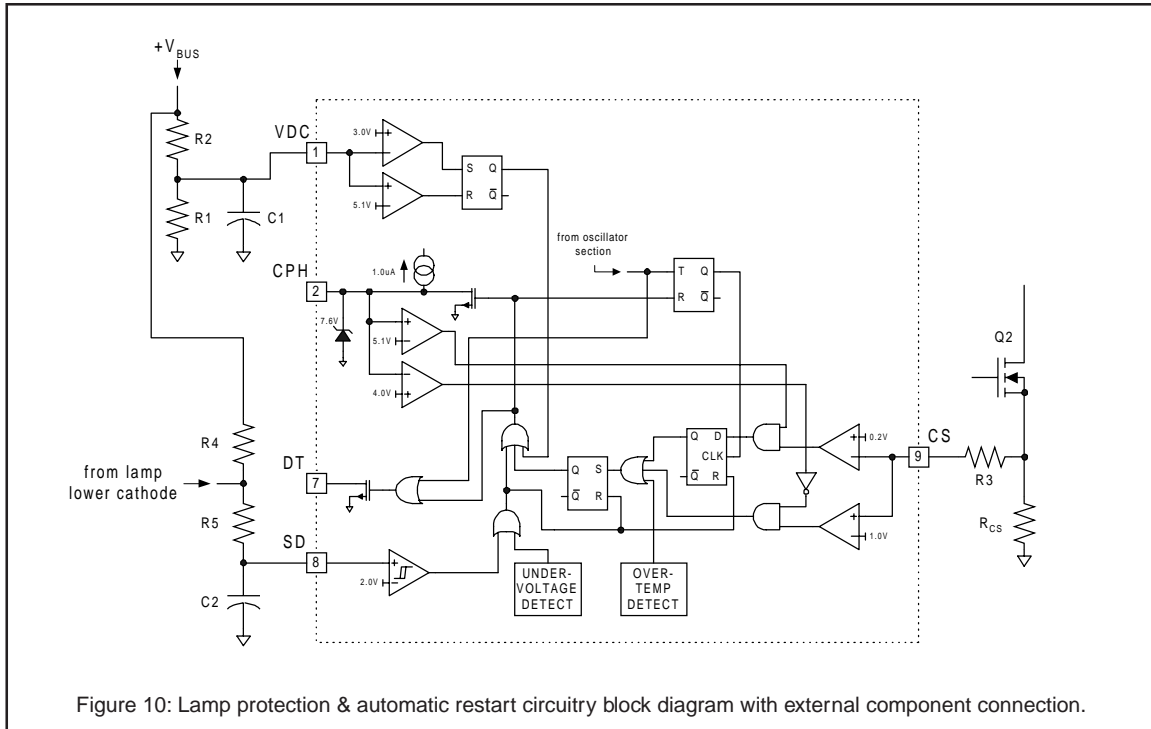


Figure 9: fosc versus effective RT (tDEAD = 1.0 usec)

Lamp Protection & Automatic Restart Circuitry Operation

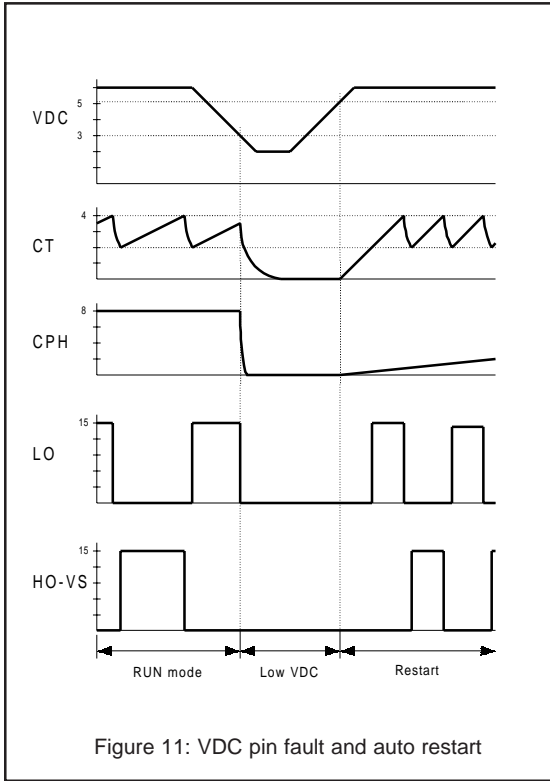
Three pins on the IR2157 are used for protection, as shown in Figure 10 below. These are VDC (dc bus monitor), SD (unlatched shutdown), and CS (latched shutdown).



Sensing the DC Bus Voltage

The first of these protection pins senses the voltage on the DC bus by means of an external resistor divider and an internal comparator with hysteresis. When power is first supplied to the IC at system startup, 3 conditions are required before oscillation is initiated: 1.) the voltage on the VCC pin must exceed the rising undervoltage lockout threshold (11.5V), 2.) the voltage at the VDC pin must exceed 5.1V, and 3.) the voltage on the SD pin must be below approximately 1.85V. If a low dc bus condition occurs during normal operation, or if power to the ballast is shut off, the dc bus will collapse prior to the VCC of the chip (assuming the VCC is derived from a charge

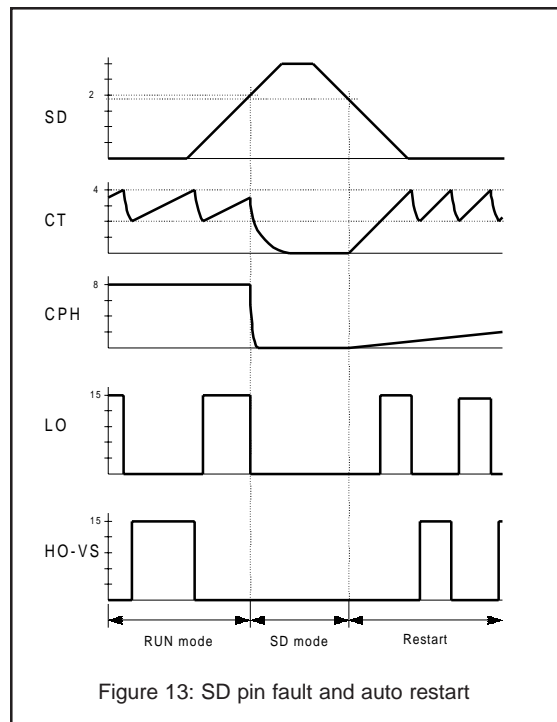
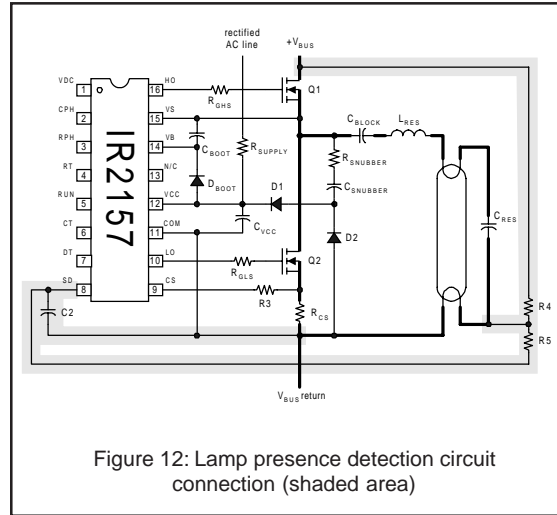
pump off of the output of the half-bridge). In this case, the voltage on the VDC pin will shut the oscillator off, thereby protecting the power transistors from potentially hazardous hard switching. Approximately 2V of hysteresis has been designed into the internal comparator sensing the VDC pin, in order to account for variations in the dc bus voltage under varying load conditions. When the dc bus recovers, the chip restarts from the beginning of the control sequence, as shown in timing diagram 11 below.



Lamp Presence Detection and Automatic Restart

The second protection pin, SD, is used for both unlatched shutdown and automatic restart functions. The SD pin would normally be connected to an external circuit which senses the presence of the lamp (or lamps), as shown in Figure 12.

When the SD pin exceeds 2.0V (approximately 150mV of hysteresis is included to increase noise immunity), signaling either a lamp fault or lamp removal, the oscillator is disabled, both gate driver outputs are pulled low, and the chip is put into the micropower mode. Since a lamp fault would normally lead to a lamp exchange, when a new lamp is inserted into the fixture, the SD pin would be pulled back to near the ground potential. Under these



conditions a reset signal would restart the chip from the beginning of the control sequence, as shown in the timing diagram in Figure 13.

Thus, for a lamp removal and replacement, the ballast automatically restarts the lamp in the proper manner, maximizing lamp life and minimizing stress on the power MOSFETs or IGBTs. The SD pin contains an internal 7.5V zener diode clamp, thereby reducing the number of external components required.

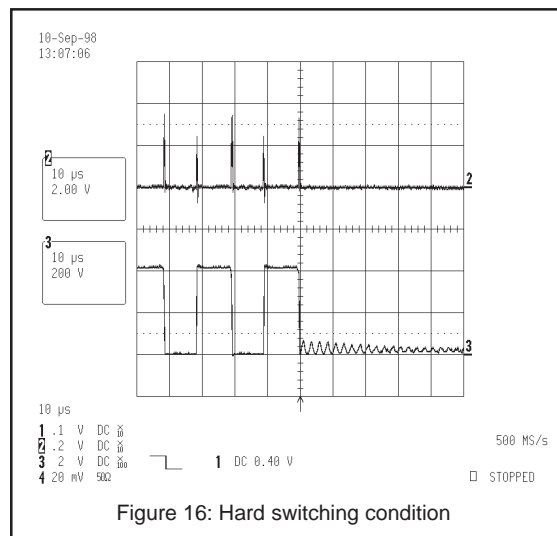
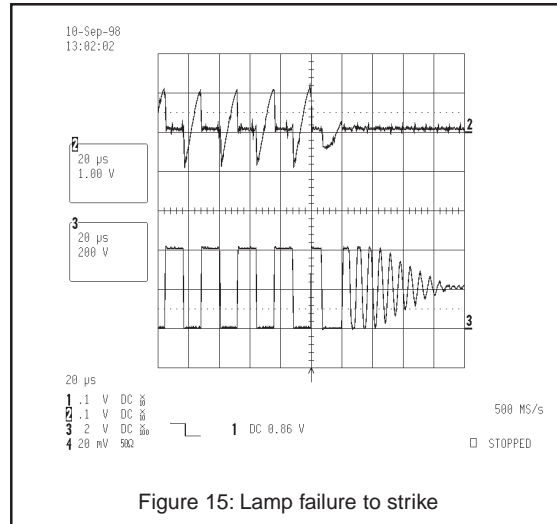
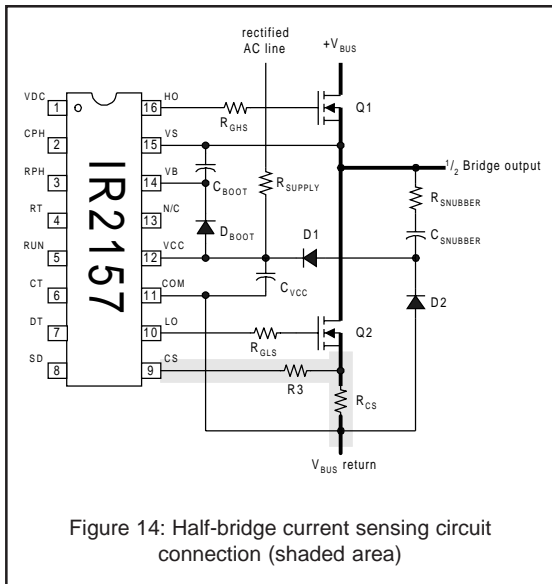
Half-Bridge Current Sensing and Protection

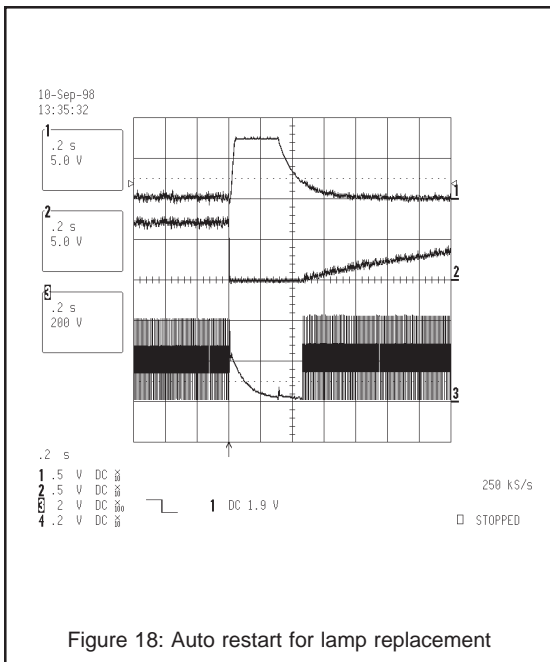
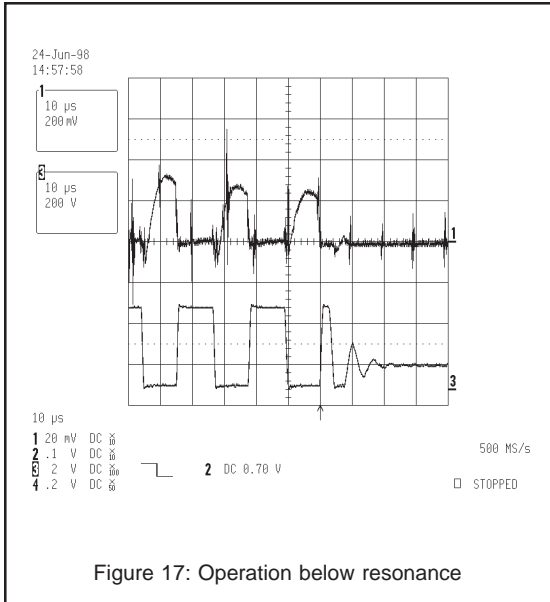
The third pin used for protection is the CS pin, which is normally connected to a resistor in the source of the lower power MOSFET, as shown in Figure 14.

The CS pin is used to sense fault conditions such as a failure of a lamp to strike, over-current during normal operation, hard switching, no load, and operation below resonance. If any one of these conditions is sensed, the fault latch is set, the oscillator is disabled, the gate driver outputs go low, and the chip is put into the micropower mode. The CS pin performs its sensing functions on a cycle-by-cycle basis in order to maximize ballast reliability. failure-to-strike, and For the over-current, hard switching fault conditions, the 1V, positive-going CS threshold is enabled at the end of the preheat time. For the under-current

and under-resonance conditions, there is a negative-going threshold of 0.2V which is enabled at the onset of the run mode. The sensing of this 0.2V threshold is synchronized with the falling edge of the LO output.

Figures 15, 16 and 17 are oscillographs of fault conditions. Figure 15 shows a failure of the lamp to strike, Figure 16 shows a hard switching condition and Figure 17 shows an under-current condition.

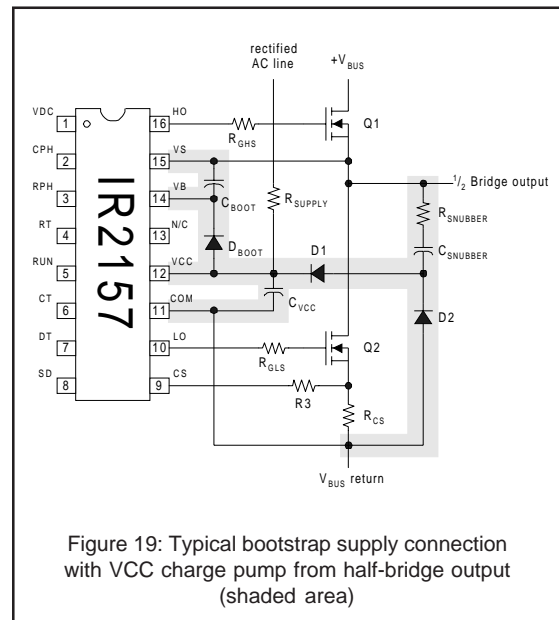




Recovery from such a fault condition is accomplished by cycling either SD pin or the VCC pin. When a lamp is removed, the SD pin goes high, the fault latch is reset, and the chip is held off in an unlatched state. Lamp replacement causes the SD pin to go low again, reinitiating the startup sequence. The fault latch can also be reset by the undervoltage lockout signal, if VCC falls below the lower undervoltage threshold.

Bootstrap Supply Considerations

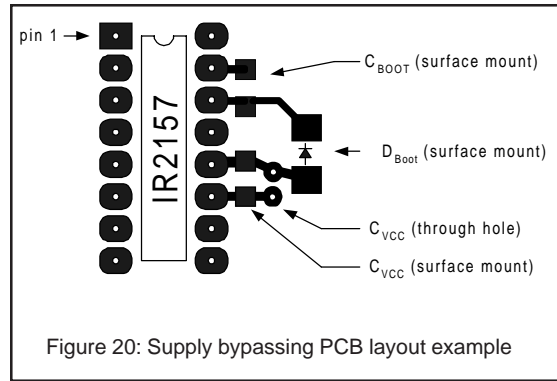
Power is normally supplied to the high-side circuitry by means of a simple charge pump from VCC, as shown in Figure 19 below.



A high voltage, fast recovery diode D_{BOOT} (the so-called bootstrap diode) is connected between VCC (anode) and VB (cathode), and a capacitor C_{BOOT} (the so-called bootstrap capacitor) is connected between the VB and VS pins. During half-bridge switching, when MOSFET Q₂ is on and Q₁ is off, the bootstrap capacitor C_{BOOT} is charged from the VCC decoupling capacitor, through the bootstrap diode D_{BOOT}, and through Q₂. Alternately, when Q₂ is off and Q₁ is on, the bootstrap diode is reverse-biased,

and the bootstrap capacitor (which 'floats' on the source of the upper power MOSFET) serves as the power supply to the upper gate driver CMOS circuitry. Since the quiescent current in this CMOS circuitry is very low (typically 45mA in the on-state), the majority of the drop in the VBS voltage when Q1 is on occurs due to the transfer of charge from the bootstrap capacitor to the gate of the power MOSFET.

VB should be bypassed to VS as close as possible to the pins of the IC with a low ESR/ESL capacitor. A PCB layout example is shown in figure 20. A rule of thumb for the value of this capacitor is to keep its minimum value at least 50 times the value of the total input capacitance (Ciss) of the MOSFET or IGBT being driven. In addition, the VS pin should be connected directly to the high side power MOSFET source.



Characteristic Curves

