TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC299AP,TC74HC299AF

8-Bit PIPO Shift Register with Asynchronous Clear

The TC74HC299A is a high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate $C^2MOS$ technology.

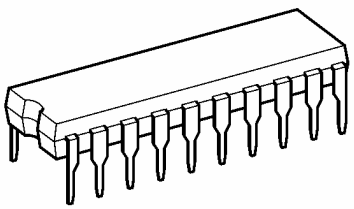
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It has four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G}1$ , $\overline{G}2$ ) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

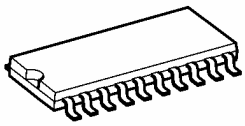
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC299AP



DIP20-P-300-2.54A

TC74HC299AF



SOP20-P-300-1.27A

Weight

DIP20-P-300-2.54A : 1.30 g (typ.)

SOP20-P-300-1.27A : 0.22 g (typ.)

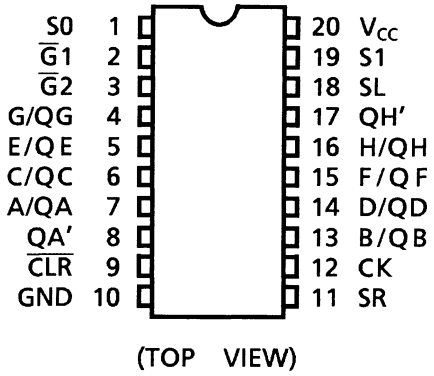
## Features (Note 1) (Note 2)

- High speed: $f_{max}$ = 42 MHz (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
- Outputs drive capability
  : 15 LSTTL loads for QA to QH
  10 LSTTL loads for QA', QH'
- Symmetrical output impedance
  : $|I_{OH}| = I_{OL}$ = 6 mA (min) For QA to QH
  $|I_{OH}| = I_{OL}$ = 4 mA (min) For QA', QH'
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC}$ (opr) = 2 to 6 V
- Pin and function compatible with 74LS299

Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

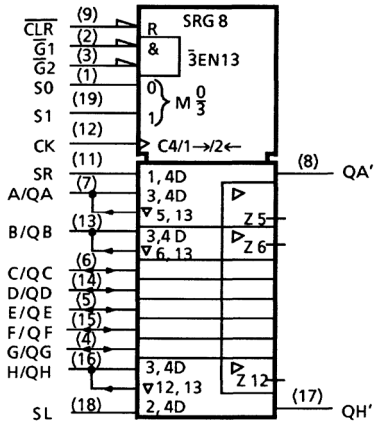
Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

## Pin Assignment




(TOP VIEW)

## IEC Logic Symbol




## Truth Table

| Mode | Inputs | | | | | | | | Inputs /Outputs | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | Function Select | | Outputs Control | | Clock | Serial | | A/QA | H/QH | QA' | QH' |
| | | S1 | S0 | $\overline{G1}$ (Note) | $\overline{G2}$ (Note) | CK | SL | SR | | | | |
| Z | L | H | H | X | X | X | X | X | Z | Z | L | L |
| CLR | L | L | X | L | L | X | X | X | L | L | L | L |
| | L | X | L | L | L | X | X | X | L | L | L | L |
| Hold | H | L | L | L | L | X | X | X | QA0 | QH0 | QA0 | QH0 |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | QGn | H | QGn |
| | H | L | H | L | L | ↑ | X | L | L | QGn | L | QGn |
| Shift Left | H | H | L | L | L | ↑ | H | X | QBn | H | QBn | H |
| | H | H | L | L | L | ↑ | L | X | QBn | L | QBn | L |
| Load | H | H | H | X | X | ↑ | X | X | a | h | a | h |

Note: When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z: High impedance

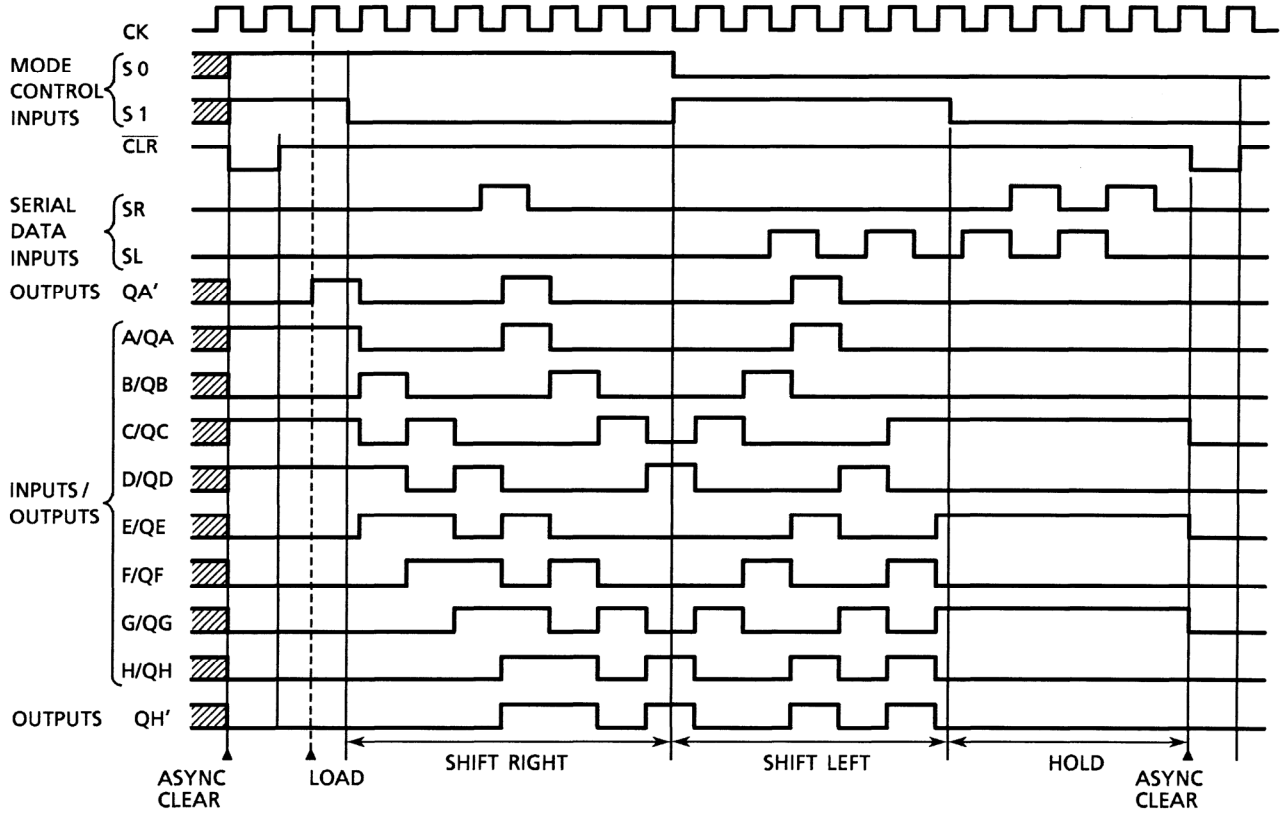
Qn0: The level of Qn before the indicated steady-state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by ↓ or ↑.

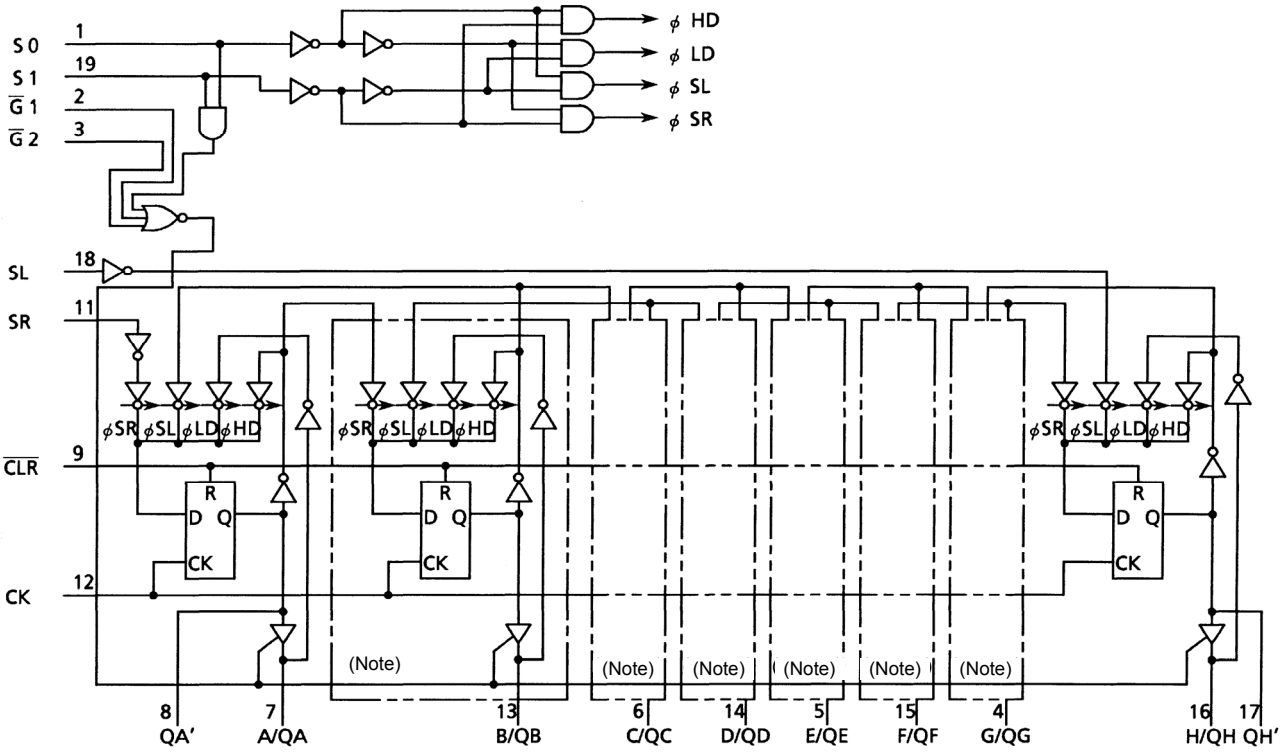
a, h: The level of the steady-state inputs A, H, respectively.

X: Don't care.

## Timing Chart




## System Diagram




Note: Equivalent circuits

## Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7 | V |
| DC input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | ±20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current (QH') | $I_{OUT}$ | ±25 | mA |
| DC output current (QA to QH) | $I_{OUT}$ | ±35 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±75 | mA |
| Power dissipation | $P_D$ | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2 to 6 | V |
| Input voltage | $V_{IN}$ | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | $t_r$, $t_f$ | 0 to 1000 ($V_{CC}$ = 2.0 V) | ns |
| | | 0 to 500 ($V_{CC}$ = 4.5 V) | |
| | | 0 to 400 ($V_{CC}$ = 6.0 V) | |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | | 4.5 | 3.15 | — | — | 3.15 | — | |
| | | | | | 6.0 | 4.20 | — | — | 4.20 | — | |
| Low-level input voltage | $V_{IL}$ | — | | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | | 4.5 | — | — | 1.35 | — | 1.35 | |
| | | | | | 6.0 | — | — | 1.80 | — | 1.80 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | $I_{OH}$ = −20 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | |
| | | | QA', QH' | $I_{OH}$ = −4 mA | 4.5 | 4.18 | 4.31 | — | 4.13 | — | |
| | | | | $I_{OH}$ = −5.2 mA | 6.0 | 5.68 | 5.80 | — | 5.63 | — | |
| | | | QA to QH | $I_{OH}$ = −6 mA | 4.5 | 4.18 | 4.31 | — | 4.13 | — | |
| | | | | $I_{OH}$ = −7.8 mA | 6.0 | 5.68 | 5.80 | — | 5.63 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | $I_{OL}$ = 20 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | QA', QH' | $I_{OL}$ = 4 mA | 4.5 | — | 0.17 | 0.26 | — | 0.33 | |
| | | | | $I_{OL}$ = 5.2 mA | 6.0 | — | 0.18 | 0.26 | — | 0.33 | |
| | | | QA to QH | $I_{OL}$ = 6 mA | 4.5 | — | 0.17 | 0.26 | — | 0.33 | |
| | | | | $I_{OL}$ = 7.8 mA | 6.0 | — | 0.18 | 0.26 | — | 0.33 | |
| 3-state output off state current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | | 6.0 | — | — | ±0.5 | — | ±5.0 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | | 6.0 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | | 6.0 | — | — | 4.0 | — | 40.0 | μA |

### Timing Recommended Operating Conditions (input: $t_r = t_f = 6$ ns)

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | Ta = −40 to 85°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Typ. | Limit | Limit | |
| Minimum pulse width (CK) | $t_{W(H)}$ / $t_{W(L)}$ | — | 2.0 | — | 75 | 95 | ns |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum pulse width ($\overline{CLR}$) | $t_{W(L)}$ | — | 2.0 | — | 75 | 88 | ns |
| | | | 4.5 | — | 15 | 18 | |
| | | | 6.0 | — | 12 | 15 | |
| Minimum set-up time ($\overline{SL}$, SR, A to H) | $t_s$ | — | 2.0 | — | 100 | 125 | ns |
| | | | 4.5 | — | 20 | 25 | |
| | | | 6.0 | — | 17 | 21 | |
| Minimum set-up time (S0, S1) | $t_s$ | — | 2.0 | — | 100 | 125 | ns |
| | | | 4.5 | — | 20 | 25 | |
| | | | 6.0 | — | 17 | 21 | |
| Minimum hold time (SL, SR, A to H) | $t_h$ | — | 2.0 | — | 0 | 0 | ns |
| | | | 4.5 | — | 0 | 0 | |
| | | | 6.0 | — | 0 | 0 | |
| Minimum hold time (S0, S1) | $t_h$ | — | 2.0 | — | 0 | 0 | ns |
| | | | 4.5 | — | 0 | 0 | |
| | | | 6.0 | — | 0 | 0 | |
| Minimum removal time ($\overline{CLR}$) | $t_{rem}$ | — | 2.0 | — | 50 | 65 | ns |
| | | | 4.5 | — | 10 | 13 | |
| | | | 6.0 | — | 8 | 10 | |
| Clock frequency | f | — | 2.0 | — | 6 | 5 | ns |
| | | | 4.5 | — | 30 | 24 | |
| | | | 6.0 | — | 35 | 23 | |

### AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Output transition time (QA', QH') | $t_{TLH}$ / $t_{THL}$ | — | — | 4 | 8 | ns |
| Propagation delay time (CK-QA', QH') | $t_{pLH}$ / $t_{pHL}$ | — | — | 19 | 30 | ns |
| Propagation delay time ($\overline{CLR}$-QA', QH') | $t_{pHL}$ | — | — | 17 | 30 | ns |
| Maximum clock frequency | $f_{max}$ | — | 35 | 73 | — | MHz |

**AC Characteristics (input: $t_r = t_f = 6$ ns)**

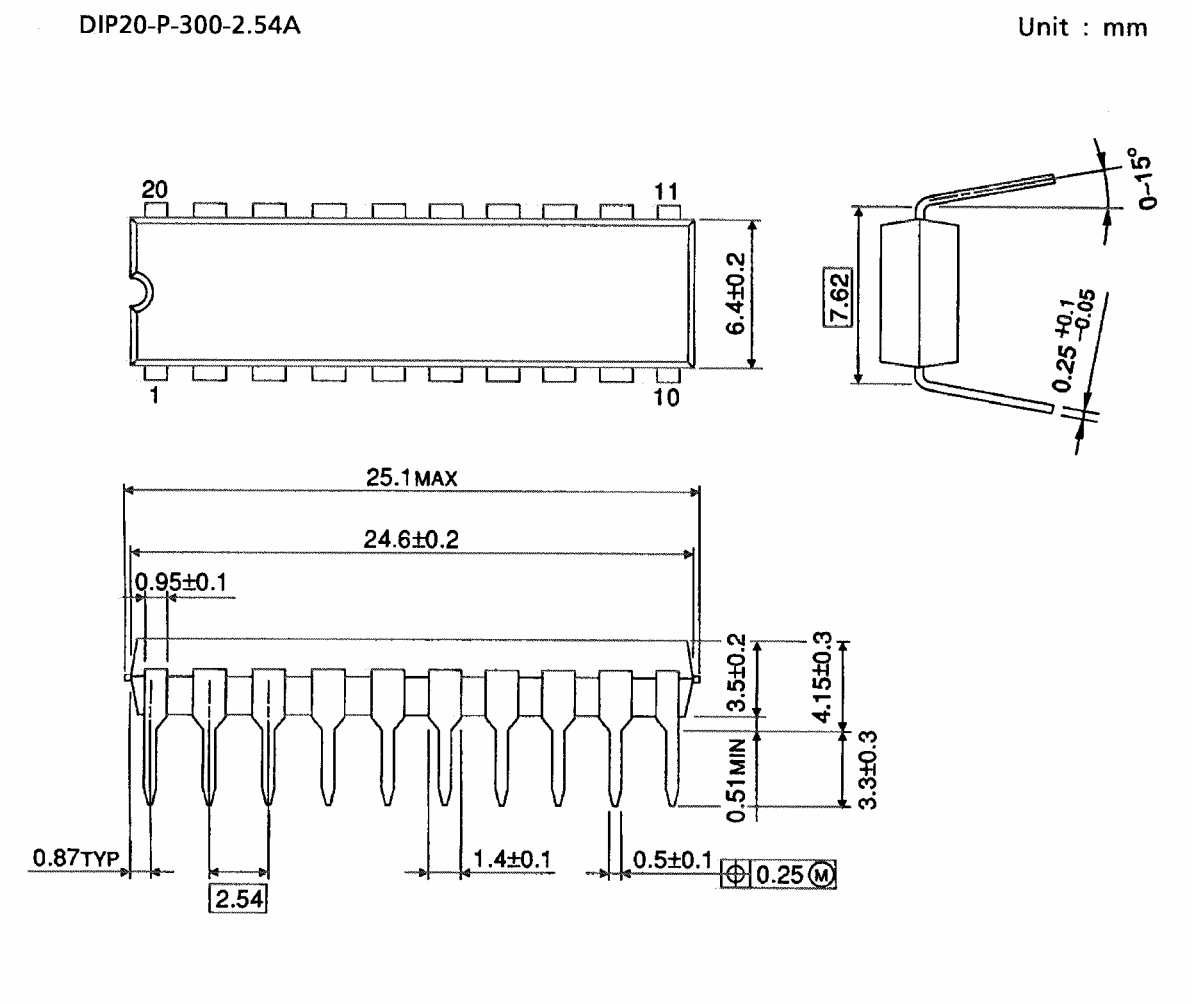
| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | CL (pF) | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| Output transition time (QA to QH) | $t_{TLH}$ $t_{THL}$ | — | 50 | 2.0 | — | 25 | 60 | — | 75 | ns |
| | | | | 4.5 | — | 7 | 12 | — | 15 | |
| | | | | 6.0 | — | 6 | 10 | — | 13 | |
| Output transition time (QA', QH') | $t_{TLH}$ $t_{THL}$ | — | 50 | 2.0 | — | 30 | 75 | — | 95 | ns |
| | | | | 4.5 | — | 8 | 15 | — | 19 | |
| | | | | 6.0 | — | 7 | 13 | — | 16 | |
| Propagation delay time (CK-QA', QH') | $t_{pLH}$ $t_{pHL}$ | — | 50 | 2.0 | — | 85 | 170 | — | 215 | ns |
| | | | | 4.5 | — | 23 | 34 | — | 43 | |
| | | | | 6.0 | — | 18 | 29 | — | 37 | |
| Propagation delay time ($\overline{CLR}$ -QA', QH') | $t_{pHL}$ | — | 50 | 2.0 | — | 85 | 175 | — | 220 | ns |
| | | | | 4.5 | — | 24 | 35 | — | 44 | |
| | | | | 6.0 | — | 18 | 30 | — | 37 | |
| Propagation delay time (CK-QA to QH) | $t_{pLH}$ $t_{pHL}$ | — | 50 | 2.0 | — | 80 | 160 | — | 200 | ns |
| | | | | 4.5 | — | 21 | 32 | — | 40 | |
| | | | | 6.0 | — | 17 | 27 | — | 34 | |
| | | | 150 | 2.0 | — | 100 | 200 | — | 250 | |
| | | | | 4.5 | — | 26 | 40 | — | 50 | |
| | | | | 6.0 | — | 21 | 34 | — | 43 | |
| Propagation delay time ($\overline{CLR}$ -QA to QH) | $t_{pHL}$ | — | 50 | 2.0 | — | 85 | 190 | — | 240 | ns |
| | | | | 4.5 | — | 24 | 38 | — | 48 | |
| | | | | 6.0 | — | 18 | 30 | — | 38 | |
| | | | 150 | 2.0 | — | 105 | 230 | — | 90 | |
| | | | | 4.5 | — | 29 | 46 | — | 58 | |
| | | | | 6.0 | — | 22 | 36 | — | 46 | |
| Output enable time | $t_{pZL}$ $t_{pZH}$ | $R_L = 1$ kΩ | 50 | 2.0 | — | 60 | 130 | — | 165 | ns |
| | | | | 4.5 | — | 17 | 26 | — | 33 | |
| | | | | 6.0 | — | 13 | 22 | — | 28 | |
| | | | 150 | 2.0 | — | 78 | 170 | — | 215 | |
| | | | | 4.5 | — | 23 | 34 | — | 43 | |
| | | | | 6.0 | — | 17 | 29 | — | 36 | |
| Output disable time | $t_{pLZ}$ $t_{pHZ}$ | $R_L = 1$ kΩ | 50 | 2.0 | — | 54 | 150 | — | 190 | ns |
| | | | | 4.5 | — | 19 | 30 | — | 38 | |
| | | | | 6.0 | — | 16 | 26 | — | 33 | |
| Maximum clock frequency | $f_{max}$ | — | 50 | 2.0 | 6 | 12 | — | 5 | — | MHz |
| | | | | 4.5 | 30 | 58 | — | 24 | — | |
| | | | | 6.0 | 35 | 80 | — | 28 | — | |
| Input capacitance | $C_{IN}$ | — | | | — | 5 | 10 | — | 10 | pF |
| Output capacitance | $C_{OUT}$ | — | | | — | 13 | — | — | — | pF |
| Power dissipation capacitance | $C_{PD}$ (Note) | — | | | — | 170 | — | — | — | pF |

Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Package Dimensions

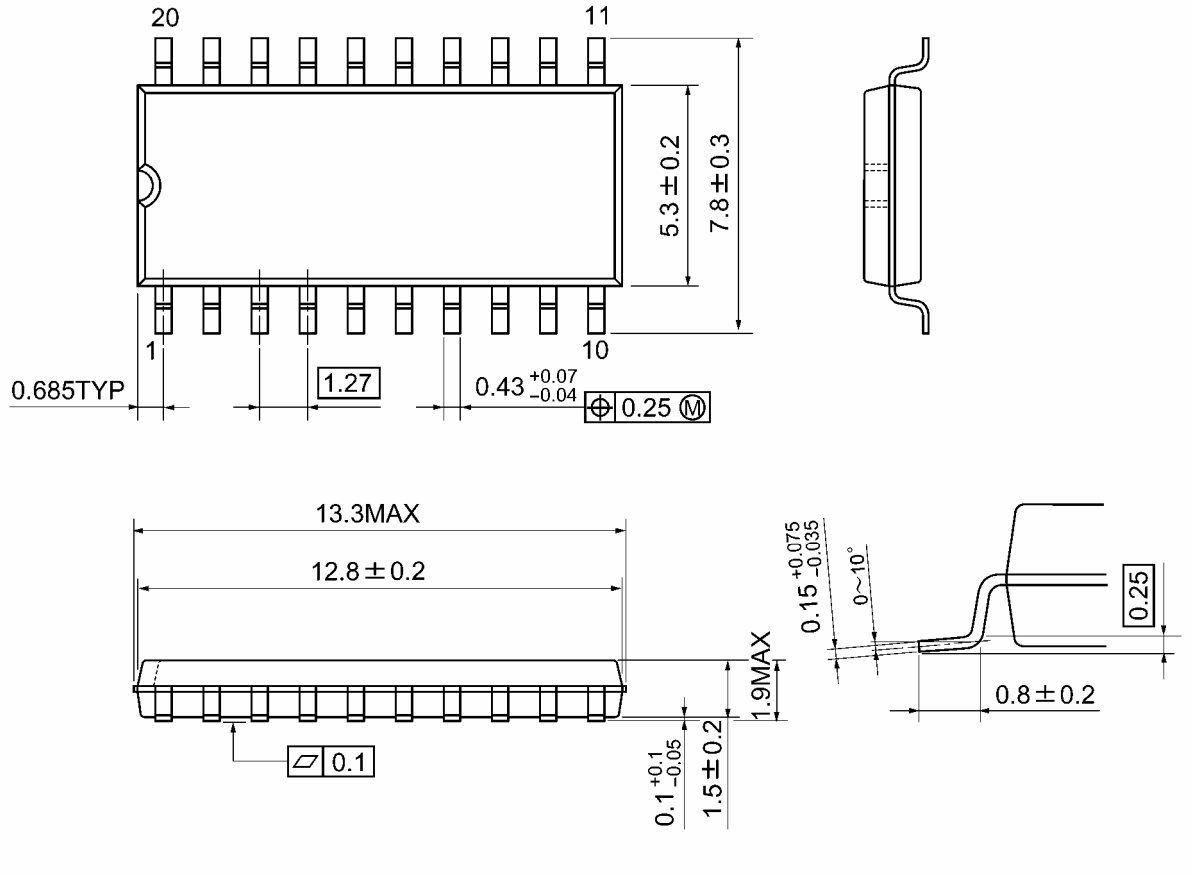
DIP20-P-300-2.54A Unit : mm




Weight: 1.30 g (typ.)

## Package Dimensions

SOP20-P-300-1.27A Unit: mm




Weight: 0.22 g (typ.)

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20070701-EN GENERAL

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