LM339 Quad Voltage Comparator

QUAD VOLTAGE COMPARATORS

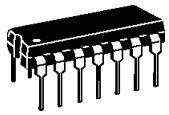
These comparators are designed for use in level detection, low–level sensing and memory applications in consumer automotive and industrial electronic applications.

FEATURES

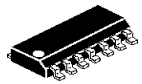
- Single or dual supplies
- Low Input Bias Current - 25nA(Typ)
- Low Input Offset Voltage - ±1.0mV(Typ)
- Low Input Offset Current - ±5.0nA(Typ)
- Input common-mode voltage range to GND
- Output Compatible with TTL, MOS, and CMOS
- Low output saturation voltage - 130mV(Typ) @ 4.0mA

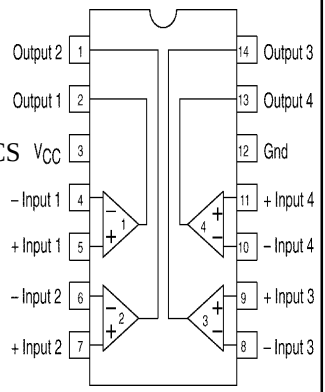
PIN ARRANGEMENT

14 DIP LM339CD



14 SOP LM339CS





ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	V
Input Differential Voltage Range	V_{IDR}	36	V
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	V
Output Short Circuit-to-Ground	I_{SC}	Continuous	mA
Power Dissipation @ 25°C Derate above 25°C	P_D	1.0 8.0	W mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_S	-65 to 150	°C

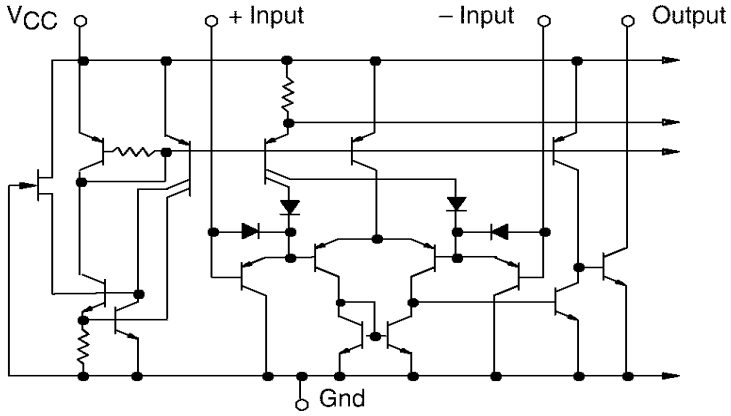
Notes:
1. The max. output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becooming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when inputs become ≥ ground or negative supply.
3. At output switch point, V_O = 1.4 Vdc, R_S = 100 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0V to V_{CC} = –1.5V).
4. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Response time is specified with a 100mV step and 5.0mV of overdrive. For larger signals, 300ns is typical.
6. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state.

ELECTRICAL CHARACTERISTICS

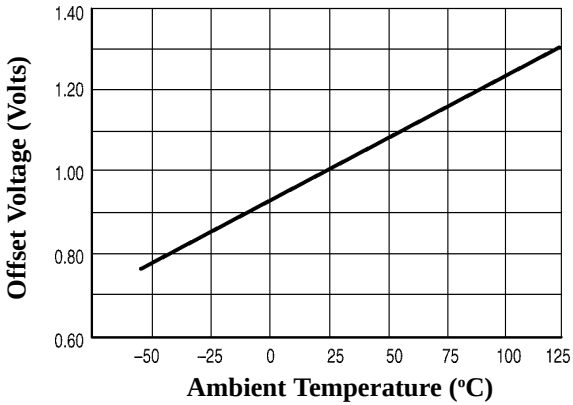
V_{CC} = 5.0Vdc, 0°C ≤ T_A ≤ 25°C (unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (3)	V_{IO}				mV
T_A = 25°C		---	+2.0	+5.0	
T_A = 0°C to 70°C		---	---	+9.0	
Input Bias Current (3,4)	I_{IB}				nA
T_A = 25°C		---	25	250	
T_A = 0°C to 70°C		---	---	400	
Input Offset Current (3)	I_{IO}				nA
T_A = 25°C		---	±50	±50	
T_A = 0°C to 70°C		---	---	±150	
Input Common Mode Voltage Range (6)	V_{ICR}				V
T_A = 25°C		0	---	V_{CC}-1.5	
T_A = 0°C to 70°C		0	---	V_{CC}-2.0	
Supply Current	I_{CC}				mA
R_L = ∞, T_A = 25°C		---	0.8	2.0	
R_L = ∞, V_{CC} = 30Vdc		---	---	---	
Voltage Gain	A_{VOL}	---	200	---	V/mV
R_L ≥ 15K, V_{CC} = 15 Vdc					
Large Signal Response Time	---	---	300	---	ns
V1 = TTL Logic Swing.					
Vref = 1.4 Vdc					
VRL = 5.0 Vdc, RL = 5.1K					
Response Time (6)	t_{TLH}	---	13	---	µs
VRL = 5.0 Vdc, RL = 5.1K					
Output Sink Current	I_{Sink}	6.0	16	---	mA
V1(-) ≥ 1.0 Vdc, V1(+) = 0 Vdc					
Vo ≤ 1.5 Vdc					
Saturation Voltage	V_{SAT}				mV
V1(-) ≥ 1.0 Vdc, V1(+) = 0 Vdc		---	130	400	
I_{Sink} ≤ 4.0 mA, T_A = 25°C					
0°C ≤ T_A ≤ 70°C		---	---	700	
Output Leakage Current	I_{OL}				nA
V1(-) = 0 Vdc, V1(+) ≥ 1.0 Vdc		---	0.1	---	
Vo = 5.0 Vdc, T_A = 25°C					
V1(-) = 0 Vdc, V1(+) ≥ 1.0 Vdc		---	---	1000	
Vo = 30 Vdc, 0°C ≤ T_A ≤ 70°C					
Input Differential Voltage (6)	V_{ID}	---	---	V_{CC}	V
All Vin ≥ GND or V-Supply					
0°C ≤ T_A ≤ 70°C					

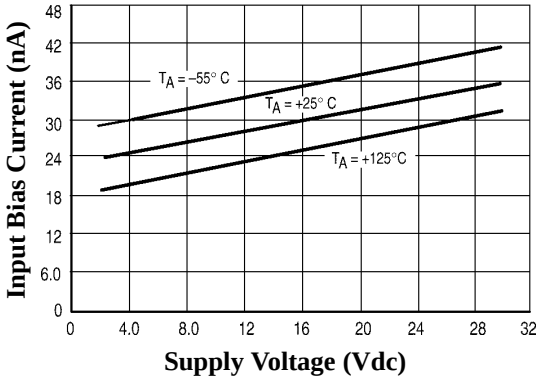
CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)

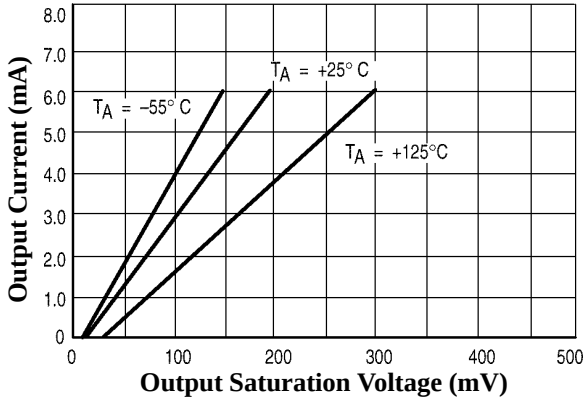


NORMALIZED INPUT OFFSET VOLTAGE



INPUT BIAS CURRENT





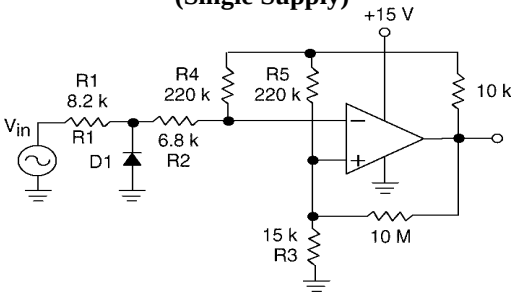
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors <10 kΩ should be used.

The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than –0.3 V should not be used.

Zero Crossing Detector (Single Supply)

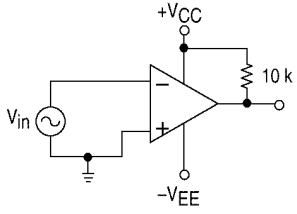


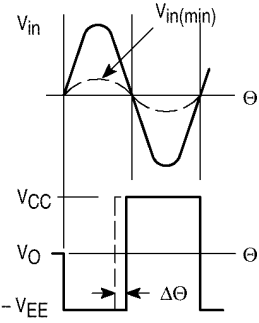
D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10}$$ for small error in zero crossing.

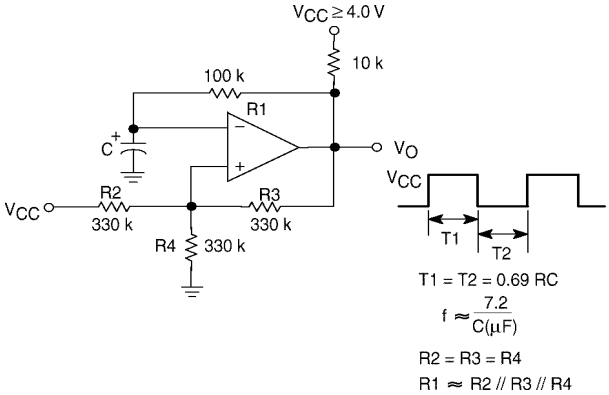
Zero Crossing Detector (Split Supply)





$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).

Square Wave Oscillator



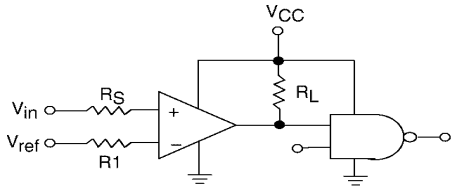
$T1 = T2 = 0.69\ RC$

$$f \approx \frac{7.2}{C(\mu F)}$$

$R2 = R3 = R4$

$R1 \approx R2\ //\ R3\ //\ R4$

Driving Logic

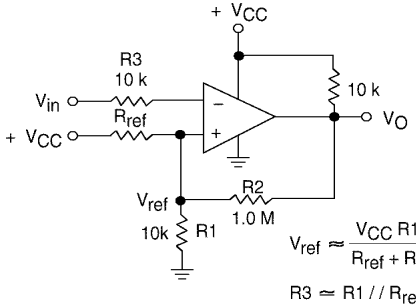


R_S = Source Resistance

$R1 \simeq R_S$

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Inverting Comparator With Hysteresis



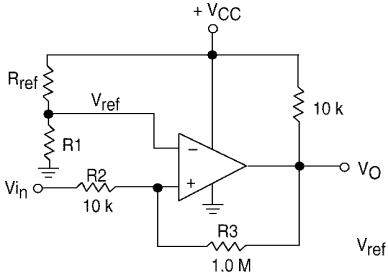
$$V_{ref} \simeq \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$R3 \simeq R1\ //\ R_{ref}\ //\ R2$

$$V_H = \frac{R1\ //\ R_{ref}}{R1//\ R_{ref} + R2}\ [V_{O(max)} - V_{O(min)}]$$

$R2 \gg Rref\ //\ R1$

Non-Inverting Comparator With Hysteresis



$$V_{ref} = \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$R2 \approx R1\ //\ R_{ref}$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\ [(V_{O(max)} - V_{O(min)}]$$