Ordering number : ENA0496

SANYO Semiconductors
DATA SHEET

LC87F1964A

CMOS IC
FROM 64K byte, RAM 5K byte on-chip

8-bit 1-chip Microcontroller With USB-host Controller

Overview

The SANYO LC87F1964A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 5120-byte RAM, an on-chip debugger, a sophisticated 16-bit timers/counters (may be divided into 8-bit timers), 16-bit timers/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), two 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, three synchronous SIO interface (with automatic block transmit/receive function), an asynchronous/synchronous SIO interface, a UART interface (full duplex), a Full-Speed USB interface (host controller), an 8-bit 12-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, and a 32-source 10-vector address interrupt feature.

Features

■Flash ROM
- Capable of on-board-programming with wide range, 3.0 to 5.5V, of voltage source.
- Block-erasable in 128-byte units
- Writable in 2-byte units
- 65536 × 8 bits

■RAM
- 5120 × 9 bits

■Minimum Bus Cycle
- 83.3ns (CF=12MHz)

  Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time
- 250ns (CF=12MHz)

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

■Ports

• I/O ports	
Ports whose I/O direction can be designated in 1 bit units	28 (P10 to P17, P20 to P27, P30 to P34, P70 to P73, PWM0, PWM1, XT2)
Ports whose I/O direction can be designated in 4 bit units	8 (P00 to P07)
• USB ports	2 (UHD+, UHD–)
• Dedicated oscillator ports	2 (CF1, CF2)
• Input-only port (also used for oscillation)	1 ($\overline{XT1}$)
• Reset pins	1 ($\overline{RES}$)
• Power pins	6 (V_{SS}1 to 3, V_{DD}1 to 3)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an-8bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes

■SIO

- SIO0: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 512/3 tCYC
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8-data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8-data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8-data bits, stop detect)
- SIO4: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Automatic continuous data transmission (1 to 4096 bytes, specifiable in 1-byte units, suspension and resumption of data transmission possible in 1-byte or 2-bytes units)
  4) Auto-start-on-falling-edge function
  5) Clock polarity selectable
  6) CRC16 calculator circuit built in

Continued on next page.

Continued from preceding page.

- SIO9: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Automatic continuous data transmission (1 to 4096 bytes, specifiable in 1-byte units, suspension and resumption of data transmission possible in 1-byte or 2-bytes units)
  4) Auto-start-on-falling-edge function
  5) Clock polarity selectable
  6) CRC16 calculator circuit built in

■Full duplex UART
- UART1
  1) Data length: 7/8/9 bits selectable
  2) Stop bits: 1 bit (2 bits in continuous transmission mode)
  3) Baud rate: 16/3 to 8192/3 tCYC

■AD Converter : 8 bits × 12 channels

■PWM: Multifrequency 12-bit PWM × 2 channels

■ USB interface (host controller)
- Full-Speed is supported
- Transfer type: Control, Bulk, Interrupt, or Isochronous transfer possible

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
- Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- Able to output oscillation clock of sub clock.

■Interrupts
- 32 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/UHC bus active
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/UHC device attach/UHC device detach/UHC resume
6	0002BH	H or L	T1L/T1H/SIO9
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/SIO4/UART1 transmit
9	00043H	H or L	ADC/T6/T7/UHC-ACK/UHC-NAK/UHC error/UHC STALL
10	0004BH	H or L	Port 0/PWM0/PWM1/UHC-SOF

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels : 2560 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, USB interface
- Crystal oscillation circuit: For system clock, time-of-day clock
- PLL circuit (internal): For USB interface (see Fig.5)

■Standby Function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
    (1) Setting the reset pin to the lower level.
    (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    (3) Having an interrupt source established at port 0
    (4) Having an bus active interrupt source established in the USB host controller circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are five ways of resetting the X'tal HOLD mode.
    (1) Setting the reset pin to the low level
    (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    (3) Having an interrupt source established at port 0
    (4) Having an interrupt source established in the base timer circuit
    (5) Having an bus active interrupt source established in the USB host controller circuit

■Package Form
- SQFP48(7×7): Lead-free type
- QIP48E(14×14): Lead-free type

■Development Tools
- On-chip debugger: TCB87 type-B + LC87F1964A

■Flash ROM programming boards

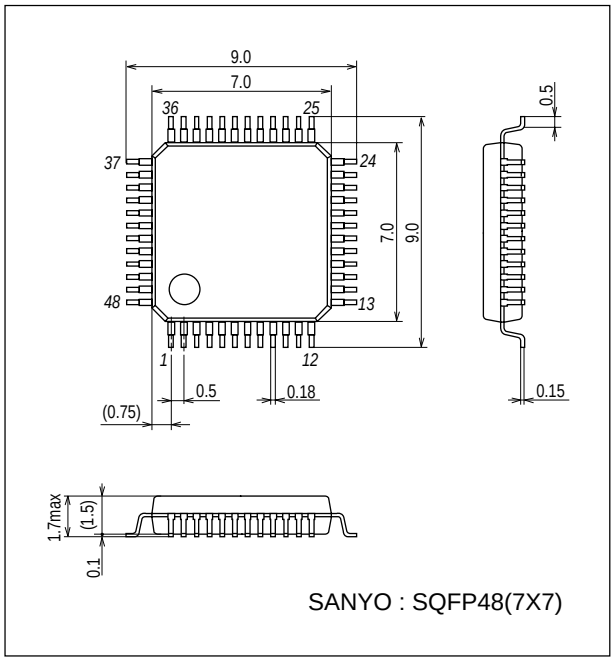
Package	Programming boards
QIP48E(14×14)	W87F55256Q
SQFP48(7×7)	W87F55256SQ

■Recommended EPROM programmer

Maker	Model	Supported version	Device
Flash Support Group, Inc. (Single)	AF9708/AF9709/AF9709B (including product of Ando Electric Co.,Ltd)	After Rev02.65	LC87F1964A
SANYO	SKK (SANYO FWS)	Application Version: After 1.03 Chip Data Version: After 2.01	LC87F1964

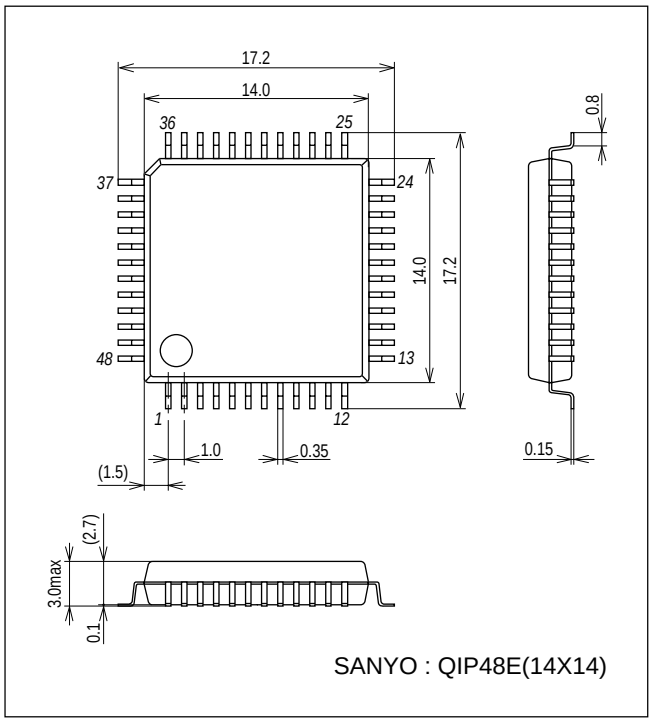
Package Dimensions

unit : mm (typ)
3163B

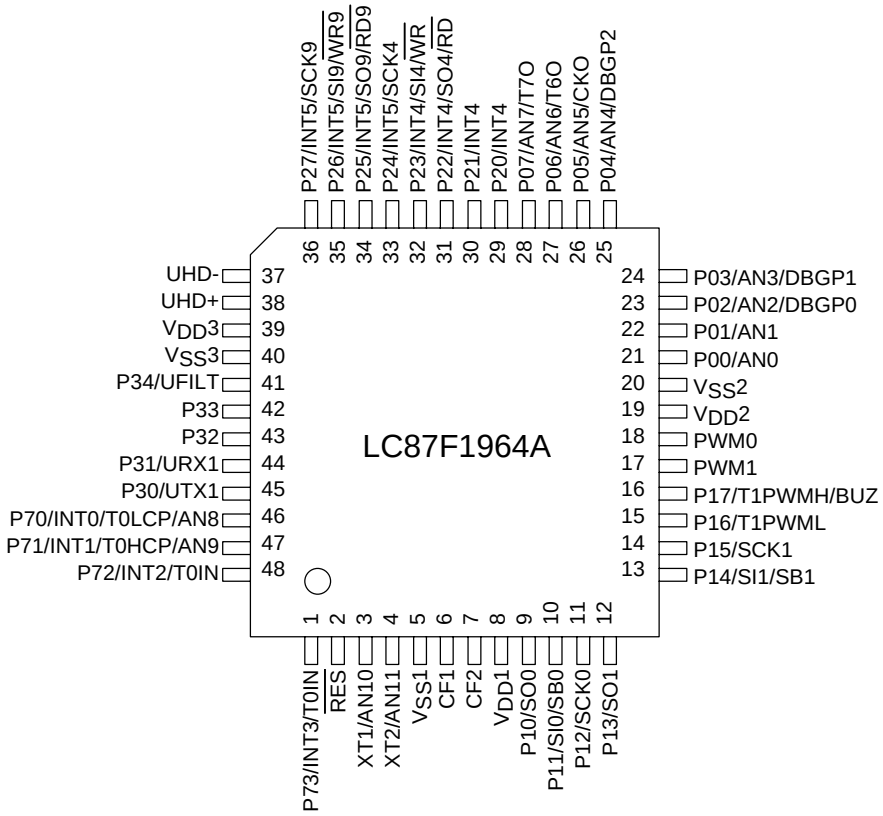


Package Dimensions

unit : mm (typ)
3156A



Pin Assignments



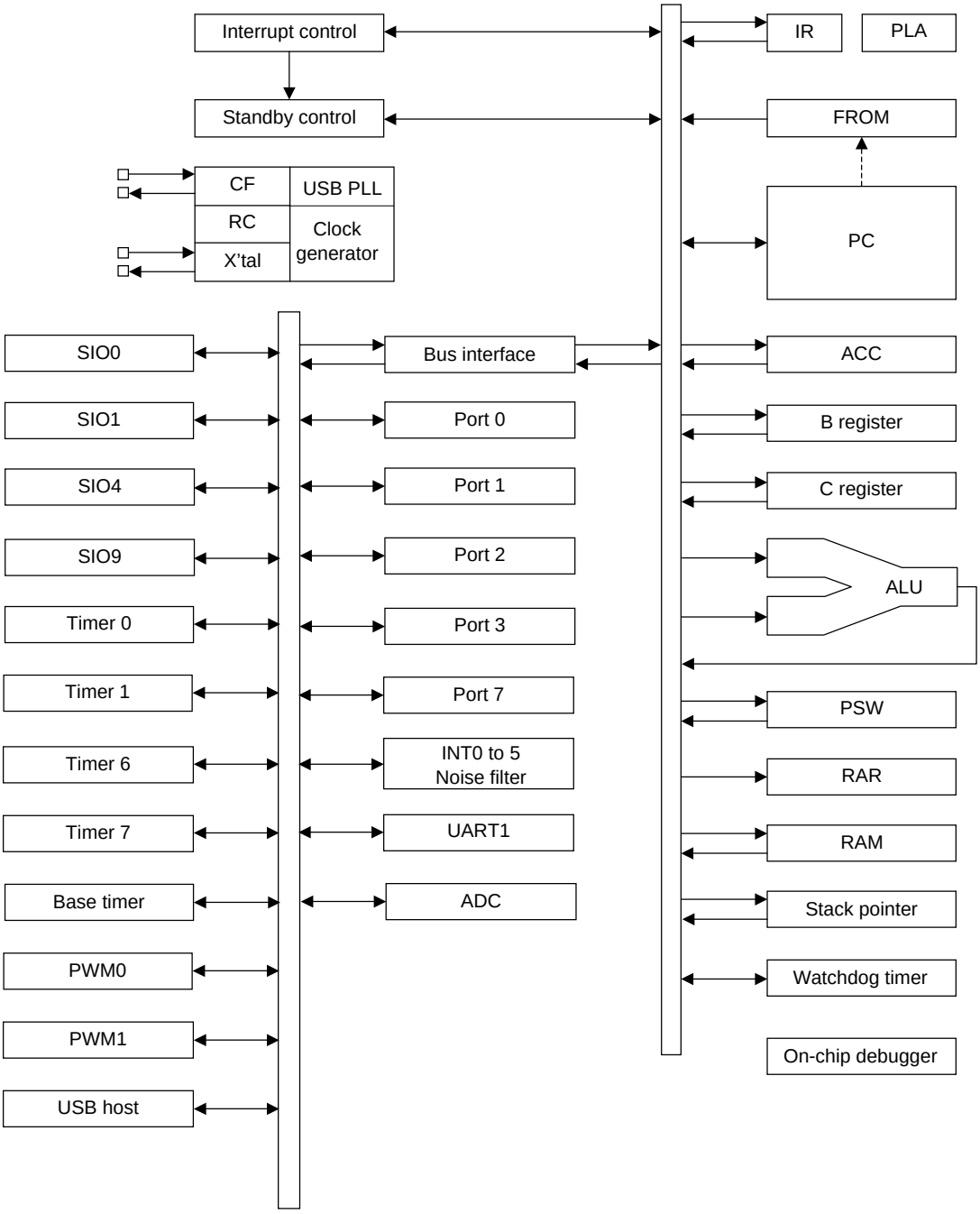
Top view

SANYO: SQFP48(7×7) “Lead-free Type”
SANYO: QIP48E(14×14) “Lead-free Type”

SQFP48/QIP48	NAME
1	P73/INT3/T0IN
2	$\overline{RES}$
3	XT1/AN10
4	XT2/AN11
5	$V_{SS}1$
6	CF1
7	CF2
8	$V_{DD}1$
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1
13	P14/SI1/SB1
14	P15/SCK1
15	P16/T1PWML
16	P17/T1PWMH/BUZ
17	PWM1
18	PWM0
19	$V_{DD}2$
20	$V_{SS}2$
21	P00/AN0
22	P01/AN1
23	P02/AN2/DBGP0
24	P03/AN3/DBGP1

SQFP48/QIP48	NAME
25	P04/AN4/DBGP2
26	P05/AN5/CKO
27	P06/AN6/T6O
28	P07/AN7/T7O
29	P20/INT4
30	P21/INT4
31	P22/INT4/SO4/$\overline{RD}$
32	P23/INT4/SI4/$\overline{WR}$
33	P24/INT5/SCK4
34	P25/INT5/SO9/$\overline{RD9}$
35	P26/INT5/SI9/$\overline{WR9}$
36	P27/INT5/SCK9
37	UHD-
38	UHD+
39	$V_{DD}3$
40	$V_{SS}3$
41	P34/UFILT
42	P33
43	P32
44	P31/URX1
45	P30/UTX1
46	P70/INT0/T0LCP/AN8
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,
$V_{SS}2$,
$V_{SS}3$</td><td></td><td>-power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$,
$V_{DD}2$</td><td></td><td>+power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}3$</td><td></td><td>USB reference voltage pin</td><td>Yes</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units.
• HOLD reset input
• Port 0 interrupt input
• Pins functions
AD converter input port: AN0 to AN7 (P00 to P07)
On-chip debugger pins: DBGP0 to DBGP2 (P02 to P04)
P05: System Clock Output
P06: Timer 6 toggle outputs
P07: Timer 7 toggle outputs</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P20 to P23: INT4 input/HOLD reset input/timer 1 event input/
timer 0L capture input/timer 0H capture input
P24 to P27: INT5 input/HOLD reset input/timer 1 event input/
timer 0L capture input/ timer 0H capture input
P22: SIO4 date I/O/parallel interface $\overline{RD}$ output
P23: SIO4 date I/O/parallel interface $\overline{WR}$ output
P24: SIO4 clock I/O
P25: SIO9 date I/O/parallel interface $\overline{RD9}$ output
P26: SIO9 date I/O/parallel interface $\overline{WR9}$ output
P27: SIO9 clock I/O
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>Yes</td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 3
P30 to P34</td><td>I/O</td><td>• 5-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30: UART1 transmit
P31: UART1 receive
P34: USB interface PLL filter pin (see Fig.5)</td><td>Yes</td></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/
High speed clock counter input
P73: INT3 input (with noise filter) /timer 0 event input/ timer 0H capture input
AD converter input port: AN8(P70), AN9(P71)Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0
PWM1</td><td>I/O</td><td>• PWM0 and PWM1 output port
• General-purpose input port</td><td>No</td></tr>
<tr><td>UHD-</td><td>I/O</td><td>• USB data I/O pin UHD-
• General-purpose I/O port</td><td>No</td></tr>
<tr><td>UHD+</td><td>I/O</td><td>• USB data I/O pin UHD+
• General-purpose I/O port</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Pin functions
General-purpose input port
AD converter input port: AN10
Must be connected to $V_{DD}1$ if not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Pin functions
General-purpose I/O port
AD converter input port: AN11
Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

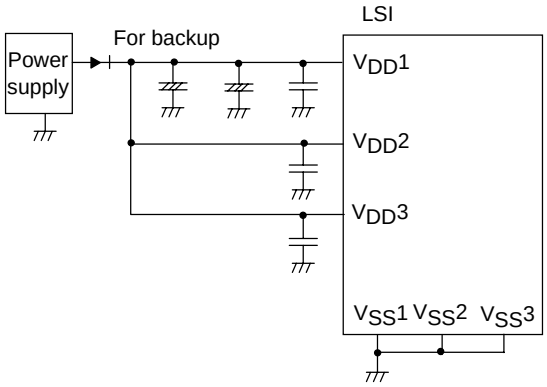
Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17 P20 to P27 P30 to P34	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
UHD+, UHD-	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal oscillator output	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

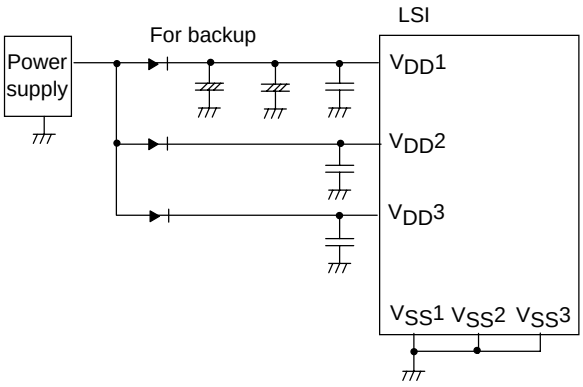
Power Pin Treatment

Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.

Example 1: When the microcontroller is in the backup state in the HOLD mode, the power to sustain the high level of output ports is supplied by their backup capacitors.



Example 2: The high level output at ports is not sustained and unstable in the HOLD backup mode.



USB Reference Power Option

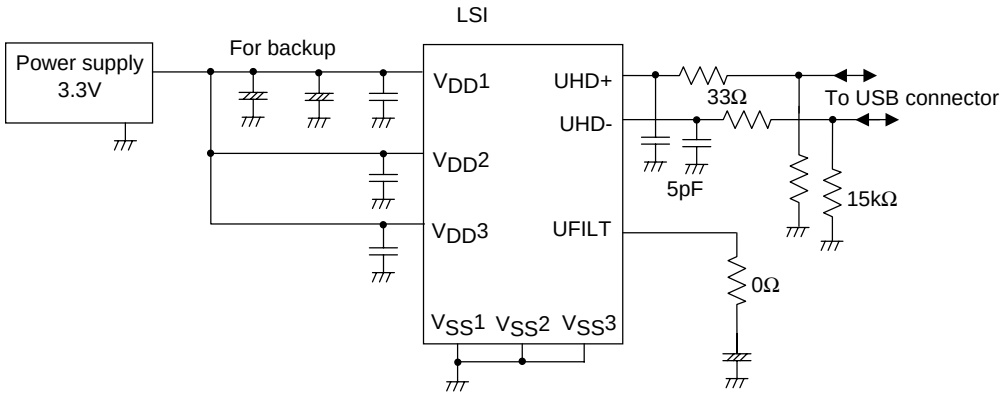
When a voltage 4.5 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by option selection. The procedure for marking the option selection is described below.

		(1)	(2)	(3)	(4)
Option selection	USB Regulator	USE	USE	USE	NONUSE
	USB Regulator in HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB Regulator in HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal state	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100µA compared with when the reference voltage circuit is inactive.

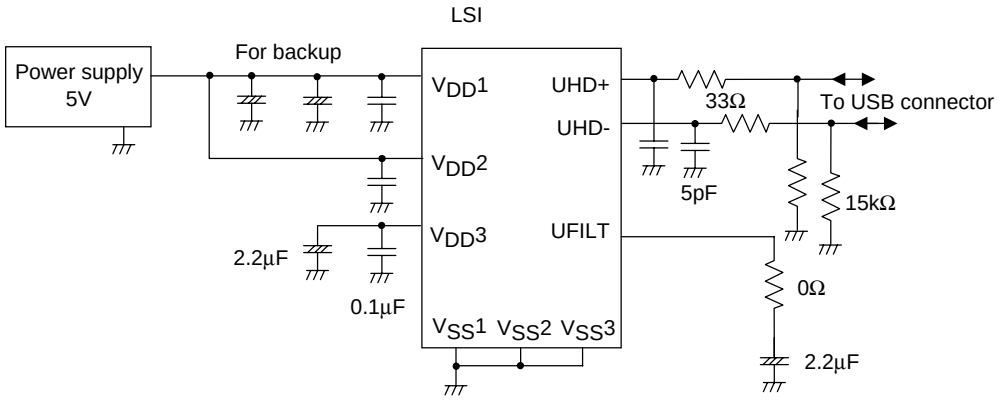
Example 1: $V_{DD}1=V_{DD}2=3.3V$

- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.



Example 2: $V_{DD}1=V_{DD}2=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and V_{SS}.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, CF1			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2, 3, 7 PWM0, PWM1 XT2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		-20			
		IOPH(3)	Ports 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-7.5			
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15			
		IOMH(3)	Ports 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total of all applicable pins		-25			
		ΣIOAH(2)	Ports 1 PWM0, PWM1	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins		-45			
		ΣIOAH(4)	Ports 3 P71 to P73	Total of all applicable pins		-10			
		ΣIOAH(5)	UHD+, UHD-	Total of all applicable pins		-25			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 3, 7 XT2	Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Ports 3, 7 XT2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total of all applicable pins				45	
		ΣIOAL(2)	Ports 1 PWM0, PWM1	Total of all applicable pins				45	
		ΣIOAL(3)	Ports 0, 1, 2 PWM0, PWM1	Total of all applicable pins				80	
		ΣIOAL(4)	Ports 3, 7 XT2	Total of all applicable pins				15	
		ΣIOAL(5)	UHD+, UHD-	Total of all applicable pins				25	
Allowable power Dissipation		Pd max	QIP48E(14×14)	Ta=-30 to +70°C				400	mW
			SQFP48(7×7)					190	
Operating ambient Temperature		Topr				-30		+70	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Allowable Operating Range at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Operating supply voltage (Note2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245µs ≤tCYC ≤ 200µs		3.0		5.5	V
			0.490µs ≤ tCYC ≤ 200µs Except for onboard programming		2.7		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Port 0, 1, 2, 3 P71 to P73 P70 port input/ interrupt side PWM0, PWM1		2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Port 70 watchdog timer side		2.7 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(3)$	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Port 1, 2, 3 P71 to P73 P70 port input/ interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 0 PWM0, PWM1		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(4)$			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	Port 70 watchdog timer side		2.7 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(6)$	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.245		200	µs
			Except for onboard programming	2.7 to 5.5	0.490		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty= 50±5%	3.0 to 5.5	0.1		12	MHz
			• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty= 50±5%	2.7 to 5.5	0.1		6	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	6MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		6		
	FmRC		Internal RC oscillation	2.7 to 5.5	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.7 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 UHD+, UHD-	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.7 to 5.5			1	µA
	$I_{IH}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 UHD+, UHD-	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.7 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{SS}$	2.7 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.7 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 P71 to P73	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	PWM0, PWM1 P05 (CK0 when using system clock output function)	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(5)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-1mA	2.7 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=2.5mA	2.7 to 5.5			0.4	
	$V_{OL}(4)$	Ports 0, 1, 2 PWM0, PWM1 XT2	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$		I_{OL}=1mA	2.7 to 5.5			0.4	
	$V_{OL}(7)$	Ports 3, 7	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(8)$		I_{OL}=1mA	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 5.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Port 1, 2, 3, 7		2.7 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.7 to 5.5		10		pF

Serial Input/Output Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/reception mode • USB, SIO4 nor SIO9 are not in use simultaneous. • See Fig. 8. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/reception mode • USB is in use simultaneous. • SIO4 nor SIO9 are not in use simultaneous. • See Fig. 8. • (Note 4-1-2)		7			
			tSCKHA(1c)		• Continuous data transmission/reception mode • USB, SIO4 and SIO9 are in use simultaneous. • See Fig. 8. • (Note 4-1-2)		9			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 8.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission/reception mode • USB, SIO4 nor SIO9 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/reception mode • USB is in use simultaneous. • SIO4 nor SIO9 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) +(19/3) tCYC	
			tSCKHA(2c)		• Continuous data transmission/reception mode • USB, SIO4 and SIO9 are in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) +(25/3) tCYC	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Continued on next page.

Continued from preceding page.

Parameter			Symbol	Pin/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.7 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.7 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 8.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 8.		2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.7 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

3. SIO4 Serial I/O Characteristics (Note 4-3-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK4(P24)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• USB, SIO9 nor continuous data transmission/eception mode of SIO0 are not in use simultaneous. • See Fig. 8. • (Note 4-3-2)		4			
			tSCKHA(5b)		• USB is in use simultaneous. • SIO9 nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • See Fig. 8. • (Note 4-3-2)		7			
			tSCKHA(5c)		• USB, SIO9 and continuous data transmission/eception mode of SIO0 are in use simultaneous. • See Fig. 8. • (Note 4-3-2)		12			
	Output clock	Frequency	tSCK(6)	SCK4(P24)	• CMOS output selected • See Fig. 8.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)				1/2			
		High level pulse width	tSCKH(6)				1/2			
			tSCKHA(6a)		• USB, SIO9 nor continuous data transmission/eception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(10/3) tCYC	tCYC
			tSCKHA(6b)		• USB is in use simultaneous. • SIO9 nor continuous data transmission/eception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(19/3) tCYC	
			tSCKHA(6c)		• USB, SIO9 and continuous data transmission/eception mode of SIO0 are in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(6) +(5/3) tCYC		tSCKH(6) +(34/3) tCYC	
Serial input	Data setup time		tsDI(3)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(3)			2.7 to 5.5	0.03			

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: To use serial-clock-input in continuous trans/rec mode, a time from SI4RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Continued on next page.

Continued from preceding page.

Parameter		Symbol	Pin/ Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Serial output	Output delay time	tdD0(5)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	µs

4. SIO9 Serial I/O Characteristics (Note 4-4-1)

Parameter			Symbol	Pin/ Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(7)	SCK9(P27)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(7)				1			
		High level pulse width	tSCKH(7)				1			
			tSCKHA(7a)		• USB, SIO4 nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • See Fig. 8. • (Note 4-4-2)		4			
			tSCKHA(7b)		• USB is in use simultaneous. • SIO4 nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • See Fig. 8. • (Note 4-4-2)		7			
			tSCKHA(7c)		• USB, SIO4 and continuous data transmission/reception mode of SIO0 are in use simultaneous. • See Fig. 8. • (Note 4-4-2)		13			

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: To use serial-clock-input in continuous trans/rec mode, a time from SI9RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Continued on next page.

Continued from preceding page.

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Output clock	Frequency	tSCK(8)	SCK9(P27)	• CMOS output selected • See Fig. 8.	2.7 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
			tSCKHA(8a)		• USB, SIO4 nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(8) +(5/3) tCYC		tSCKH(8) +(10/3) tCYC	tCYC
			tSCKHA(8b)		• USB is in use simultaneous. • SIO4 nor continuous data transmission/reception mode of SIO0 are not in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(8) +(5/3) tCYC		tSCKH(8) +(19/3) tCYC	
			tSCKHA(8c)		• USB, SIO4 and continuous data transmission/reception mode of SIO0 are in use simultaneous. • CMOS output selected • See Fig. 8.		tSCKH(8) +(5/3) tCYC		tSCKH(8) +(37/3) tCYC	
Serial input	Data setup time		tsDI(4)	SO9(P25), SI9(P26)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(4)			2.7 to 5.5	0.03			
Serial output	Output delay time		tdD0(6)	SO9(P25), SI9(P26)	• Must be specified with respect to rising edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	

Pulse Input Conditions at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tP1H(1) tP1L(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.7 to 5.5	200			µs

AD Converter Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.49µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0. 294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	47.04 (tCYC= 0. 735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHzside	4.5 to 5.5		9.3	23	mA
	IDDOP(2)		• Internal PLL oscillation stopped • Internal RC oscillation stopped • 1/1 frequency division ration	3.0 to 3.6		5.3	13	
	IDDOP(3)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side	4.5 to 5.5		12	28	
	IDDOP(4)		• Internal PLL oscillation mode • Internal RC oscillation stopped • 1/1 frequency division ration	3.0 to 3.6		6.4	16	
	IDDOP(5)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side	4.5 to 5.5		6.1	15	
	IDDOP(6)		• Internal RC oscillation stopped • 1/2 frequency division ration	3.0 to 3.6		3.5	8.2	
	IDDOP(7)			2.7 to 3.0		2.9	6.4	
	IDDOP(8)		• FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration	4.5 to 5.5		0.68	3.3	
	IDDOP(9)			3.0 to 3.6		0.36	1.6	
	IDDOP(10)			2.7 to 3.0		0.30	1.2	
	IDDOP(11)		• FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		40	160	μA
	IDDOP(12)			3.0 to 3.6		17	64	
	IDDOP(13)			2.7 to 3.0		13	46	
HALT mode consumption current (Note 7-1)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		4.2	10	mA
	IDDHALT(2)			3.0 to 3.6		2.3	5.5	
	IDDHALT(3)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode • Internal RC oscillation stopped • 1/1 frequency division ration	4.5 to 5.5		6.1	15	
	IDDHALT(4)			3.0 to 3.6		3.3	7.9	
	IDDHALT(5)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		2.6	6.4	
	IDDHALT(6)			3.0 to 3.6		1.4	3.3	
	IDDHALT(7)			2.7 to 3.0		1.2	2.6	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(8)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ration	4.5 to 5.5		0.37	1.8	mA
	IDDHALT(9)			3.0 to 3.6		0.18	0.84	
	IDDHALT(10)			2.7 to 3.0		0.15	0.63	
	IDDHALT(11)		• HALT mode • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • 1/2 frequency division ration	4.5 to 5.5		25	102	µA
	IDDHALT(12)			3.0 to 3.6		7.6	32	
	IDDHALT(13)			2.7 to 3.0		5.4	20	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.10	24	
	IDDHOLD(2)			3.0 to 3.6		0.04	15	
	IDDHOLD(3)			2.7 to 3.0		0.03	12	
Timer HOLD mode consumption current	IDDHOLD(4)		Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		21	88	
	IDDHOLD(5)			3.0 to 3.6		5.0	23	
	IDDHOLD(6)			2.7 to 3.0		3.2	14	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

USB Characteristics and Timing at Ta=0 to +70°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
High level output	$V_{OH(USB)}$	• 15 kΩ±5% to GND	2.8		3.6	V
Low level output	V_{OL}(USB)	• 1.5 kΩ±5% to 3.6 V	0.0		0.3	V
Output signal crossover voltage	V_{CRS}		1.3		2.0	V
Differential input sensitivity	V_{DI}	• |(UHD+)-(UHD-)|	0.2			V
Differential input common mode range	V_{CM}		0.8		2.5	V
High level input	V_{IH}(USB)		2.0			V
Low level input	V_{IL}(USB)				0.8	V
USB data rise time	t_R	• R_S=33Ω,C_L=50pF	4		20	ns
USB data fall time	t_F	• R_S=33Ω,C_L=50pF	4		20	ns

F-ROM Programming Characteristics at Ta = -10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU current	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing	3.0 to 5.5		20	30	ms
	tFW(2)		• Programming			40	60	µs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
6MHz	MURATA	CSTCR6M00G15***-R0	(39)	(39)	1k	2.7 to 5.5	0.10	0.50	Built in C1, C2
8MHz	MURATA	CSTCE8M00G15***-R0	(33)	(33)	680	3.0 to 5.5	0.10	0.50	
10MHz	MURATA	CSTCE10M0G15***-R0	(33)	(33)	470	3.0 to 5.5	0.10	0.50	
12MHz	MURATA	CSTCE12M0G15***-R0	(33)	(33)	470	3.0 to 5.5	0.10	0.50	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	510k	2.7 to 5.5	1.1	3.0	Applicable CL value= 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

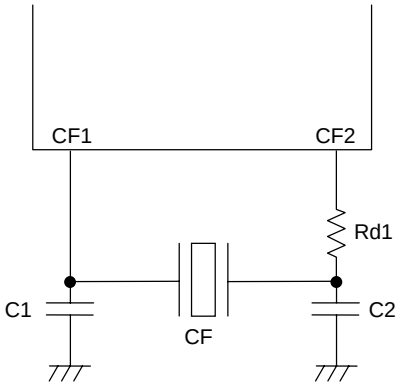


Figure 1 CF Oscillator Circuit

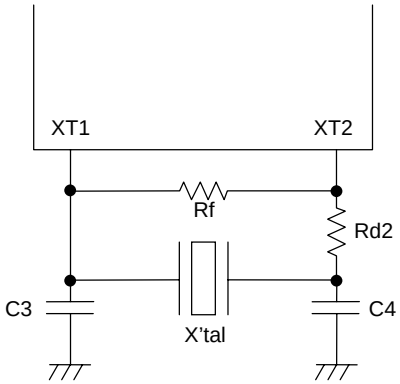


Figure 2 XT Oscillator Circuit

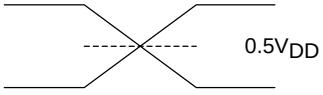
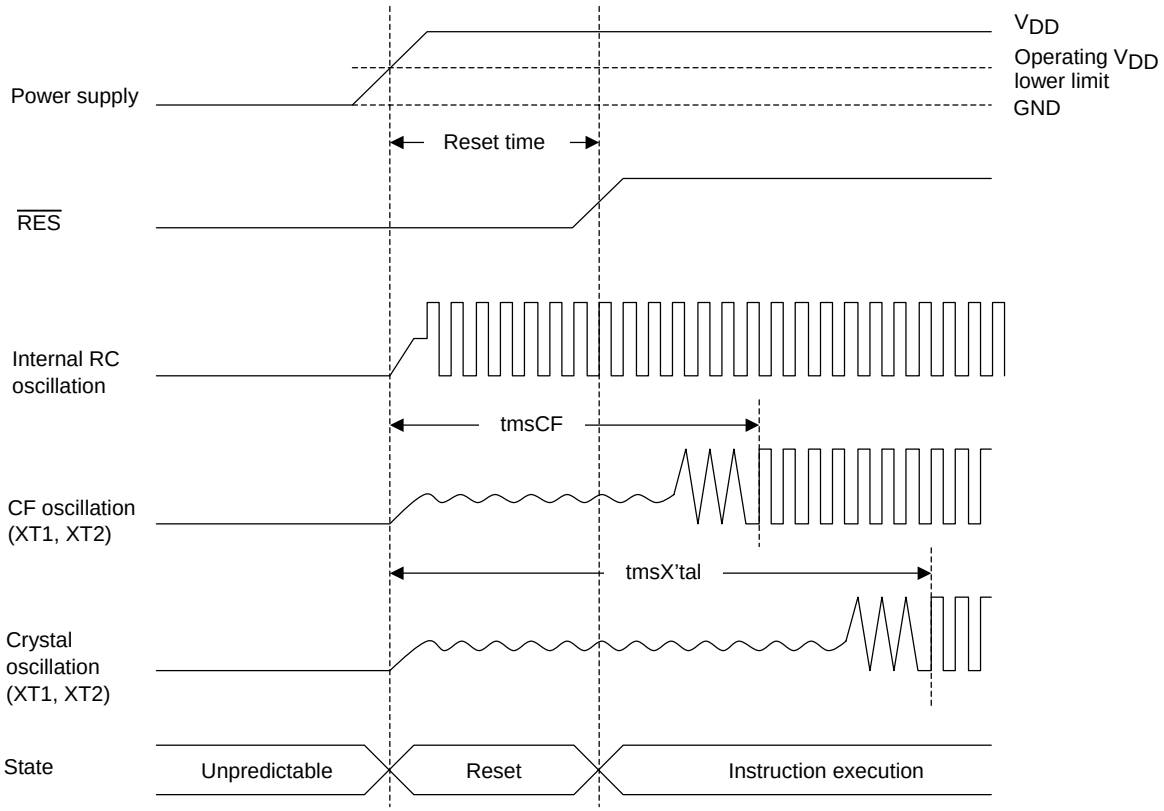
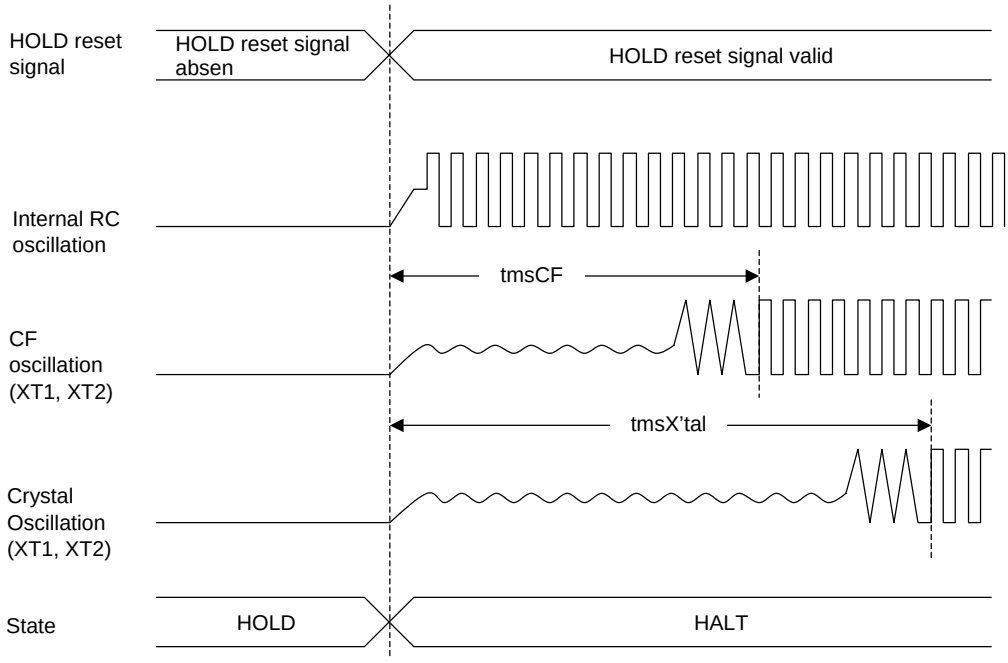


Figure 3 AC Timing Measurement Point

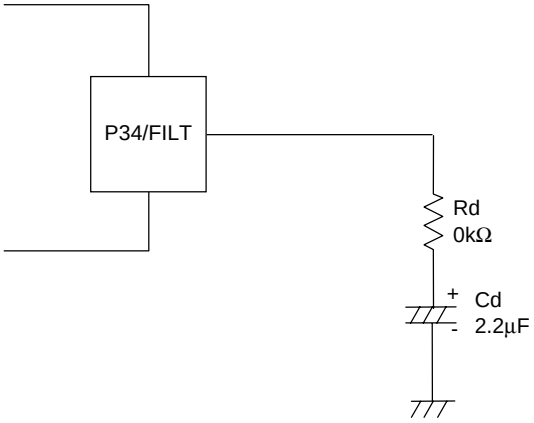


Reset Time and Oscillation Stabilization Time



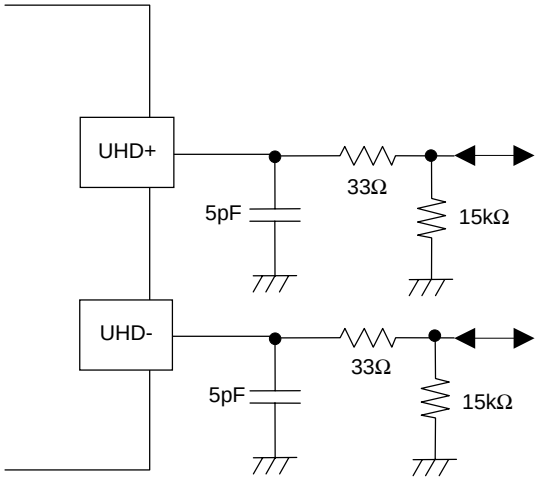
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



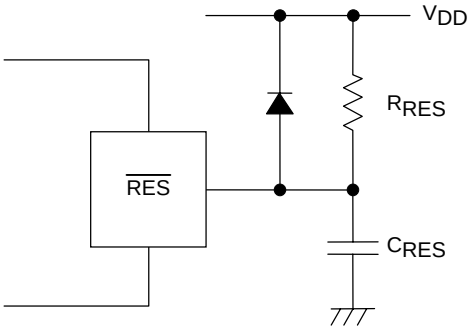
When using the internal PLL circuit to generate the 48MHz clock for USB, it is necessary to connect a filter circuit such as that shown to the left to the P34/FILT pin.

Figure 5 Filter Circuit for the Internal PLL Circuit



Note:
It’s necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit each mounting board.

Figure 6 USB Port Peripheral Circuit



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 7 Reset Circuit

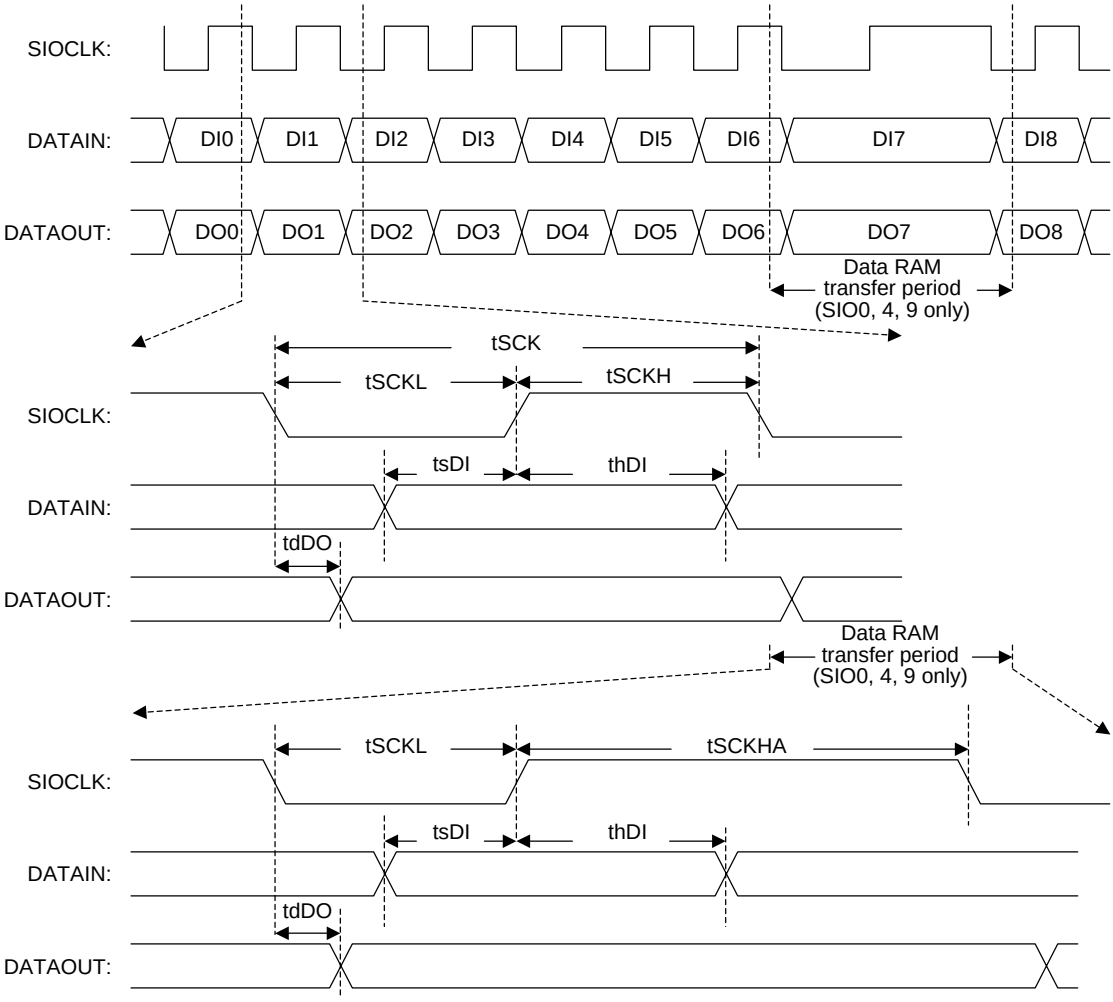


Figure 8 Serial I/O Output Waveforms

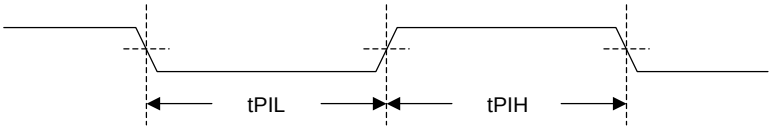


Figure 9 Pulse Input Timing Signal Waveform

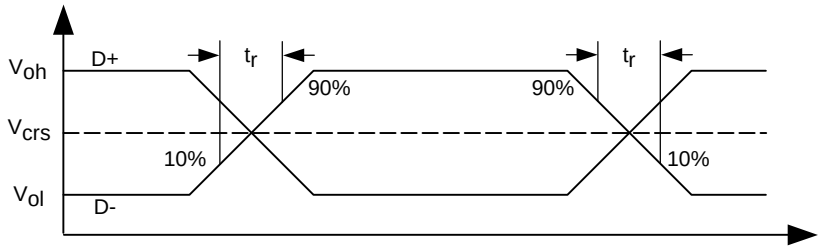


Figure 10 USB Data Signal Timing and Voltage Level