CS5376A

Low-power, Multi-channel Decimation Filter

Features

- 1- to 4-channel Digital Decimation Filter
  - Multiple On-chip FIR and IIR Coefficient Sets
  - Programmable Coefficients for Custom Filters
  - Synchronous Operation
- Selectable Output Word Rate
  - 4000, 2000, 1000, 500, 333, 250 SPS
  - 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS
- Digital Gain and Offset Corrections
- Test DAC Bit Stream Generator
  - Sine Wave or Impulse Output Mode
- Time Break Controller, General Purpose I/O
- Secondary SPI™ Port, Boundary Scan JTAG
- Microcontroller or EEPROM Configuration
- Small-footprint, 64-pin TQFP Package
- Low Power Consumption
  - 9 mW per Channel at 500 SPS
- Flexible Power Supplies
  - I/O Interface: 3.3 V or 5.0 V
  - Digital Logic Core: 3.0 V, 3.3 V or 5.0 V

Description

The CS5376A is a multi-function digital filter utilizing a low-power signal processing architecture to achieve efficient filtering for up to four ΔΣ modulators. By combining the CS5376A with CS3301/02 differential amplifiers, CS5371/72 ΔΣ modulators, and the CS4373A ΔΣ test DAC a synchronous, high-resolution, self-testing, multi-channel measurement system can be designed quickly and easily.

Digital filter coefficients for the CS5376A FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400 mHz when using the on-chip coefficient sets.

The CS5376A includes integrated peripherals to simplify system design: offset and gain corrections, a test DAC bit stream generator, a time-break controller, 12 general-purpose I/O pins, a secondary SPI port, and a boundary scan JTAG port.

ORDERING INFORMATION

See page 107.

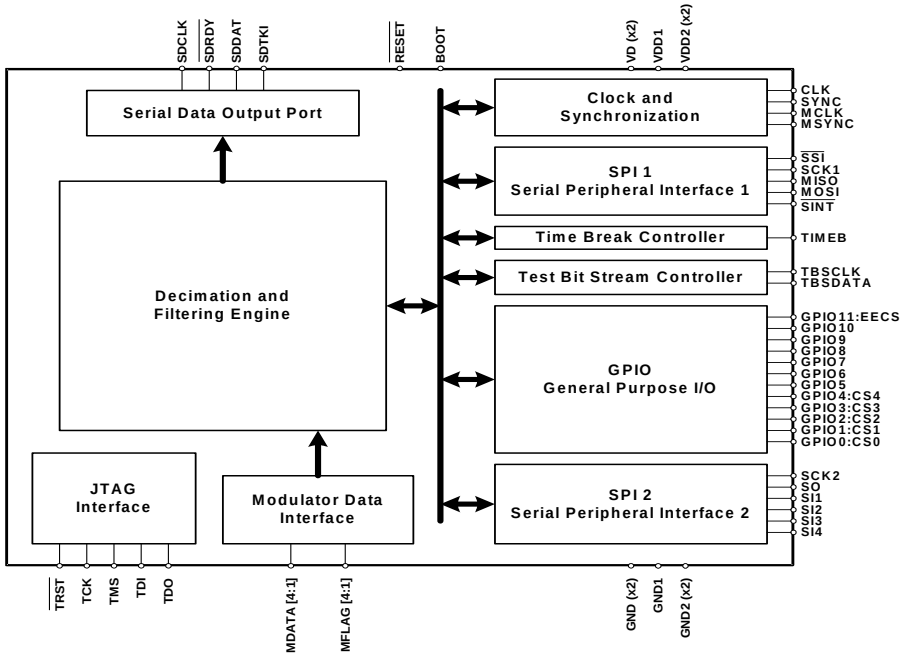


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

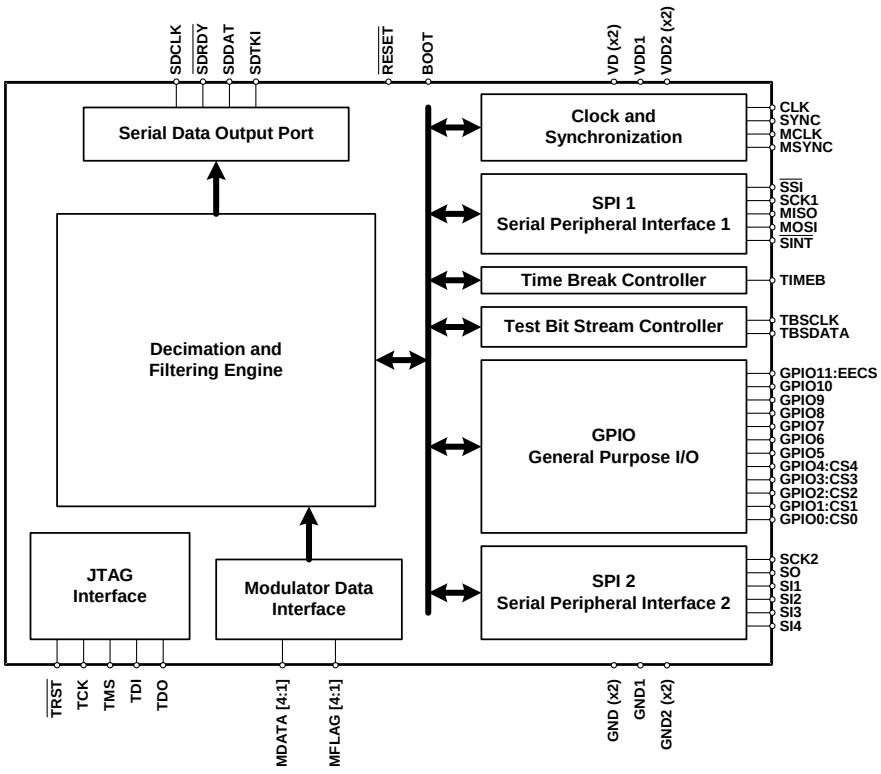


Figure 1. CS5376A Block Diagram

1. GENERAL DESCRIPTION

The CS5376A is a multi-channel digital filter with integrated system peripherals. Figure 1 illustrates a simplified block diagram of the CS5376A.

1.1 Digital Filter Features

- Multi-channel decimation filter for CS5371/72 ΔΣ modulators.
  - 1, 2, 3, or 4 channel concurrent operation.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - Internal synchronization of digital filter phase to an external SYNC signal.
- Multiple output word rates, including low bandwidth rates.
  - Standard output rates: 4000, 2000, 1000, 500, 333, 250 SPS.
  - Low bandwidth rates: 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS.
- Flexible digital filter configuration. (See Figure 2)
  - Cascaded SINC, FIR, and IIR filters with selectable output stage.
  - Linear and minimum phase FIR low-pass filter coefficients included.
  - 3 Hz Butterworth IIR high-pass filter coefficients included.
  - FIR and IIR coefficients are programmable to create a custom filter response.
- Digital gain correction.
  - Individual channel gain correction to normalize signal amplitudes.

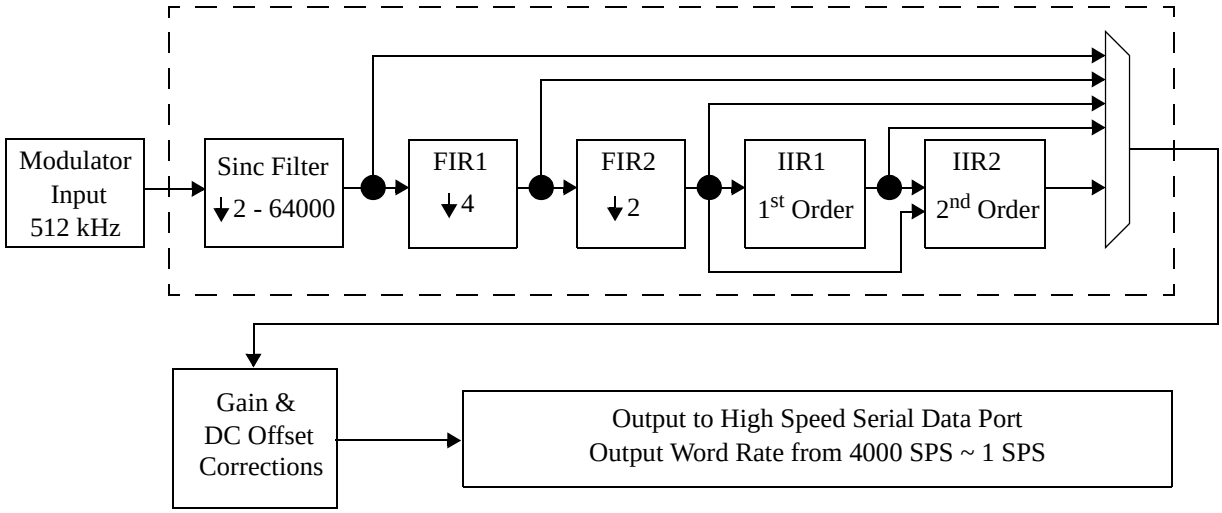


Figure 2. Digital Filtering Stages

- Digital offset correction and calibration.
  - Individual channel offset correction to remove measurement offsets.
  - Calibration engine for automatic calculation of offset correction factors.

1.2 Integrated Peripheral Features

- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - MCLK / MSYNC output signals to synchronize external components.
- High speed serial data output port (SD port).
  - Asynchronous operation to 4 MHz for direct connection to system telemetry.
  - Internal 8-deep data FIFO for flexible output timing.
- Digital test bit stream signal generator suitable for CS4373A ΔΣ test DAC.
  - Sine wave output mode for testing total harmonic distortion.
  - Impulse output mode for transfer function characterization.
  - Programmable waveform data for custom test signal generation.
- Time break controller to record system timing information.
  - Dedicated TB status bit in the output data stream.
  - Programmable output delay to match system group delay.
- Additional hardware peripherals simplify system design.
  - 12 General Purpose I/O (GPIO) pins for local hardware control.
  - Secondary SPI 2 serial port to control local serial peripherals.
  - JTAG port for boundary scan (IEEE 1149.1 compliant).

1.3 System Level Features

- Flexible configuration options.
  - Configuration 'on-the-fly' via microcontroller or system telemetry.
  - Fixed configuration via stand-alone boot

EEPROM.

- Low power consumption.
  - 37 mW for 4-channel operation at 500 SPS (9.25 mW/channel).
  - 40 µW standby mode.
- Flexible power supply configurations.
  - Separate digital logic core, telemetry I/O, and modulator I/O power supplies.
  - Telemetry I/O and modulator I/O interfaces operate from 3.3 V or 5 V.
  - Digital logic core operates from 3.0 V, 3.3 V or 5 V.
- Small 64-pin TQFP package.
  - Total footprint 12 mm x 12 mm plus five bypass capacitors.

1.4 Configuration Interface

- Configuration from microcontroller or stand-alone boot EEPROM.
  - Microcontroller boot permits reconfiguration during operation.
  - EEPROM boot sets a fixed operational configuration.
- Configuration commands written through Serial Peripheral Interface 1. (See Table 1)
  - Standardized microcontroller interface using SPI 1 registers. (See Table 3)
  - Commands write digital filter registers, filter coefficients, and test bit stream data.
  - Digital filter registers set hardware configuration options.

Microcontroller Boot Configuration Commands

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
WRITE TBS DATA	000006	NUM TBS (TBS DATA)	- (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	000007	-	-	Use On-Chip TBS Data
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

EEPROM Boot Configuration Commands

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
WRITE TBS DATA	05	NUM TBS (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	06	-	Use On-Chip TBS Data
FILTER START	07	-	Start Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 1. Microcontroller and EEPROM Configuration Commands

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 3. FIR and IIR Coefficient Set Selection Word

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 2. TBS Configurations Using On-Chip Data

SPI 1 Registers

Name	Addr.	Type	# Bits	Description
SPI1CTRL	00 - 02	R/W	8, 8, 8	SPI 1 Control
SPI1CMD	03 - 05	R/W	8, 8, 8	SPI 1 Command
SPI1DAT1	06 - 08	R/W	8, 8, 8	SPI 1 Data 1
SPI1DAT2	09 - 0B	R/W	8, 8, 8	SPI 1 Data 2

Digital Filter Registers

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG0	0E	R/W	24	GPIO[7:0] Direction, Pull-up Enable, and Data
GPCFG1	0F	R/W	24	GPIO[11:8] Direction, Pull-up Enable, and Data
SPI2CTRL	10	R/W	24	SPI 2 Control
SPI2CMD	11	R/W	16	SPI 2 Command
SPI2DAT	12	R/W	24	SPI 2 Data
RESERVED	13-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN1	21	R/W	24	Gain Correction Channel 1
GAIN2	22	R/W	24	Gain Correction Channel 2
GAIN3	23	R/W	24	Gain Correction Channel 3
GAIN4	24	R/W	24	Gain Correction Channel 4
OFFSET1	25	R/W	24	Offset Correction Channel 1
OFFSET2	26	R/W	24	Offset Correction Channel 2
OFFSET3	27	R/W	24	Offset Correction Channel 3
OFFSET4	28	R/W	24	Offset Correction Channel 4
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

Table 3. SPI 1 and Digital Filter Registers

2. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- GND, GND1, GND2 = 0 V, all voltages with respect to 0 V.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Logic Core Power Supply		VD	2.85	3.0	5.25	V
Microcontroller Interface Power Supply		VDD1	3.135	3.3	5.25	V
Modulator Interface Power Supply		VDD2	3.135	3.3	5.25	V
Ambient Operating Temperature	Industrial (-IQ)	T_A	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies	Logic Core	VD	-0.3	6.0	V
	Microcontroller Interface	VDD1	-0.3	6.0	V
	Modulator Interface	VDD2	-0.3	6.0	V
Input Current, Any Pin Except Supplies	(Note 1)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 1)	I_{IN}	-	±50	mA
Output Current	(Note 1)	I_{OUT}	-	±25	mA
Power Dissipation		P_{DN}	-	500	mW
Digital Input Voltages		V_{IND}	-0.5	VDD+0.5	V
Ambient Operating Temperature (Power Applied)		T_A	-40	85	°C
Storage Temperature Range		T_{STG}	-65	150	°C

1. Transient currents up to 100 mA will not cause SCR latch-up.

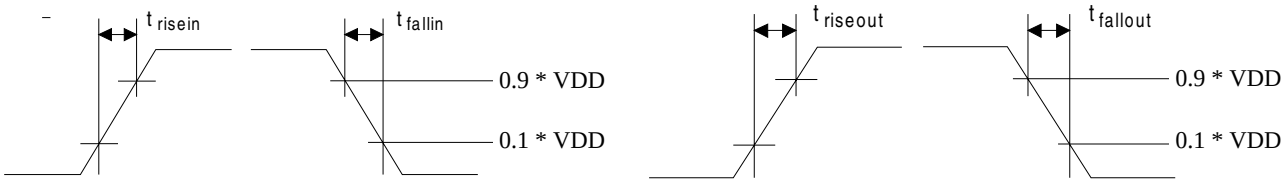
THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature	T_J	-	-	135	°C
Junction to Ambient Thermal Impedance	Θ_{JA}	-	65		°C / W
Ambient Operating Temperature (Power Applied)	T_A	-40	-	+85	°C

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Drive Voltage		V_{IH}	0.6 * VDD	-	VDD	V
Low-Level Input Drive Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Drive Voltage	I_{out} = -40 µA	V_{OH}	VDD - 0.3	-	VDD	V
Low-Level Output Drive Voltage	I_{out} = +40 µA	V_{OL}	0.0	-	0.3	V
Rise Times, Digital Inputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs		t_{FALL}	-	-	100	ns
Rise Times, Digital Outputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Outputs		t_{FALL}	-	-	100	ns
Input Leakage Current	(Note 2)	I_{IN}	-	± 1	± 10	µA
3-State Leakage Current		I_{OZ}	-	-	± 10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Pin Capacitance		C_{OUT}	-	9	-	pF

Notes: 2. Max leakage for pins with pull-up resistors ($\overline{TRST}$, TMS, TDI, $\overline{SSI}$, GPIO, MOSI, SCK1) is ±250 µA.



POWER CONSUMPTION

Parameter	Symbol	Min	Typ	Max	Unit
Operational Power Consumption					
1.024 MHz Digital Filter Clock	PWR_1	-	21	-	mW
2.048 MHz Digital Filter Clock	PWR_2	-	26	-	mW
4.096 MHz Digital Filter Clock	PWR_4	-	37	-	mW
8.192 MHz Digital Filter Clock	PWR_8	-	57	-	mW
16.384 MHz Digital Filter Clock	PWR_{16}	-	85	-	mW
Standby Power Consumption					
32 kHz Digital Filter Clock, Filter Stopped	PWR_S	-	40	-	µW

SWITCHING CHARACTERISTICS

SPI 1 Interface Timing (External Master)

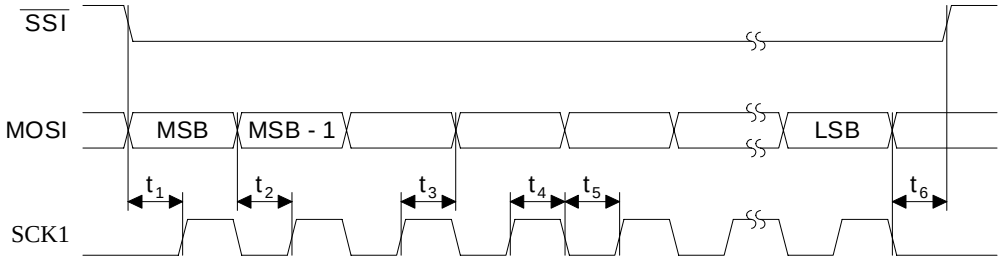


Figure 4. MOSI Write Timing in SPI Slave Mode

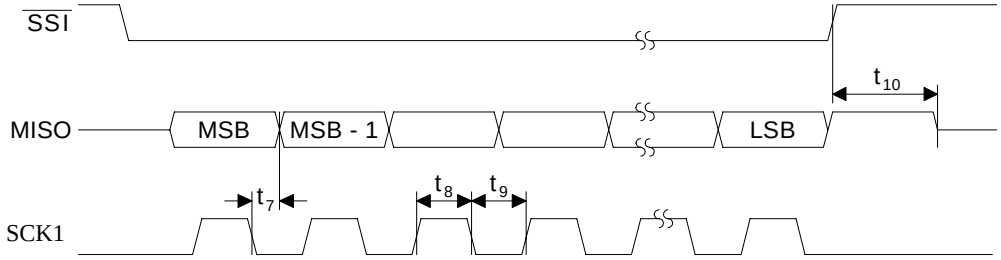


Figure 5. MISO Read Timing in SPI Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
MOSI Write Timing					
$\overline{SSI}$ Enable to Valid Latch Clock	t_1	60	-	-	ns
Data Set-up Time Prior to SCK1 Rising	t_2	60	-	-	ns
Data Hold Time After SCK1 Rising	t_3	120	-	-	ns
SCK1 High Time	t_4	120	-	-	ns
SCK1 Low Time	t_5	120	-	-	ns
SCK1 Falling Prior to $\overline{SSI}$ Disable	t_6	60	-	-	ns
MISO Read Timing					
SCK1 Falling to New Data Bit	t_7	-	-	200	ns
SCK1 High Time	t_8	120	-	-	ns
SCK1 Low Time	t_9	120	-	-	ns
$\overline{SSI}$ Rising to MISO Hi-Z	t_{10}	-	-	150	ns

SWITCHING CHARACTERISTICS

Serial Data Port (SD Port)

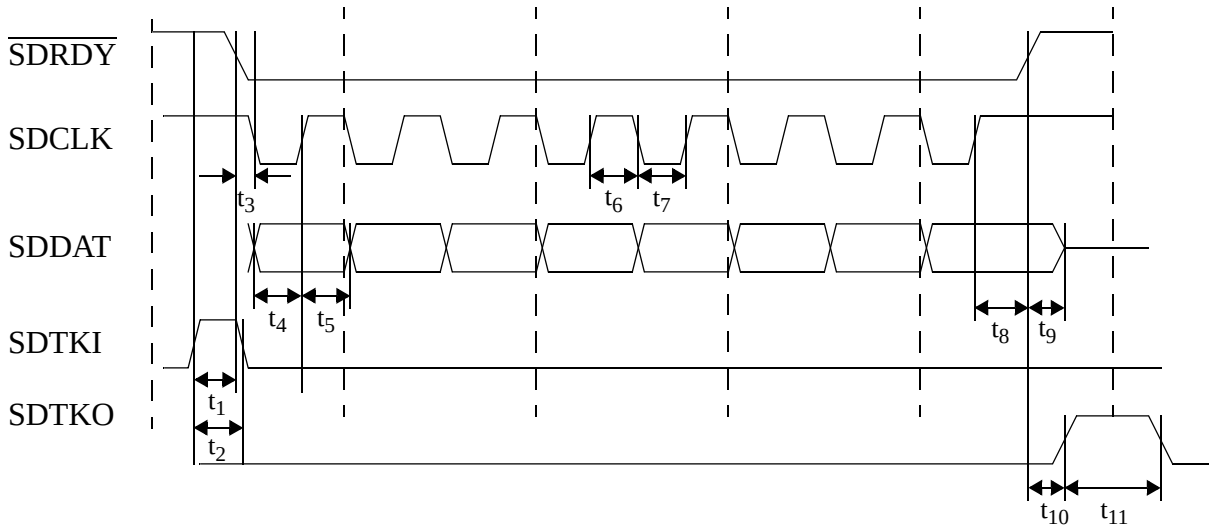
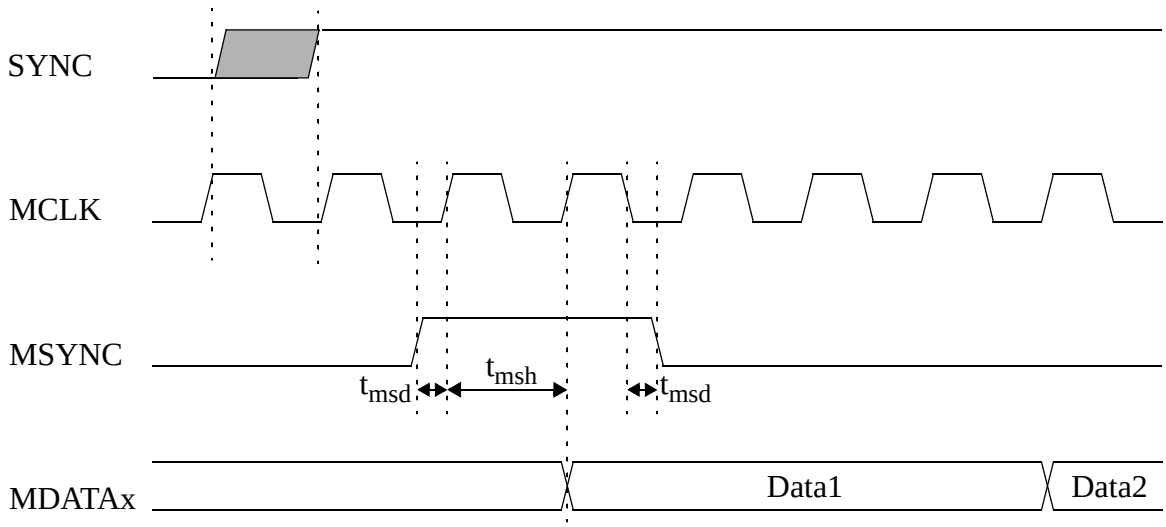


Figure 6. SD Port Read Timing

Parameter	Symbol	Min	Typ	Max	Unit
SDTKI to $\overline{\text{SDRDY}}$ Falling Edge	t_1	60	-	-	ns
SDTKI High Time Width	t_2	60	-	1000	ns
$\overline{\text{SDRDY}}$ Falling Edge to SDCLK Falling Edge	t_3	50	-	-	ns
Data Setup Time Prior to SDCLK Rising	t_4	60	-	-	ns
Data Hold Time After SDCLK Rising	t_5	60	-	-	ns
SDCLK High Time	t_6	120	-	-	ns
SDCLK Low Time	t_7	120	-	-	ns
SDCLK Rising to $\overline{\text{SDRDY}}$ Rising	t_8	60	-	-	ns
Data Hold Time After $\overline{\text{SDRDY}}$ Rising	t_9	-	-	150	ns
$\overline{\text{SDRDY}}$ High to SDTKO Rising Edge	t_{10}	-	-	60	ns
SDTKO High Time	t_{11}	90	-	-	ns

SWITCHING CHARACTERISTICS

CLK, SYNC, MCLK, MSYNC, and MDATAx



Note: SYNC input latched on MCLK rising edge. MSYNC output triggered by MCLK falling edge.

f_{MCLK}	2.048 MHz	1.024 MHz
$t_{msd} = T_{MCLK} / 4$	t_{msd} = 122 ns	t_{msd} = 244 ns
$t_{msh} = T_{MCLK}$	t_{msh} = 488 ns	t_{msh} = 976 ns

Figure 7. SYNC, MCLK, MSYNC, MDATA Interface Timing

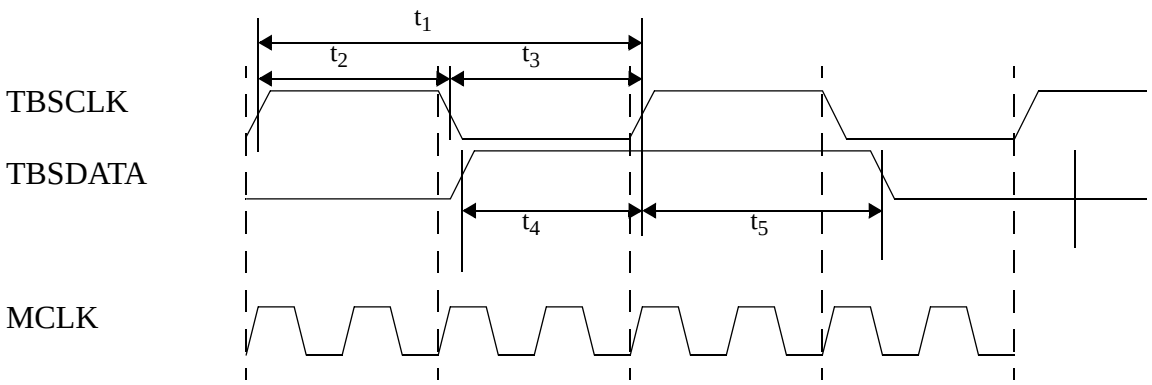
Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 3)	CLK	32	32.768	33	MHz
Master Clock Duty Cycle		DTY	40	-	60	%
Master Clock Rise Time		t_{RISE}	-	-	20	ns
Master Clock Fall Time		t_{FALL}	-	-	20	ns
Master Clock Jitter		JTR	-	-	300	ps
Synchronization after SYNC rising	(Note 4)	SYNC	-2	-	2	µs
MSYNC Setup Time to MCLK rising		t_{msr}	20	-	-	ns
MCLK rising to Valid MDATA		t_{mdv}	-	-	75	ns
MSYNC falling to MCLK rising		t_{msf}	20	-	-	ns

Notes: 3. Master clock frequencies above or below 32.768 MHz will affect generated clock frequencies.

4. Sampling synchronization between multiple CS5376A devices receiving identical SYNC signals.

SWITCHING CHARACTERISTICS

Test Bit Stream (TBS)



Note: Example timing shown for a 256 kHz output rate and no programmable delays.

Figure 8. TBS Output Clock and Data Timing

Parameter		Symbol	Min	Typ	Max	Unit
TBS Clock Timing						
TBS Clock Period		t_1	-	3.906	-	µs
TBS Clock High Time	(Note 5)	t_2	40	-	60	%
TBS Clock Low Time		t_3	40	-	60	%
TBS Data Output Timing						
TBS Data Bit Rate			-	256	-	kbps
TBS Data Rising to TBS Clock Rising Setup Time		t_4	60	-	-	ns
TBS Clock Rising to TBS Data Falling Hold Time	(Note 6)	t_5	60	-	-	ns

5. TBSCLK phase can be delayed in 1/8 increments. The timing diagram shows no TBSCLK delay.
6. TBSDATA can be delayed from 0 to 63 full bit periods. The timing diagram shows no TBSDATA delay.

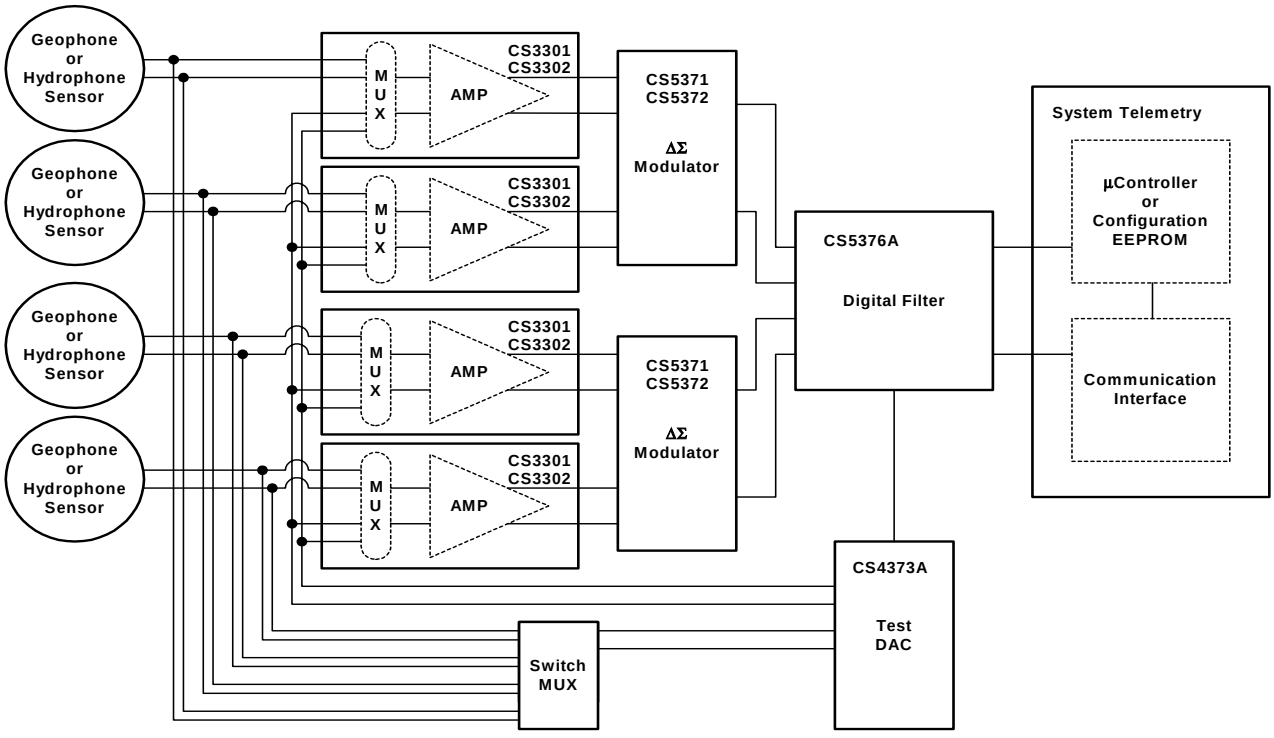


Figure 9. Multi-Channel System Block Diagram

3. SYSTEM DESIGN WITH CS5376A

Figure 9 illustrates a simplified block diagram of the CS5376A in a multi-channel measurement system.

Up to four differential sensors are connected through CS3301/02 differential amplifiers to the CS5371/72 ΔΣ modulators, where analog to digital conversion occurs. Each modulators 1-bit output connects to a CS5376A MDATA input, where the oversampled ΔΣ data is decimated and filtered to 24-bit output samples at a programmed output rate. These output samples are buffered in an 8-deep data FIFO and passed to the system telemetry on command.

System self tests are performed by connecting the CS5376A test bit stream (TBS) generator to the CS4373A test DAC. Analog tests drive differential signals from the CS4373A test DAC into the multiplexed inputs of the CS3301/02 amplifiers or directly to the sensors through external analog switches. Digital loopback tests internally connect the TBS digital output directly to the CS5376A modulator inputs.

3.1 Power Supplies

The multi-channel system shown in Figure 9 typically operates from a ±2.5 V analog power supply and a 3.3 V digital power supply. The CS5376A logic core can be powered from 3 V to minimize power consumption, if required.

3.2 Reset Control

System reset is required only for the CS5376A device, and is a standard active low signal that can be generated by a power supply monitor or microcontroller. Other system devices default to a power-down state when the CS5376A is reset.

3.3 Clock Generation

A single 32.768 MHz low-jitter clock input, which can be generated from a VCXO based PLL, is required to drive the CS5376A device. Clock inputs for other system devices are driven by clock outputs from the CS5376A.

3.4 Synchronization

Digital filter phase and analog sample timing of the four ΔΣ modulators connected to the CS5376A are synchronized by a rising edge on the SYNC pin. If a synchronization signal is received identically by all CS5376A devices in a measurement network, synchronous sampling across the network is guaranteed.

3.5 System Configuration

Through the SPI 1 serial port, filter coefficients and digital filter register settings can either be programmed by a microcontroller or automatically loaded from an external EEPROM after reset. System configuration is only required for the CS5376A device, as other devices are configured via the CS5376A General Purpose I/O pins.

Two registers in the digital filter, SYSTEM1 and SYSTEM2 (0x2C, 0x2D), are provided for user defined system information. These are general purpose registers that will hold any 24-bit data values written to them.

3.6 Digital Filter Operation

After analog to digital conversion occurs in the modulators, the oversampled 1-bit ΔΣ data is read into the CS5376A through the MDATA pins. The digital filter then processes data through the enabled filter stages, decimating it to 24-bit words at a programmed output word rate. The final 24-bit samples are concatenated with 8-bit status words and placed into an output FIFO.

3.7 Data Collection

Data is collected from the CS5376A through the Serial Data port (SD port). Automatically or upon request, depending how the SDTKI pin is connected, the SD port initiates serial transactions to transfer 32-bit data from the output FIFO to the system telemetry. The output FIFO has eight data locations to permit latency in data collection.

3.8 Integrated peripherals

Test Bit Stream (TBS)

A digital signal generator built into the CS5376A produces a 1-bit ΔΣ sine wave or impulse function. This digital test bit stream can be connected to the CS4373A test DAC to create high quality analog test signals or it can be internally looped back to the CS5376A MDATA inputs to test the digital filter and data collection circuitry.

Time Break

Timing information is recorded during data collection by strobing the TIMEB pin. A dedicated flag in the sample status bits, TB, is set high to indicate over which measurement the timing event occurred.

General Purpose I/O (GPIO)

Twelve general purpose pins are available on the CS5376A for system control. Each pin can be set as input or output, high or low, with an internal pull-up enabled or disabled. The CS3301/02, CS5371/72 and CS4373A devices in Figure 9 are configured by simple pin settings controlled through the CS5376A GPIO pins.

Serial Peripheral Interface 2 (SPI 2)

A secondary master mode serial port to communicate with external serial peripherals.

JTAG Port

Boundary scan JTAG is IEEE 1149.1 compliant.

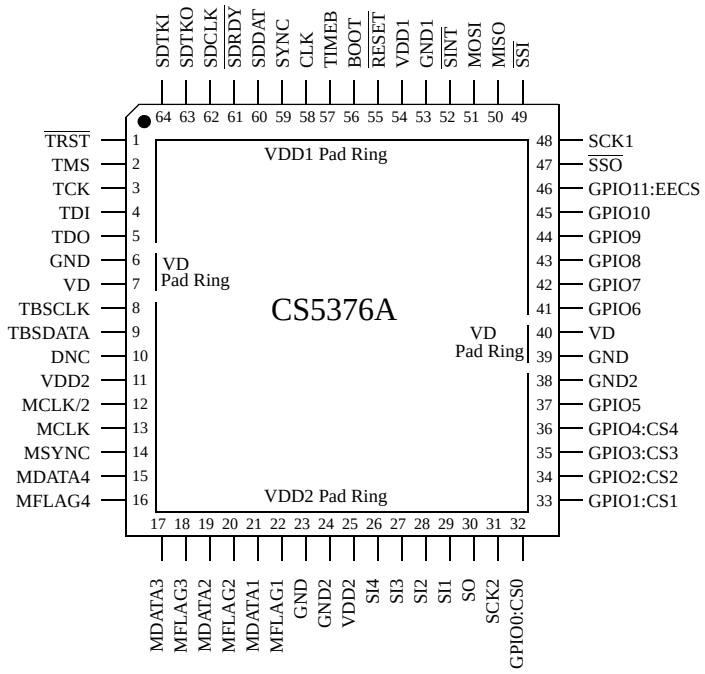


Figure 10. Power Supply Block Diagram

4. POWER SUPPLIES

The CS5376A has three sets of power supply inputs. Two sets supply power to the I/O pins of the device (VDD1, VDD2), and the third supplies power to the logic core (VD). The I/O pin power supplies determine the maximum input and output voltages when interfacing to peripherals, and the logic core power supply largely determines the power consumption of the CS5376A.

4.1 Pin Descriptions

VDD1, GND1 - Pins 54,53

Sets the interface voltage to a microcontroller and system telemetry. Can be driven with voltages from 3.3 V to 5 V.

VDD1 powers pins 1-5 and 41-64:

$\overline{\text{TRST}}$, TMS, TCK, TDI, TDO

GPIO6 - GPIO11:EECS

$\overline{\text{SSO}}$, SCK1, $\overline{\text{SSI}}$, MISO, MOSI, $\overline{\text{SINT}}$,

$\overline{\text{RESET}}$, BOOT, TIMEB, CLK, SYNC

SDDAT, $\overline{\text{SDRDY}}$, SDCLK, SDTKO, SDTKI

VDD2, GND2 - Pins 11, 25, 24, 38

Sets the interface voltage to the modulators, test DAC, and serial peripherals. Can be driven with voltages from 3.3 V to 5 V.

VDD2 powers pins 8-37:

TBSCLK, TBSDATA

MCLK/2, MCLK, MSYNC

MDATA1 - MDATA4

MFLAG1 - MFLAG4

SI1 - SI4, SO, SCK2

GPIO0:CS0 - GPIO5

VD, GND - Pins 7, 40, 6, 23, 39

Sets the operational voltage of the CS5376A logic core. Can be driven with voltages from 3 V to 5 V. A 3 V supply minimizes total power consumption.

4.2 Bypass Capacitors

Each power supply pin should be bypassed with parallel 1 µF and 0.01 µF caps, or by a single 0.1 µF cap, placed as close as possible to the CS5376A. Bypass capacitors should be ceramic (X7R, C0G), tantalum, or other good quality dielectric type.

4.3 Power Consumption

Power consumption of the CS5376A depends primarily on the power supply voltage of the logic core (VD) and the programmed digital filter clock rate. Digital filter clock rates are selected based on the required output word rate as explained in “Digital Filter Initialization” on page 41.

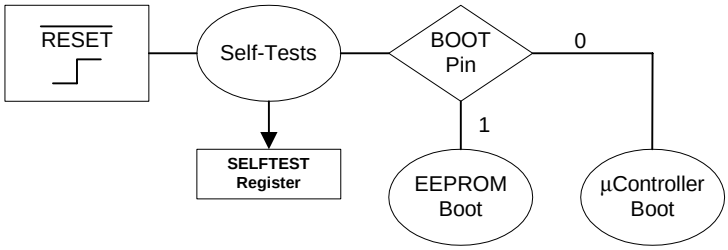


Figure 11. Reset Control Block Diagram

5. RESET CONTROL

The CS5376A reset signal is active low. When released, a series of self-tests are performed and the device either actively boots from an external EEPROM or enters an idle state waiting for microcontroller configuration.

5.1 Pin Descriptions

$\overline{\text{RESET}}$ - Pin 55

Reset input, active low.

BOOT - Pin 56

Boot mode select, latched following a $\overline{\text{RESET}}$ rising edge.

BOOT = 1 = EEPROM boot

BOOT = 0 = Microcontroller boot

5.2 Reset Self-Tests

After $\overline{\text{RESET}}$ is released but before booting, a series of digital filter self-tests are run. Results are combined into the SELFTEST register (0x2F), with 0x0AAAAA indicating all passed. Self-tests require 60 ms to complete, after which configuration commands are serviced.

Self-Test Type	Pass Code	Fail Code
Program ROM	0x00000A	0x00000F
Data ROM	0x0000A0	0x0000F0
Program RAM	0x000A00	0x000F00
Data RAM	0x00A000	0x00F000
Execution Unit	0x0A0000	0x0F0000

5.3 Boot Configurations

The logic state of the BOOT pin after reset determines if the CS5376A actively reads configuration information from EEPROM or enters an idle state waiting for a microcontroller to write configuration commands.

EEPROM Boot

When the BOOT pin is high after reset, the CS5376A actively reads data from an external serial EEPROM and then begins operation in the specified configuration. Configuration commands and data are encoded in the EEPROM as specified in the ‘Configuration By EEPROM’ section of this data sheet, starting on page 26.

Microcontroller Boot

When the BOOT pin is low after reset, the CS5376A enters an idle state waiting for a microcontroller to write configuration commands and initialize filter operation. Configuration commands and data are written as specified in the ‘Configuration By Microcontroller’ section of this data sheet, starting on page 32.

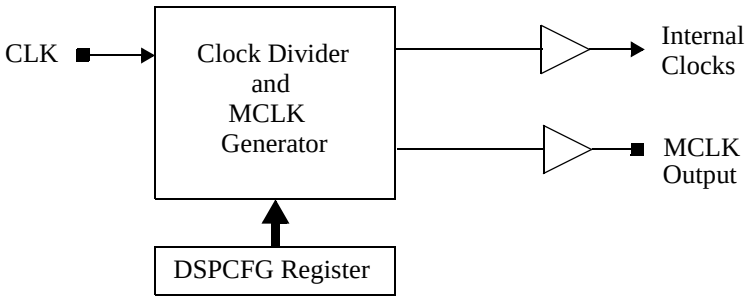


Figure 12. Clock Generation Block Diagram

6. CLOCK GENERATION

The CS5376A requires a 32.768 MHz master clock input, which is used to generate internal digital filter clocks and external modulator clocks.

6.1 Pin Description

CLK - Pin 58

Clock input, nominal frequency 32.768 MHz.

6.2 Synchronous Clocking

To guarantee synchronous measurements throughout a sensor network, the CS5376A master clock should be distributed to arrive at all nodes in phase. The 32.768 MHz master clock can either be directly distributed through the system telemetry, or reconstructed locally using a VCXO based PLL. To ensure recovered clocks have identical phase, system PLL designs should use a phase/frequency detector architecture.

6.3 Master Clock Jitter and Skew

Care must be taken to minimize jitter and skew in the received master clock as both parameters affect measurement performance.

Jitter in the master clock causes jitter in the generated modulator clocks, resulting in sample timing errors and increased noise.

Skew in the master clock from node to node creates a sample timing offset, resulting in systematic measurement errors in the reconstructed signal.

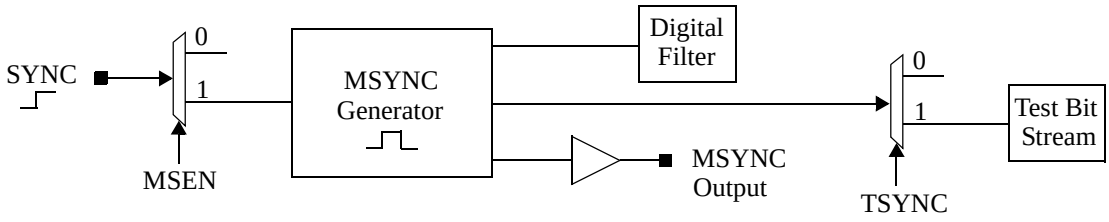


Figure 13. Synchronization Block Diagram

7. SYNCHRONIZATION

The CS5376A has a dedicated SYNC input that aligns the internal digital filter phase and generates an external signal for synchronizing modulator analog sampling. By providing simultaneous rising edges to the SYNC pins of multiple CS5376A devices, synchronous sampling across a network can be guaranteed.

7.1 Pin Description

SYNC - Pin 59

Synchronization input, rising edge triggered.

7.2 MSYNC Generation

The SYNC signal rising edge is used to generate a retimed synchronization signal, MSYNC. The MSYNC signal reinitializes internal digital filter phase and is driven onto the MSYNC output pin to phase align modulator analog sampling.

The MSEN bit in the digital filter CONFIG register (0x00) enables MSYNC generation. See “Modulator Interface” on page 39 for more information about MSYNC.

7.3 Digital Filter Synchronization

The internal MSYNC signal resets the digital filter state machine to establish a known digital filter phase. Filter convolutions restart, and the next output word is available one full sample period later.

Repetitive synchronization is supported when SYNC events occur at exactly the selected output word rate. In this case, re-synchronization occurs at the start of a convolution cycle when the digital filter state machine is already reset.

7.4 Modulator Synchronization

The external MSYNC signal phase aligns modulator analog sampling when connected to the CS5371/72 MSYNC input. This ensures synchronous analog sampling relative to MCLK.

Repetitive synchronization of the modulators is supported when SYNC events occur at exactly the selected output word rate. In this case, synchronization will occur at the start of analog sampling.

7.5 Test Bit Stream Synchronization

When the test bit stream generator is enabled, an MSYNC signal can reset the internal data pointer. This restarts the test bit stream from the first data point to establish a known output signal phase.

The TSYNC bit in the digital filter TBSCFG register (0x2A) enables synchronization of the test bit stream by MSYNC. When TSYNC is disabled, the test bit stream phase is not affected by MSYNC.

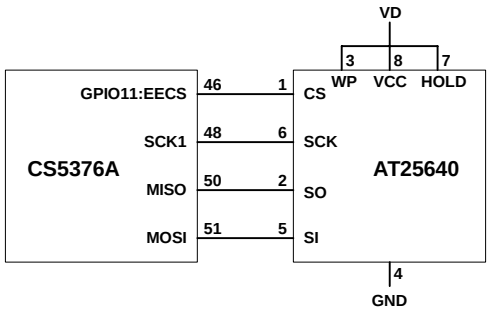


Figure 14. EEPROM Configuration Block Diagram

8. CONFIGURATION BY EEPROM

After reset, the CS5376A reads the state of the BOOT pin to determine a source for configuration commands. If BOOT is high, the CS5376A initiates serial transactions through the SPI 1 port to read configuration information from an external EEPROM.

8.1 Pin Descriptions

Pins required for EEPROM boot are listed here, other SPI 1 pins are inactive.

GPIO11:EECS - Pin 46

EEPROM chip select output, active low.

SCK1 - Pin 48

Serial clock output, nominally 1.024 MHz.

MOSI - Pin 51

Serial data output pin. Valid on rising edge of SCK1, transition on falling edge.

MISO - Pin 50

Serial data input pin. Valid on rising edge of SCK1, transition on falling edge.

8.2 EEPROM Hardware Interface

When booting from EEPROM the CS5376A SPI 1 port actively performs serial transactions, as shown in Figure 15, to read configuration commands and data. 8-bit SPI opcodes and 16-bit addresses are combined to read back 8-bit configuration commands and 24-bit configuration data.

System design should include a connection to the configuration EEPROM for in-circuit reprogramming. The CS5376A SPI 1 pins go high impedance when inactive to support external connections to the serial bus.

8.3 EEPROM Organization

The boot EEPROM holds the 8-bit commands and 24-bit data required to initialize the CS5376A into an operational state. Configuration information starts at memory location 0x10, with addresses 0x00 to 0x0F free for use as manufacturing header information.

The first serial transaction reads a 1-byte command from memory location 0x10 and then, depending on the command type, reads multiple 3-byte data words to complete the command. Command and data reads continue until the ‘Filter Start’ command is recognized.

The maximum number of bytes that can be written for a single configuration is approximately

Instruction	Opcode	Address	Definition
Read	0x03	ADDR[15:0]	Read data beginning at the address given in ADDR.

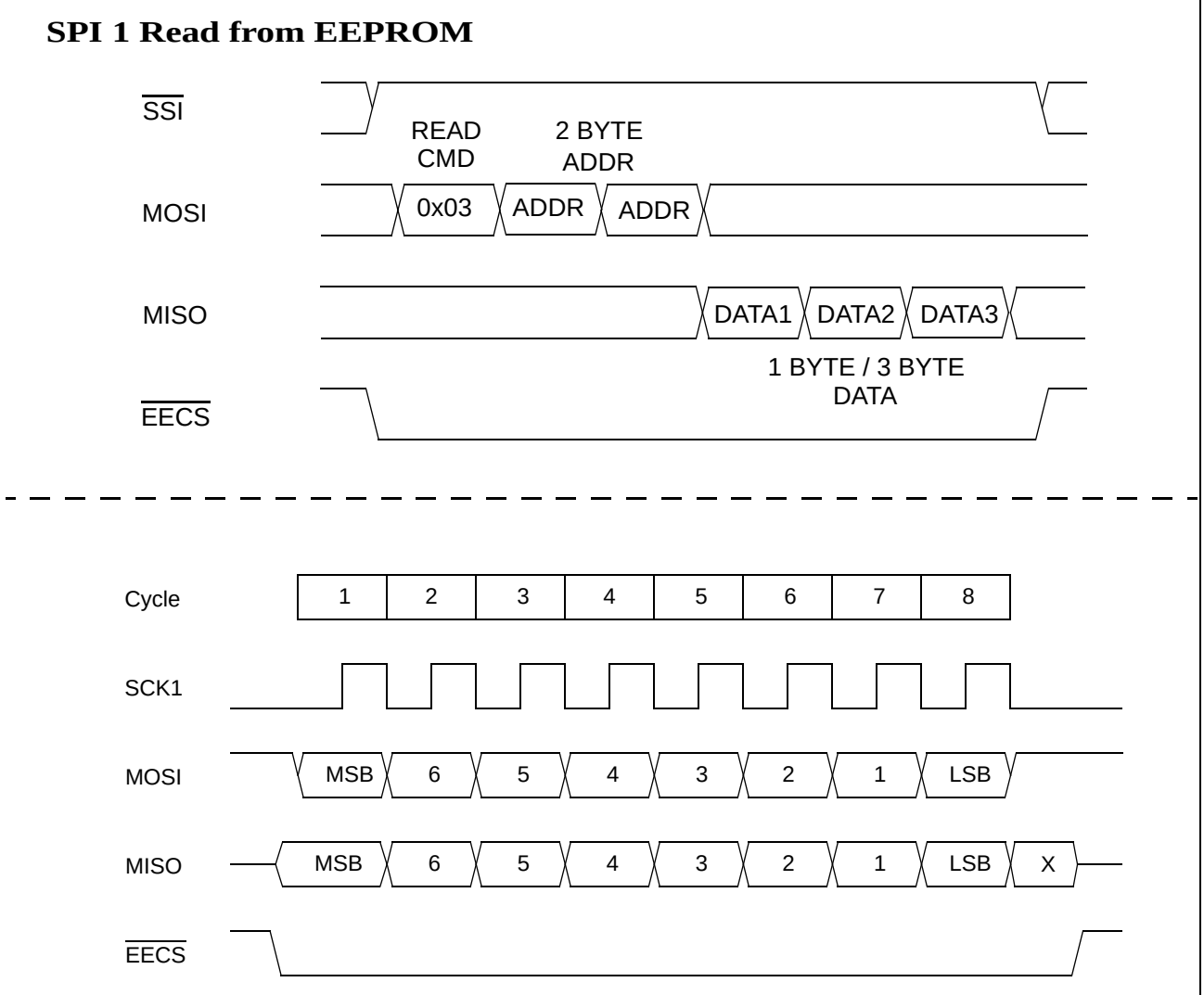


Figure 15. SPI 1 EEPROM Read Transactions

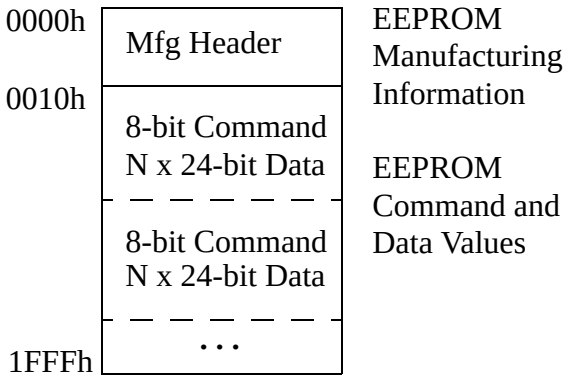


Figure 16. 8 Kbyte EEPROM Memory Organization

5 KByte (40 Kbit), which includes command overhead:

Memory Requirement	Bytes
Digital Filter Registers (22)	154
FIR Coefficients (255+255)	1537
IIR Coefficients (3+5)	25
Test Bit Stream Data (1024)	3076
'Filter Start' Command	1
Total Bytes	**4793**

Table 4. Maximum EEPROM Configuration

Supported serial configuration EEPROMs are SPI mode 0 (0,0) compatible, 16-bit addresses, 8-bit data, larger than 5 KByte (40 KBit). ATMEL AT25640, AT25128, or similar serial EEPROMs are recommended.

8.4 EEPROM Configuration Commands

A summary of available EEPROM commands is shown in Table 5.

Write DF Register - 0x01

This EEPROM command writes a data value to the specified digital filter register. Digital filter registers control hardware peripherals and filtering functions. See "Digital Filter Registers" on page 87 for the bit definitions of the digital filter registers.

Sample Command:

Write digital filter register 0x00 with data value 0x070431. Then write 0x20 with data 0x000240.

01 00 00 00 07 04 31

01 00 00 20 00 02 40

Write FIR Coefficients - 0x02

This EEPROM command writes custom coefficients for the FIR1 and FIR2 filters. The first two data words set the number of FIR1 and FIR2 coefficients to be written. The remaining data words are the concatenated FIR1 and FIR2 coefficients.

A maximum of 255 coefficients can be written for each FIR filter, though the available digital filter computation cycles will limit their practical size. See "FIR Filter" on page 47 for more information about FIR filter coefficients.

Sample Command:

Write FIR1 coefficients 0x00022E, 0x000771 then FIR2 coefficients 0xFFFFB9, 0xFFFE8D.

02 00 00 02 00 00 02

00 02 2E 00 07 71 FF FF B9 FF FE 8D

Write IIR Coefficients - 0x03

This EEPROM command writes custom coefficients for the two stage IIR filter. The IIR architecture and number of coefficients is fixed, so eight data words containing coefficient values always immediately follow the command byte. The IIR coefficient write order is: a11, b10, b11, a21, a22, b20, b21, and b22. See "IIR Filter" on page 55 for more information about IIR filter coefficients.

Sample Command:

Write IIR1 coefficients 0x84BC9D, 0x7DA1B1, 0x825E4F, and IIR2 coefficients 0x83694F, 0x3CAD5F, 0x3E5104, 0x835DF8, 0x3E5104.

03

84 BC 9D 7D A1 B1 82 5E 4F 83 69 4F

3C AD 5F 3E 51 04 83 5D F8 3E 51 04

Write ROM Coefficients - 0x04

This EEPROM command selects the on-chip coefficients for the FIR1, FIR2, IIR 1st order, and IIR 2nd order filters for use by the digital filter. One data word is required to select which internal coefficient sets to use. See “Filter Coefficient Selection” on page 41 for information about selecting on-chip FIR and IIR coefficient sets.

Sample Command:

Select IIR1 and IIR2 3 Hz @ 500 SPS low-cut coefficients, with FIR1 and FIR2 linear phase high-cut coefficients. Data word 0x002200.

04 00 22 00

Write TBS Data - 0x05

This EEPROM command writes a custom data set for the test bit stream (TBS) generator. This command, along with the ability to program the test bit stream generator interpolation and clock rate, can create custom frequency test signals.

The first data word sets the number of TBS data to be written and the remaining data words are the TBS data values. See “Test Bit Stream Generator” on page 64 for information about using custom test bit stream data sets.

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
WRITE TBS DATA	05	NUM TBS (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	06	-	Use On-Chip TBS Data
FILTER START	07	-	Start Digital Filter Operation

(DATA) indicates multiple words of this type are to be written.

Table 5. EEPROM Boot Configuration Commands

Sample Command:

Write test bit stream data 0x000000, 0x0007DA, 0x000FB5, 0x00178F.

05 00 00 04

00 00 00 00 07 DA 00 0F B5 00 17 8F

Write TBS ROM Data - 0x06

This EEPROM command selects the on-chip test bit stream (TBS) data for use by the TBS generator. No data words are required for this EEPROM command. See “Test Bit Stream Generator” on page 64 for more information about the on-chip test bit stream data set.

Sample Command:

06

Filter Start - 0x07

This EEPROM command initializes and starts the digital filter. Measurement data becomes available one full sample period after this command is received. No data words are required for this EEPROM command.

Sample Command:

07

8.5 Example EEPROM Configuration

Table 6 shows an example EEPROM file for a minimal CS5376A configuration.

Addr	Data	Description
00	00	Mfg header
01	00	
02	00	
03	00	
04	00	
05	00	
06	00	
07	00	
08	00	
09	00	
0A	00	
0B	00	
0C	00	
0D	00	
0E	00	
0F	00	
10	04	Write ROM Coefficients
11	00	
12	22	
13	00	
14	06	Write TBS ROM Data
15	01	Write CONFIG Register
16	00	
17	00	
18	00	
19	07	
1A	04	
1B	31	
1C	01	Write FILTCFG Register
1D	00	
1E	00	
1F	20	

Addr	Data	Description
20	00	
21	02	
22	40	
23	01	Write TBSCFG Register
24	00	
25	00	
26	2A	
27	07	
28	40	
29	40	
2A	01	Write TBSGAIN Register
2B	00	
2C	00	
2D	2B	
2E	04	
2F	B0	
30	00	
31	07	Filter Start

Table 6. Example EEPROM File

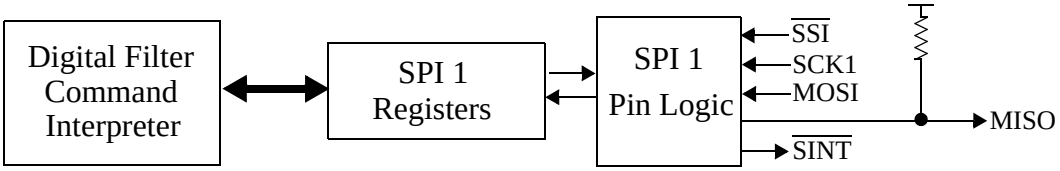


Figure 17. Serial Peripheral Interface 1 (SPI 1) Block Diagram

9. CONFIGURATION BY MICROCONTROLLER

After reset, the CS5376A reads the state of the BOOT pin to determine a source for configuration commands. If BOOT is low, the CS5376A receives configuration commands from a microcontroller.

9.1 Pin Descriptions

Pins required for microcontroller boot are listed here, other SPI 1 pins are inactive.

$\overline{SSI}$ - Pin 49

Slave select input pin, active low. Serial chip select input from a microcontroller.

SCK1 - Pin 48

Serial clock input pin. Serial clock input from microcontroller, maximum 4.096 MHz.

MOSI - Pin 51

Serial data input pin. Valid on rising edge of SCK1, transition on falling edge.

MISO - Pin 50

Serial data output pin. Valid on rising edge of SCK1, transition on falling edge. Open drain output requiring a 10 kΩ pull-up resistor.

$\overline{SINT}$ - Pin 52

Serial interrupt output pin, active low. 1 uS active low pulse output when ready for next serial transaction.

9.2 Microcontroller Hardware Interface

When booting from a microcontroller the CS5376A SPI 1 port receives configuration commands and configuration data through serial transactions, as shown in Figure 18. 8-bit SPI opcodes and 8-bit addresses are combined to read and write 24-bit configuration commands and data.

Microcontroller serial transactions require toggling the $\overline{SSI}$ pin as the CS5376A chip select and writing a serial clock to the SCK1 input. Serial data is input to the CS5376A on the MOSI pin, and output from the CS5376A on the MISO pin.

9.3 Microcontroller Serial Transactions

Microcontroller configuration commands are written to the digital filter through the SPI 1 registers. A 24-bit command and two 24-bit data words can be written to the SPI 1 registers in any single serial transaction. Some commands require additional data words through additional serial transactions to complete.

9.3.1 SPI opcodes

A microcontroller communicates with the CS5376A SPI 1 port using standard 8-bit SPI opcodes and an 8-bit SPI address. The standard SPI ‘Read’ and ‘Write’ opcodes are listed in Figure 18.

Instruction	Opcode	Address	Definition
Write	0x02	ADDR[7:0]	Write SPI 1 registers beginning at the address in ADDR.
Read	0x03	ADDR[7:0]	Read SPI 1 registers beginning at the address in ADDR.

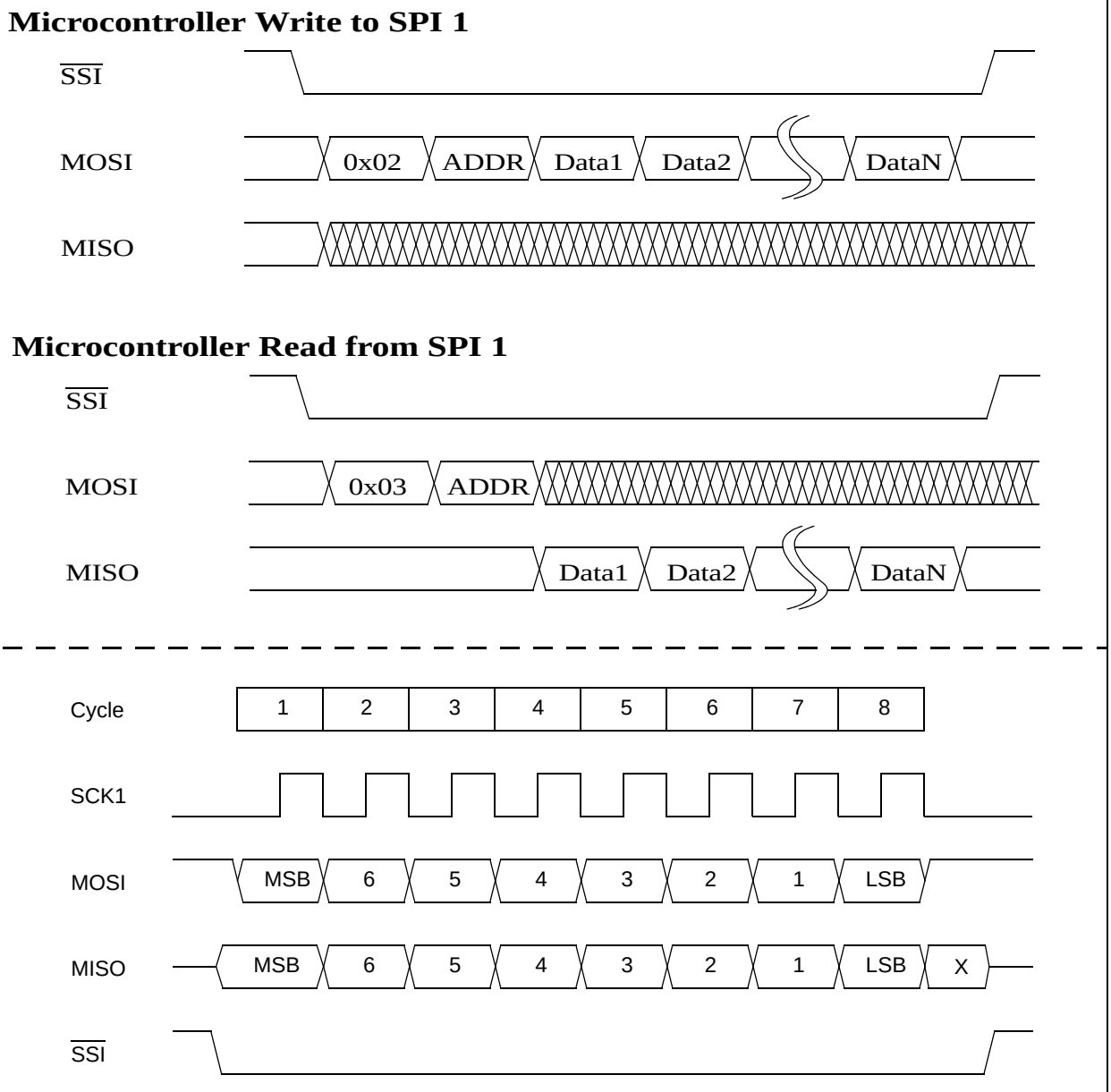


Figure 18. Microcontroller Serial Transactions

9.3.2 SPI 1 registers

The SPI 1 registers are shown in Figure 19 and are 24-bit registers mapped into an 8-bit register space as high, mid, and low bytes. See “SPI 1 Registers” on page 82 for the bit definitions of the SPI 1 registers.

9.3.3 SPI 1 transactions

A serial transaction to the SPI 1 registers starts with an SPI opcode, followed by an address, and then some number of data bytes written or read starting at that address.

Typical serial write transactions require sending groups of 5, 8, or 11 total bytes to the SPI1CMD or SPI1DAT1 registers.

Example 5-byte write transaction to SPI1CMD

02 03 12 34 56

Example 5-byte write transaction to SPI1DAT1

02 06 12 34 56

Example 8-byte write transaction to SPI1CMD

02 03 12 34 56 AB CD EF

Example 8-byte write transaction to SPI1DAT1

02 06 12 34 56 AB CD EF

Example 11-byte write transaction to SPI1CMD

02 03 12 34 56 AB CD EF 65 43 21

Typical serial read transactions require groups of 3 or 5 bytes, split between writing into MOSI and reading from MISO.

3-byte read transaction of mid-byte of SPI1CTRL

MOSI: 03 01 00

MISO: xx xx 12

5-byte read transaction of SPI1DAT1

MOSI: 03 06 00 00 00

MISO: xx xx 12 34 56

9.3.4 Multiple serial transactions

Some configuration commands require multiple serial transactions to complete. There must be a small delay between transactions for the CS5376A to process the incoming data. Three methods can be used to ensure the CS5376A is ready to receive the next configuration command.

1) Delay a fixed 1 ms period to guarantee enough time for the command to be completed.

2) Monitor the $\overline{\text{SINT}}$ pin for a 1 us active low pulse. This pulse output occurs once the CS5376A completes processing the current command.

3) Verify the status of the E2DREQ bit by reading the SPI1CTRL register. When low, the CS5376A is ready for the next command.

9.3.5 Polling E2DREQ

One transaction type that can always be performed no matter the delay from the previous configuration command is reading E2DREQ in the mid-byte of the SPI1CTRL register. A 3-byte read transaction.

MOSI: 03 01 00

MISO: xx xx 01 <- E2DREQ bit high

MISO: xx xx 00 <- E2DREQ bit low

Name	Addr.	Type	# Bits	Description
SPI1CTRL	00 - 02	R/W	8, 8, 8	SPI 1 Control
SPI1CMD	03 - 05	R/W	8, 8, 8	SPI 1 Command
SPI1DAT1	06 - 08	R/W	8, 8, 8	SPI 1 Data 1
SPI1DAT2	09 - 0B	R/W	8, 8, 8	SPI 1 Data 2

Figure 19. SPI 1 Registers

The E2DREQ bit reads high while a configuration command is being processed. When low, the digital filter is ready to receive a new configuration command.

9.4 Microcontroller Configuration Commands

A summary of available microcontroller configuration commands is listed in Table 7.

Write DF Register - 0x01

This configuration command writes a specified digital filter register. Digital filter registers control hardware peripherals and filtering functions. See “Digital Filter Registers” on page 87 for the bit definitions of the digital filter registers.

Sample Command:

Write digital filter register 0x00 with data value 0x070431. Then write 0x20 with data 0x000240.

02 03 00 00 01 00 00 00 07 04 31

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

02 03 00 00 01 00 00 20 00 02 40

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

Read DF Register - 0x02

This command reads a specified digital filter register. The register value is requested in the first SPI transaction, with the register value copied to SPI1DAT1 and read in a subsequent SPI transaction.

Sample Command:

Read digital filter registers 0x00 and 0x20.

02 03 00 00 02 00 00 00

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
WRITE TBS DATA	000006	NUM TBS (TBS DATA)	- (TBS DATA)	Write Custom Test Bit Stream Data
WRITE ROM TBS	000007	-	-	Use On-Chip TBS Data
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 7. Microcontroller Boot Configuration Commands

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

MOSI: 03 06 00 00 00

MISO: xx xx 07 04 31

02 03 00 00 02 00 00 20

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

MOSI: 03 06 00 00 00

MISO: xx xx 00 02 40

Write FIR Coefficients - 0x03

This command writes custom coefficients for the FIR1 and FIR2 filters. The first two data words set the number of FIR1 and FIR2 coefficients to be written. The remaining data words are the concatenated FIR1 and FIR2 coefficients.

A maximum of 255 coefficients can be written for each FIR filter, though the available digital filter computation cycles will limit their practical size. See "FIR Filter" on page 47 for more information about FIR filter coefficients.

Sample Command:

Write FIR1 coefficients 0x00022E, 0x000771 then FIR2 coefficients 0xFFFFB9, 0xFFFE8D.

02 03 00 00 03 00 00 02 00 00 02

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

02 06 00 02 2E 00 07 71

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

02 06 FF FF B9 FF FE 8D

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

Write IIR Coefficients - 0x04

This command writes custom coefficients for the two stage IIR filter. The IIR architecture and number of coefficients is fixed, so eight coefficient values immediately follow this command. The IIR coefficient write order is: a11, b10, b11, a21, a22, b20, b21, and b22. See "IIR Filter" on page 55 for more information about IIR filter coefficients.

Sample Command:

Write IIR1 coefficients 0x84BC9D, 0x7DA1B1, 0x825E4F, and IIR2 coefficients 0x83694F, 0x3CAD5F, 0x3E5104, 0x835DF8, 0x3E5104.

02 03 00 00 04 84 BC 9D 7D A1 B1

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

02 06 82 5E 4F 83 69 4F

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

02 06 3C AD 5F 3E 51 04

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

02 06 83 5D F8 3E 51 04

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

Write ROM Coefficients - 0x05

This configuration command selects the on-chip coefficients for FIR1, FIR2, IIR 1st order, and IIR 2nd order filters for use by the digital filter. One data word is required to select which internal coefficient sets to use. See "Filter Coefficient Selection" on page 41 for information about selecting on-chip FIR and IIR coefficient sets.

Sample Command:

Select IIR1 and IIR2 3 Hz @ 500 SPS low-cut coefficients, with FIR1 and FIR2 linear phase high-cut coefficients. Data word 0x002200.

02 03 00 00 05 00 22 00

Delay 1 ms, monitor $\overline{SINT}$, or poll E2DREQ

Write TBS Data - 0x06

This command writes a custom data set for the test bit stream (TBS) generator. This command, along with the ability to program the test bit stream generator interpolation and clock rate, can create custom frequency test signals.

The first data word sets the number of TBS data to be written and the remaining data words are the TBS data values. See "Test Bit Stream Generator"

on page 64 for information about using custom test bit stream data sets.

Sample Command:

Write test bit stream data 0x000000, 0x0007DA, 0x000FB5, 0x00178F.

02 03 00 00 06 00 00 04

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

02 06 00 00 00 00 07 DA

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

02 06 00 0F B5 00 17 8F

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

Write TBS ROM Data - 0x07

This command selects the on-chip test bit stream (TBS) data for use by the TBS generator. No data words are required for this configuration command. See "Test Bit Stream Generator" on page 64 for information about the on-chip test bit stream data set.

Sample Command:

02 03 00 00 07

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

Filter Start - 0x08

This command initializes and starts the digital filter. Measurement data becomes available one full sample period after this command is issued. No data words are required for this configuration command.

Sample Command:

02 03 00 00 08

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

Filter Stop - 0x09

This command disables the digital filter. Measurement data output stops immediately after this command is issued. No data words are required for this configuration command.

Sample Command:

02 03 00 00 09

Delay 1 ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ

9.5 Example Microcontroller Configuration

Table 6 shows example microcontroller transactions for a minimal CS5376A configuration.

Transaction	SPI Data	Description
01	02 03 00 00 05 00 22 00	Write ROM coefficients
02	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
03	02 03 00 00 07	Write ROM TBS Data
04	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
05	02 03 00 00 01 00 00 00 07 04 31	Write CONFIG Register
06	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
07	02 03 00 00 01 00 00 20 00 02 40	Write FILTCFG Register
08	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
09	02 03 00 00 01 00 00 2A 07 40 40	Write TBSCFG Register
10	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
11	02 03 00 00 01 00 00 2B 04 B0 00	Write TBSGAIN Register
12	Delay 1ms, monitor $\overline{\text{SINT}}$, or poll E2DREQ	
13	02 03 00 00 08	Filter Start

Table 8. Example Microcontroller Configuration

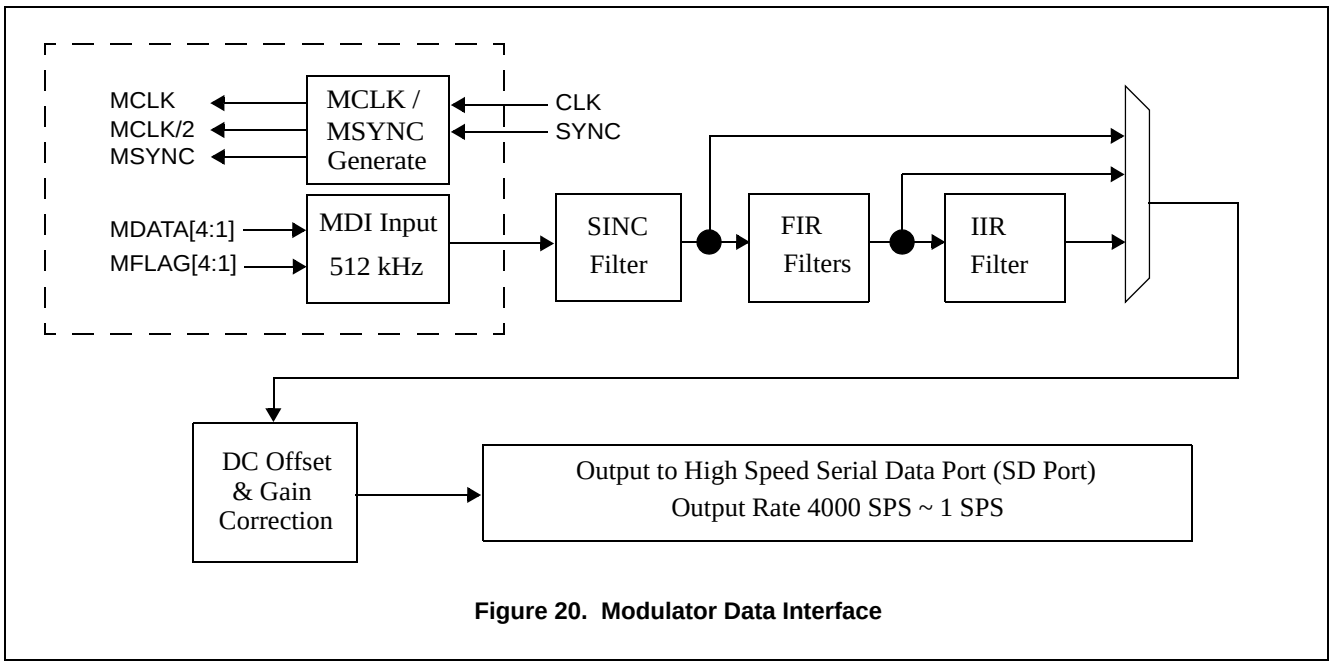


Figure 20. Modulator Data Interface

10. MODULATOR INTERFACE

The CS5376A performs digital filtering for up to four ΔΣ modulators. Signals from the modulators are connected through the modulator data interface (MDI).

10.1 Pin Descriptions

MCLK, MCLK/2 - Pins 13, 12

Modulator clock outputs. Nominally 2.048 MHz and 1.024 MHz.

MSYNC - Pin 14

Modulator synchronization signal output. Generated from the SYNC input.

MDATA1 - MDATA4 - Pins 15, 17, 19, 21

Modulator data inputs, nominally 512 kbit/s.

MFLAG1 - MFLAG4 - Pins 16, 18, 20, 22

Modulator flag inputs. Driven high when modulator is unstable due to an analog over-range signal.

10.2 Modulator Clock Generation

The MCLK and MCLK/2 outputs are low-jitter, low-skew modulator clocks generated from the 32.768 MHz master clock.

MCLK typically operates at 2.048 MHz unless analog low-power modes require a 1.024 MHz modulator clock. MCLK/2 always produces a clock at half the selected MCLK rate.

The MCLK rate is selected and the MCLK and MCLK/2 outputs are enabled by bits in the digital filter CONFIG register (0x00). By default MCLK and MCLK/2 are disabled and driven low.

10.3 Modulator Synchronization

The MSYNC output signal follows an input on the SYNC pin. MSYNC phase aligns the modulator sampling instant to guarantee synchronous analog sampling across a measurement network.

MSYNC is enabled by a bit in the CONFIG register (0x00). By default SYNC inputs do not cause an MSYNC output.

10.4 Modulator Data Inputs

The MDATA input expects 1-bit ΔΣ data at a 512 kHz or 256 kHz rate. The input rate is selected by a bit in the CONFIG register (0x00). By default, MDATA is expected at 512 kHz.

The MDATA input one's density is designed for full scale positive at 86% and full scale negative at 14%, with absolute maximum over-range capability to 93% and 7%. These raw ΔΣ inputs are decimated and filtered by the digital filter to create 24-bit samples at the output rate.

10.5 Modulator Flag Inputs

A high MFLAG input signal indicates the corresponding ΔΣ modulator has become unstable due to an analog over-range input signal. Once the over-range signal is reduced, the modulator recovers stability and the MFLAG signal is cleared.

The MFLAG inputs are mapped to status bits in the SD port, and are associated with each sample when written. See "Serial Data Port" on page 61 for more information on the MFLAG error bits in the SD port status byte.

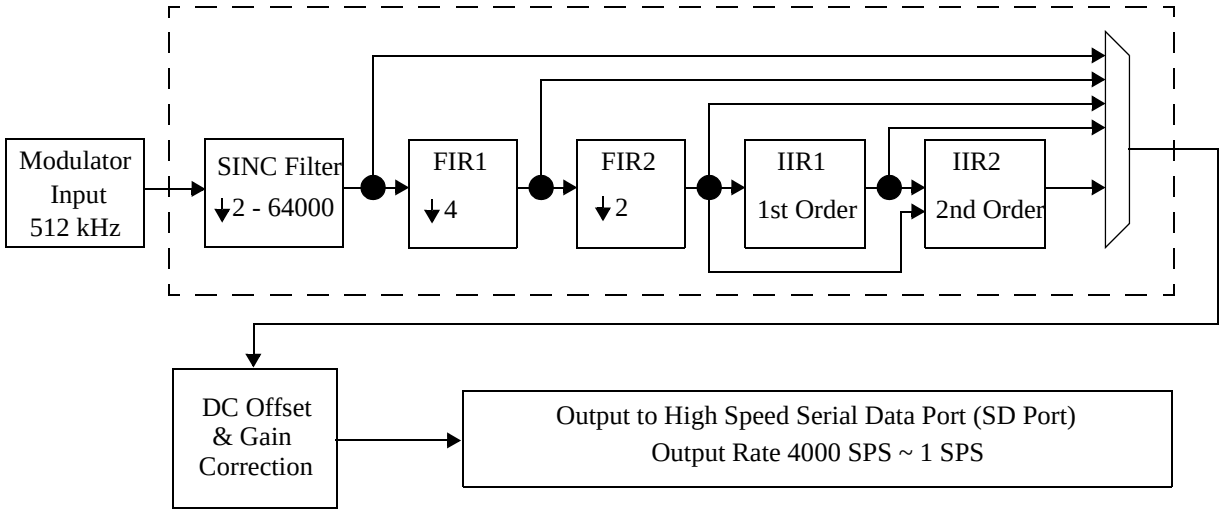


Figure 21. Digital Filter Stages

11.DIGITAL FILTER INITIALIZATION

The CS5376A digital filter consists of three multi-stage sections: a three stage SINC filter, a two stage FIR filter, and a two stage IIR filter.

To initialize the digital filter, FIR and IIR coefficient sets are selected using configuration commands, and the FILTCFG register (0x20) is written to select the output filter stage, the output word rate, and the number of enabled channels. The digital filter clock rate is selected by writing the CONFIG register (0x00).

11.1 Filter Coefficient Selection

Selection of SINC filter coefficients is not required as they are selected automatically based on the programmed output word rate.

Digital filter FIR and IIR coefficients are selected using the 'Write FIR Coefficients' and 'Write IIR Coefficients', or the 'Write ROM Coefficients' configuration commands. When writing the FIR and IIR coefficients from ROM, a data word selects an on-chip coefficient set for each filter stage. Figure 22 shows the format of the coefficient selection word, and the available coefficient sets for each selection.

Characteristics of the on-chip digital filter coefficients are discussed in the 'SINC Filter', 'FIR Filter', and 'IIR Filter' sections of this data sheet.

11.2 Filter Configuration Options

Digital filter parameters are selected by bits in the FILTCFG register (0x20), and the digital filter clock rate is selected by bits in the CONFIG register (0x00).

11.2.1 Output Filter Stage

The digital filter can output data following any stage in the filter chain. The output filter stage is selected by the FSEL bits in the FILTCFG register.

Taking data from the SINC or FIR1 filter stages reduces the overall decimation of the filter chain and increases the output rate, as discussed in the following section. Taking data from FIR2, IIR1, IIR2, or IIR3 results in data at the selected rate.

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 22. FIR and IIR Coefficient Set Selection Word

11.2.2 Output Word Rate

The CS5376A digital filter supports output word rates (OWRs) between 4000 SPS and 1 SPS. The output word rate is selected by the DEC bits in the FILTCFG register.

When taking data directly from the SINC filter, the decimation of the FIR1 and FIR2 stages is bypassed and the actual output word rate is multiplied by a factor of eight compared with the register selection. When taking data directly from FIR1, the decimation of the FIR2 stage is bypassed and the actual output word rate is multiplied by a factor of two. Data taken from the FIR2, IIR1, IIR2, or IIR3 filtering stages is output at the selected rate.

11.2.3 Channel Enable

Digital filtering can be performed simultaneously for up to four ΔΣ modulators. The number of enabled channels is selected by the CH bits in the FILTCFG register.

Channels are enabled sequentially. Selecting one channel operation enables channel 1 only, selecting two channel operation enables channels 1 and 2, selecting three channel operation enables channels 1, 2, and 3, and selecting four channel operation enables all four channels.

11.2.4 Digital Filter Clock

The digital filter clock rate is programmable between 16.384 MHz and 32 kHz by bits in the CONFIG register.

Computation Cycles

The minimum digital filter clock rate for a configuration depends on the computation cycles required to complete digital filter convolutions at the selected output word rate. All configurations work for a maximum digital filter clock, but lower clock rates consume less power.

Standby Mode

The CS5376A can be placed in a low-power standby mode by sending the ‘Filter Stop’ configuration command and programming the digital filter clock to 32 kHz. In this mode the digital filter idles, consuming minimal power until re-enabled by later configuration commands.

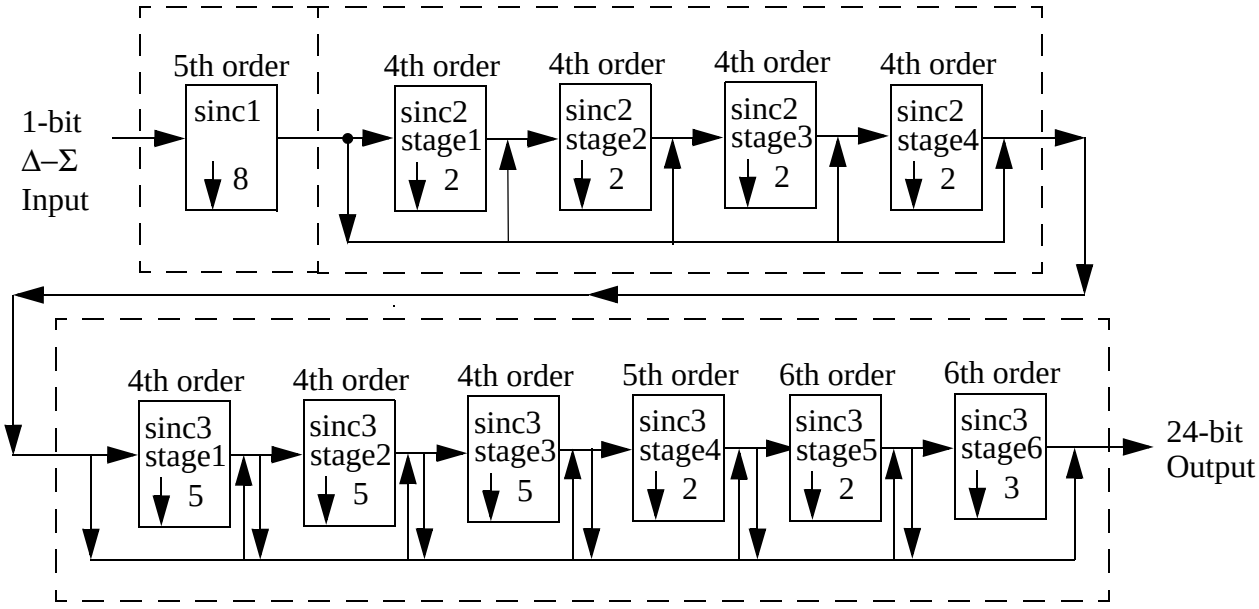


Figure 23. SINC Filter Block Diagram

12. SINC FILTER

The SINC filters primary purpose is to attenuate out-of-band noise components from the ΔΣ modulators. While doing so, they decimate 1-bit ΔΣ data into lower frequency 24-bit data suitable for the FIR and IIR filters.

The SINC filter has three cascaded sections, SINC1, SINC2, and SINC3, which are each made up of the smaller stages shown in Figure 23.

The selected output word rate in the FILTCFG register automatically determines the coefficients and decimation ratios selected for the SINC filters. Once the SINC filter configuration is set, all enabled channels are filtered and decimated using an identical hardware algorithm.

12.1 SINC1 Filter

The first section is SINC1, a single stage 5th order fixed decimate by 8 SINC filter. This SINC filter decimates the incoming 1-bit ΔΣ bit stream from the modulators down to a 64 kHz rate.

12.2 SINC2 Filter

The second section is SINC2, a multi-stage, variable order, variable decimation SINC filter. Depending on the selected output word rate in the FILTCFG register, different cascaded SINC2 stages are enabled, as shown in Table 9.

12.3 SINC3 Filter

The last section is SINC3, a flexible multi-stage variable order, variable decimation SINC filter. Depending on the selected output word rate in the FILTCFG register, different SINC3 stages are enabled, as shown in Table 9.

12.4 SINC Filter Synchronization

The SINC filter is synchronized to the external system by the MSYNC signal, which is generated from the SYNC input. The MSYNC signal sets a reference time (time 0) for all filter operations, and the SINC filter is restarted to phase align with this reference time.

SINC1 – Single stage, fixed decimate by 8

5th order decimate by 8, 36 coefficients

SINC2 – Multi-stage, variable decimation

Stage 1: 4th order decimate by 2, 5 coefficients
Stage 2: 4th order decimate by 2, 5 coefficients
Stage 3: 5th order decimate by 2, 6 coefficients
Stage 4: 6th order decimate by 2, 7 coefficients

SINC3 – Multi-stage, variable decimation

Stage 1: 4th order decimate by 5, 17 coefficients
Stage 2: 4th order decimate by 5, 17 coefficients
Stage 3: 4th order decimate by 5, 17 coefficients
Stage 4: 5th order decimate by 2, 6 coefficients
Stage 5: 6th order decimate by 2, 7 coefficients
Stage 6: 6th order decimate by 3, 13 coefficients

Figure 24. SINC Filter Stages

SINC filters

FIR2 Output Word Rate	DEC Bit Setting	SINC1 Deci-mation	SINC2 Deci-mation	SINC2 Stages	SINC3 Deci-mation	SINC3 Stages
4000	0111	8	2	4	-	-
2000	0110	8	4	3,4	-	-
1000	0101	8	8	2,3,4	-	-
500	0100	8	16	1,2,3,4	-	-
333	0011	8	8	2,3,4	3	6
250	0010	8	16	1,2,3,4	2	5
200	0001	8	2	4	20	3,4,5
125	0000	8	16	1,2,3,4	4	4,5
100	1111	8	4	3,4	20	3,4,5
50	1110	8	8	2,3,4	20	3,4,5
40	1101	8	2	4	100	2,3,4,5
25	1100	8	16	1,2,3,4	20	3,4,5
20	1011	8	4	3,4	100	2,3,4,5
10	1010	8	8	2,3,4	100	2,3,4,5
5	1001	8	16	1,2,3,4	100	2,3,4,5
1	1000	8	16	1,2,3,4	500	1,2,3,4,5

Table 9. SINC Filter Configurations

Filter Type	System Function	Filter Coefficients
SINC1 5th order decimate by 8 36 coefficients	$H(z) = \left(\frac{1-z^{-8}}{1-z^{-1}}\right)^5$	h_0 = 1 h_{18} = 2460 h_1 = 5 h_{19} = 2380 h_2 = 15 h_{20} = 2226 h_3 = 35 h_{21} = 2010 h_4 = 70 h_{22} = 1750 h_5 = 126 h_{23} = 1470 h_6 = 210 h_{24} = 1190 h_7 = 330 h_{25} = 926 h_8 = 490 h_{26} = 690 h_9 = 690 h_{27} = 490 h_{10} = 926 h_{28} = 330 h_{11} = 1190 h_{29} = 210 h_{12} = 1470 h_{30} = 126 h_{13} = 1750 h_{31} = 70 h_{14} = 2010 h_{32} = 35 h_{15} = 2226 h_{33} = 15 h_{16} = 2380 h_{34} = 5 h_{17} = 2460 h_{35} = 1

Filter Type	System Function	Filter Coefficients
SINC2 (Stage 1) SINC2 (Stage 2) 4th order decimate by 2 5 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^4$	h_0 = 1 h_1 = 4 h_2 = 6 h_3 = 4 h_4 = 1
SINC2 (Stage 3) 5th order decimate by 2 6 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^5$	h_0 = 1 h_1 = 5 h_2 = 10 h_3 = 10 h_4 = 5 h_5 = 1
SINC2 (Stage 4) 6th order decimate by 2 7 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^6$	h_0 = 1 h_1 = 6 h_2 = 15 h_3 = 20 h_4 = 15 h_5 = 6 h_6 = 1

Table 10. SINC1 and SINC2 Filter Coefficients

Filter Type	System Function	Filter Coefficients
SINC3 (Stage 1) SINC3 (Stage 2) SINC3 (Stage 3) 4^{th} order decimate by 5 17 coefficients	$H(z) = \left(\frac{1-z^{-5}}{1-z^{-1}}\right)^4$	h_0 = 1 h_1 = 4 h_2 = 10 h_3 = 20 h_4 = 35 h_5 = 52 h_6 = 68 h_7 = 80 h_8 = 85 h_9 = 80 h_{10} = 68 h_{11} = 52 h_{12} = 35 h_{13} = 20 h_{14} = 10 h_{15} = 4 h_{16} = 1
SINC3 (Stage 4) 5^{th} order decimate by 2 6 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^5$	h_0 = 1 h_1 = 5 h_2 = 10 h_3 = 10 h_4 = 5 h_5 = 1
SINC3 (Stage 5) 6^{th} order decimate by 2 7 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^6$	h_0 = 1 h_1 = 6 h_2 = 15 h_3 = 20 h_4 = 15 h_5 = 6 h_6 = 1
SINC3 (Stage 6) 6^{th} order decimate by 3 13 coefficients	$H(z) = \left(\frac{1-z^{-3}}{1-z^{-1}}\right)^6$	h_0 = 1 h_1 = 6 h_2 = 21 h_3 = 50 h_4 = 90 h_5 = 126 h_6 = 141 h_7 = 126 h_8 = 90 h_9 = 50 h_{10} = 21 h_{11} = 6 h_{12} = 1

Table 11. SINC3 Filter Coefficients

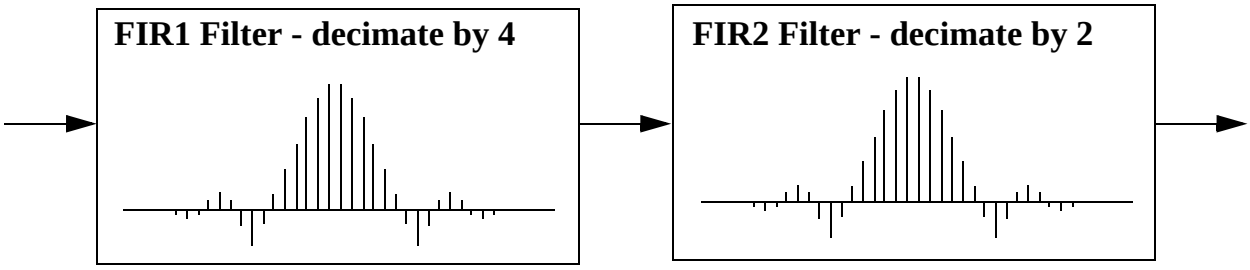


Figure 25. FIR Filter Block Diagram

13. FIR FILTER

The finite impulse response (FIR) filter block consists of two cascaded stages, FIR1 and FIR2. It compensates for SINC filter droop and creates a low-pass corner to block aliased components of the input signal.

On-chip linear phase or minimum phase coefficients can be selected using a configuration command, or the coefficients can be programmed for a custom filter response.

13.1 FIR1 Filter

The FIR1 filter stage has a decimate by four architecture. It compensates for SINC filter droop and flattens the magnitude response of the pass band.

The on-chip linear and minimum phase coefficient sets are 48-tap, with a maximum 255 programmable coefficients. All coefficients are normalized to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equation for FIR1 is a convolution of the input values, X(n), and the filter coefficients, h(k), to produce an output value, Y.

$Y = [h(k)*X(n-k)] + [h(k+1)*X(n-(k+1))] + ...$

13.2 FIR2 Filter

The FIR2 filter stage has a decimate by two architecture. It creates a low-pass brick wall filter to block aliased components of the input signal.

The on-chip linear and minimum phase coefficient sets are 126-tap, with a maximum 255 programmable coefficients. All coefficients are normalized to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equation for FIR2 is a convolution of the input values, X(n), and the filter coefficients, h(k), to produce an output value, Y.

$Y = [h(k)*X(n-k)] + [h(k+1)*X(n-(k+1))] + ...$

13.3 On-Chip FIR Coefficients

Two sets of on-chip linear phase and minimum phase coefficients are available for FIR1 and FIR2. Performance of the on-chip coefficient sets is very good, with excellent ripple and stop band characteristics as described in Figure 26 and Table 12.

Which on-chip coefficient set to use is selected by a data word following the 'Write ROM Coefficients' configuration command. See "Filter Coefficient Selection" on page 41 for information about selecting on-chip coefficient sets.

13.4 Programmable FIR Coefficients

A maximum of 255 + 255 coefficients can be programmed into FIR1 and FIR2 to create a custom filter response. The total number of coefficients for the FIR filter is fundamentally limited by the available computation cycles in the digital filter, which itself is determined by the digital filter clock rate.

Custom filter sets should normalize the maximum coefficient value to 24-bit two's complement full scale, 0x7FFFFF, and scale all other coefficients accordingly. To maintain maximum internal dynamic range, the CS5376A FIR filter performs double precision calculations with an automatic gain correction to scale the final output.

Custom FIR coefficients are uploaded using the 'Write FIR Coefficients' configuration command. See "EEPROM Configuration Commands" on page 28 or "Microcontroller Configuration Commands" on page 35 for information about writing custom FIR coefficients.

13.5 FIR Filter Synchronization

The FIR1 and FIR2 filters are synchronized to the external system by the MSYNC signal, which is generated from the SYNC input. The MSYNC signal sets a reference time (time 0) for all filter operations, and the FIR filters are restarted to phase align with this reference time.

FIR1 – Single stage, fixed decimate by 4

Coefficient set 0: linear phase decimate by 4, 48 coefficients
Coefficient set 1: minimum phase decimate by 4, 48 coefficients
SINC droop compensation filter

FIR2 – Single stage, fixed decimate by 2

Coefficient set 0: linear phase decimate by 2, 126 coefficients
Coefficient set 1: minimum phase decimate by 2, 126 coefficients
Brick wall low-pass filter, flat to 40% f_s

Combined SINC + FIR digital filter specifications

Passband ripple less than +/- 0.01 dB below 40% f_s
Transition band -3 dB frequency at 42.89% f_s
Stopband attenuation greater than 130 dB above 50% f_s

Figure 26. FIR Filter Stages

SINC + FIR filters

FIR2 Output Word Rate	SINC Deci-mation	FIR1 Deci-mation	FIR2 Deci-mation	Total Deci-mation	Passband Ripple (± dB)	Stopband Atten-uation (dB)
4000	16	4	2	128	0.0042	130.38
2000	32	4	2	256	0.0045	130.38
1000	64	4	2	512	0.0040	130.42
500	128	4	2	1024	0.0041	130.42
333	192	4	2	1536	0.0080	130.45
250	256	4	2	2048	0.0064	130.43
200	320	4	2	2560	0.0041	130.43
125	512	4	2	4096	0.0046	130.42
100	640	4	2	5120	0.0040	130.43
50	1280	4	2	10240	0.0040	130.43
40	1600	4	2	12800	0.0036	130.43
25	2560	4	2	20480	0.0040	132.98
20	3200	4	2	25600	0.0036	130.43
10	6400	4	2	51200	0.0036	130.43
5	12800	4	2	102400	0.0036	130.43
1	64000	4	2	512000	0.0029	134.31

Table 12. FIR Filter Characteristics

Individual filter stage group delay (no IIR)

	Decimation Ratios	Number of Coefficients	Group Delay (Filter Stage Input Rate)
SINC1	8	36	17.5
SINC2			
Stage 4	2	7	3.0
Stages 3,4	2,2	6,7	8.5
Stages 2,3,4	2,2,2	5,6,7	19.0
Stages 1,2,3,4	2,2,2,2	5,5,6,7	40.0
SINC3			
Stage 6	3	13	6.0
Stage 5	2	7	3.0
Stages 4,5	2,2	6,7	8.5
Stages 3,4,5	5,2,2	17,6,7	50.5
Stages 2,3,4,5	5,5,2,2	17,17,6,7	260.5
Stages 1,2,3,4,5	5,5,5,2,2	17,17,17,6,7	1310.5
FIR1			
Coefficient Set 0	4	48	23.5
Coefficient Set 1	4	48	See Figure
FIR2			
Coefficient Set 0	2	126	62.5
Coefficient Set 1	2	126	See Figure

Cumulative linear phase group delay (no IIR)

FIR2 Output Word Rate	SINC Output Group Delay (SINC Filter Input Rate)	FIR1 Output Group Delay (SINC Filter Input Rate)	FIR2 Output Group Delay (SINC Filter Input Rate)	FIR2 Output Group Delay (FIR2 Output Word Rate)
4000	41.5	417.5	4417.5	34.5117
2000	85.5	837.5	8837.5	34.5215
1000	169.5	1673.5	17673.5	34.5186
500	337.5	3345.5	35345.5	34.5171
333	553.5	5065.5	53065.5	34.5479
250	721.5	6737.5	70737.5	34.5398
200	849.5	8369.5	88369.5	34.5193
125	1425.5	13457.5	141457.5	34.5355
100	1701.5	16741.5	176741.5	34.5198
50	3401.5	33481.5	353481.5	34.5197
40	4209.5	41809.5	441809.5	34.5164
25	6801.5	66961.5	706961.5	34.5196
20	8421.5	83621.5	883621.5	34.5165
10	16841.5	167241.5	1767241.5	34.5164
5	33681.5	334481.5	3534481.5	34.5164
1	168081.5	1672081.5	17672081.5	34.5158

Table 13. SINC + FIR Group Delay

Minimum phase group delay

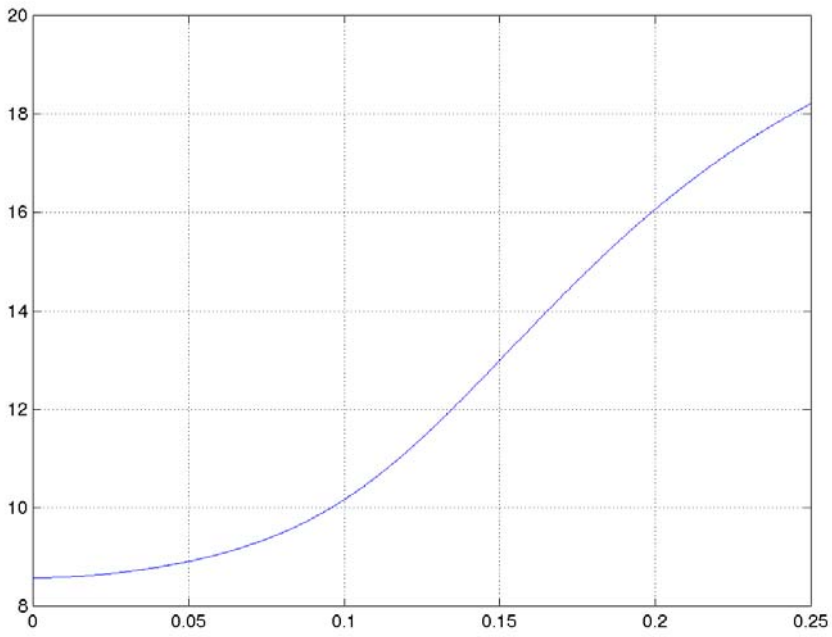
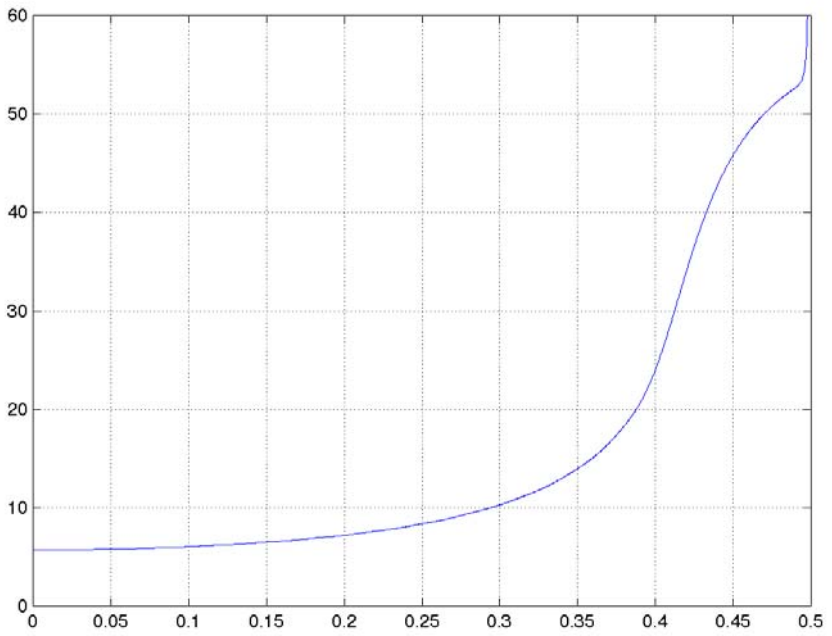
FIR1 Minimum Phase Group Delay (Normalized frequency)	
FIR2 Minimum Phase Group Delay (Normalized frequency)	

Figure 27. Minimum Phase Group Delay

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR1 (Coefficient set 0) Low pass, SINC compensation Linear phase decimate by 4 48 coefficients	h_0 = 558	h_{24} = 8388607
	h_1 = 1905	h_{25} = 7042723
	h_2 = 3834	h_{26} = 4768946
	h_3 = 5118	h_{27} = 2266428
	h_4 = 365	h_{28} = 189436
	h_5 = -14518	h_{29} = -1053303
	h_6 = -39787	h_{30} = -1392827
	h_7 = -67365	h_{31} = -1084130
	h_8 = -69909	h_{32} = -496361
	h_9 = -19450	h_{33} = 39864
	h_{10} = 97434	h_{34} = 332367
	h_{11} = 258881	h_{35} = 375562
	h_{12} = 375562	h_{36} = 258881
	h_{13} = 332367	h_{37} = 97434
	h_{14} = 39864	h_{38} = -19450
	h_{15} = -496361	h_{39} = -69909
	h_{16} = -1084130	h_{40} = -67365
	h_{17} = -1392827	h_{41} = -39787
	h_{18} = -1053303	h_{42} = -14518
	h_{19} = 189436	h_{43} = 365
	h_{20} = 2266428	h_{44} = 5118
	h_{21} = 4768946	h_{45} = 3834
	h_{22} = 7042723	h_{46} = 1905
	h_{23} = 8388607	h_{47} = 558
FIR1 (Coefficient set 1) Low pass, SINC compensation Minimum phase decimate by 4 48 coefficients	h_0 = 3337	h_{24} = 555919
	h_1 = 22258	h_{25} = -165441
	h_2 = 88284	h_{26} = -581479
	h_3 = 266742	h_{27} = -617500
	h_4 = 655747	h_{28} = -388985
	h_5 = 1371455	h_{29} = -99112
	h_6 = 2502684	h_{30} = 114761
	h_7 = 4031988	h_{31} = 186557
	h_8 = 5783129	h_{32} = 141374
	h_9 = 7396359	h_{33} = 58582
	h_{10} = 8388607	h_{34} = -12664
	h_{11} = 8325707	h_{35} = -42821
	h_{12} = 6988887	h_{36} = -35055
	h_{13} = 4531706	h_{37} = -16792
	h_{14} = 1507479	h_{38} = 367
	h_{15} = -1319126	h_{39} = 7929
	h_{16} = -3207750	h_{40} = 5926
	h_{17} = -3736028	h_{41} = 2892
	h_{18} = -2980701	h_{42} = 23
	h_{19} = -1421498	h_{43} = -1164
	h_{20} = 237307	h_{44} = -538
	h_{21} = 1373654	h_{45} = -238
	h_{22} = 1711919	h_{46} = 18
	h_{23} = 1322371	h_{47} = 113

Table 14. FIR1 Coefficients

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR2 (Coefficient set 0) Low pass, passband to 40% f_s Linear phase decimate by 2 126 coefficients	h_0 = -71	h_{63} = 8388607
	h_1 = -371	h_{64} = 3875315
	h_2 = -870	h_{65} = -766230
	h_3 = -986	h_{66} = -1854336
	h_4 = 34	h_{67} = -137179
	h_5 = 1786	h_{68} = 1113788
	h_6 = 2291	h_{69} = 454990
	h_7 = 291	h_{70} = -642475
	h_8 = -2036	h_{71} = -553873
	h_9 = -943	h_{72} = 298975
	h_{10} = 2985	h_{73} = 533334
	h_{11} = 3784	h_{74} = -49958
	h_{12} = -1458	h_{75} = -443272
	h_{13} = -5808	h_{76} = -116005
	h_{14} = -1007	h_{77} = 318763
	h_{15} = 7756	h_{78} = 208018
	h_{16} = 5935	h_{79} = -187141
	h_{17} = -7135	h_{80} = -238025
	h_{18} = -11691	h_{81} = 68863
	h_{19} = 3531	h_{82} = 221211
	h_{20} = 17500	h_{83} = 22850
	h_{21} = 4388	h_{84} = -174452
	h_{22} = -20661	h_{85} = -81993
	h_{23} = -15960	h_{86} = 114154
	h_{24} = 18930	h_{87} = 109009
	h_{25} = 29808	h_{88} = -54172
	h_{26} = -9795	h_{89} = -109189
	h_{27} = -42573	h_{90} = 4436
	h_{28} = -7745	h_{91} = 90744
	h_{29} = 49994	h_{92} = 29702
	h_{30} = 33021	h_{93} = -62651
	h_{31} = -47092	h_{94} = -47092
	h_{32} = -62651	h_{95} = 33021
	h_{33} = 29702	h_{96} = 49994
	h_{34} = 90744	h_{97} = -7745
	h_{35} = 4436	h_{98} = -42573
	h_{36} = -109189	h_{99} = -9795
	h_{37} = -54172	h_{100} = 29808
	h_{38} = 109009	h_{101} = 18930
	h_{39} = 114154	h_{102} = -15960
	h_{40} = -81993	h_{103} = -20661
	h_{41} = -174452	h_{104} = 4388
	h_{42} = 22850	h_{105} = 17500
	h_{43} = 221211	h_{106} = 3531
	h_{44} = 68863	h_{107} = -11691
	h_{45} = -238025	h_{108} = -7135
	h_{46} = -187141	h_{109} = 5935
	h_{47} = 208018	h_{110} = 7756
	h_{48} = 318763	h_{111} = -1007
	h_{49} = -116005	h_{112} = -5808
	h_{50} = -443272	h_{113} = -1458
	h_{51} = -49958	h_{114} = 3784
	h_{52} = 533334	h_{115} = 2985
	h_{53} = 298975	h_{116} = -943
	h_{54} = -553873	h_{117} = -2036
	h_{55} = -642475	h_{118} = 291
	h_{56} = 454990	h_{119} = 2291
	h_{57} = 1113788	h_{120} = 1786
	h_{58} = -137179	h_{121} = 34
	h_{59} = -1854336	h_{122} = -986
	h_{60} = -766230	h_{123} = -870
	h_{61} = 3875315	h_{124} = -371
	h_{62} = 8388607	h_{125} = -71

Table 15. FIR2 Linear Phase Coefficients

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR2 (Coefficient set 1) Low pass, passband to 40% f_s Minimum phase decimate by 2 126 coefficients	h_0 = 4019	h_{63} = 67863
	h_1 = 43275	h_{64} = -190800
	h_2 = 235427	h_{65} = -128546
	h_3 = 848528	h_{66} = 114197
	h_4 = 2240207	h_{67} = 147750
	h_5 = 4525758	h_{68} = -46352
	h_6 = 7077833	h_{69} = -143269
	h_7 = 8388607	h_{70} = -13290
	h_8 = 6885673	h_{71} = 114721
	h_9 = 2483461	h_{72} = 51933
	h_{10} = -2538963	h_{73} = -75952
	h_{11} = -4800543	h_{74} = -68746
	h_{12} = -2761696	h_{75} = 38171
	h_{13} = 1426109	h_{76} = 68492
	h_{14} = 3624338	h_{77} = -7856
	h_{15} = 1820814	h_{78} = -57526
	h_{16} = -1695825	h_{79} = -12540
	h_{17} = -2885148	h_{80} = 41717
	h_{18} = -605252	h_{81} = 23334
	h_{19} = 2135021	h_{82} = -25516
	h_{20} = 1974197	h_{83} = -26409
	h_{21} = -630111	h_{84} = 11717
	h_{22} = -2168177	h_{85} = 24246
	h_{23} = -750147	h_{86} = -1620
	h_{24} = 1516192	h_{87} = -19248
	h_{25} = 1550127	h_{88} = -4610
	h_{26} = -508445	h_{89} = 13356
	h_{27} = -1686937	h_{90} = 7526
	h_{28} = -437822	h_{91} = -7887
	h_{29} = 1308705	h_{92} = -8016
	h_{30} = 1069556	h_{93} = 3559
	h_{31} = -657282	h_{94} = 7023
	h_{32} = -1301014	h_{95} = -598
	h_{33} = -30654	h_{96} = -5350
	h_{34} = 1173754	h_{97} = -1097
	h_{35} = 579643	h_{98} = 3579
	h_{36} = -803111	h_{99} = 1806
	h_{37} = -895851	h_{100} = -2058
	h_{38} = 328399	h_{101} = -1859
	h_{39} = 962522	h_{102} = 936
	h_{40} = 124678	h_{103} = 1558
	h_{41} = -820948	h_{104} = -224
	h_{42} = -466657	h_{105} = -1129
	h_{43} = 545674	h_{106} = -152
	h_{44} = 652827	h_{107} = 718
	h_{45} = -220448	h_{108} = 290
	h_{46} = -680495	h_{109} = -395
	h_{47} = -80886	h_{110} = -290
	h_{48} = 578844	h_{111} = 178
	h_{49} = 306445	h_{112} = 227
	h_{50} = -395302	h_{113} = -53
	h_{51} = -431004	h_{114} = -151
	h_{52} = 181900	h_{115} = -5
	h_{53} = 454403	h_{116} = 86
	h_{54} = 15856	h_{117} = 23
	h_{55} = -395525	h_{118} = -42
	h_{56} = -166123	h_{119} = -22
	h_{57} = 284099	h_{120} = 17
	h_{58} = 253485	h_{121} = 14
	h_{59} = -152407	h_{122} = -5
	h_{60} = -277888	h_{123} = -7
	h_{61} = 28526	h_{124} = 1
	h_{62} = 250843	h_{125} = 3

Table 16. FIR2 Minimum Phase Coefficients

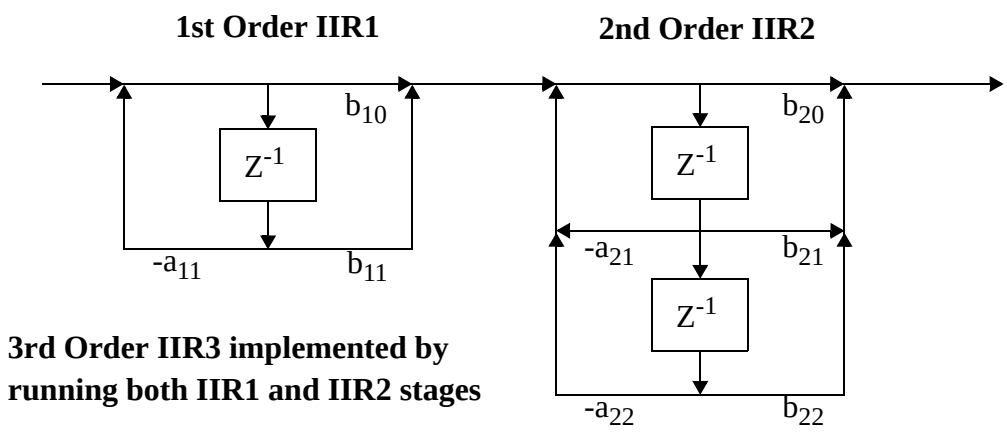


Figure 28. IIR Filter Block Diagram

14. IIR FILTER

The infinite impulse response (IIR) filter block consists of two cascaded stages, IIR1 and IIR2. It creates a high-pass corner to block very low-frequency and DC components of the input signal.

On-chip IIR1 and IIR2 coefficients can be selected using a configuration command, or the coefficients can be programmed for a custom filter response.

14.1 IIR Architecture

The architecture of the IIR filter is automatically determined when the output filter stage is selected in the FILTCFG register. Selecting the 1st order IIR1 filter bypasses the 2nd order stage, while selecting the 2nd order IIR2 filter bypasses the 1st order stage. Selection of the 3rd order IIR3 filter enables both the 1st and 2nd order stages.

14.2 IIR1 Filter

The 1st order IIR filter stage is a direct form filter with three coefficients: a11, b10, and b11. Coefficients of a 1st order IIR are inherently normalized to one, and should be scaled to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equations for the 1st order IIR include an input value, X, an output value, Y, and two intermediate values, W1 and W2, separated by a delay element (z^{-1}).

W2 = W1

W1 = X + (-a11 * W2)

Y = (W1 * b10) + (W2 * b11)

14.3 IIR2 Filter

The 2nd order IIR filter stage is a direct form filter with five coefficients: a21, a22, b20, b21, and b22. Coefficients of a 2nd order IIR are inherently normalized to two, and should be scaled to 24-bit two's complement full scale, 0x7FFFFF. Normalization effectively divides the 2nd order coefficients in half relative to the input, and requires modification of the characteristic equations.

The characteristic equations for the 2nd order IIR include an input value, X, an output value, Y, and three intermediate values, W3, W4, and W5, each separated by a delay element (z^{-1}). The following

characteristic equations model the operation of the 2nd order IIR filter with unnormalized coefficients.

W5 = W4

W4 = W3

W3 = X + (-a21 * W4) + (-a22 * W5)

Y = (W3 * b20) + (W4 * b21) + (W5 * b22)

Internally, the CS5376A uses normalized coefficients to perform the 2nd order IIR filter calculation, which changes the algorithm slightly. The following characteristic equations model the operation of the 2nd order IIR filter when using normalized coefficients.

W5 = W4

W4 = W3

W3 = 2 * [(X / 2) + (-a21 * W4) + (-a22 * W5)]

Y = 2 * [(W3 * b20) + (W4 * b21) + (W5 * b22)]

14.4 IIR3 Filter

The 3rd order IIR filter is implemented by running both the 1st order and 2nd order IIR filter stages. It can be modeled by cascading the characteristic equations of the 1st order and 2nd order IIR stages.

14.5 On-Chip IIR Coefficients

Five sets of on-chip coefficients are available for IIR1 and IIR2, each providing a 3 Hz high-pass Butterworth response at different output word rates. Characteristics of the on-chip coefficient sets are described in Figure 29 and Table 17.

Which on-chip coefficient set to use is selected by a data word following the 'Write ROM Coefficients' configuration command. See "Filter Coefficient Selection" on page 41 for information about selecting on-chip coefficient sets.

14.6 Programmable IIR Coefficients

A maximum of 3 + 5 coefficients can be programmed into IIR1 and IIR2 to create a custom filter response. Custom filter sets should normalize the coefficients to 24-bit two's complement full scale, 0x7FFFFF. To maintain maximum internal dynamic range, the CS5376A IIR filter performs double precision calculations with an automatic gain correction to scale the final output.

Custom IIR coefficients are uploaded using the 'Write IIR Coefficients' configuration command. See "EEPROM Configuration Commands" on page 28 or "Microcontroller Configuration Commands" on page 35 for information about writing custom IIR coefficients.

14.7 IIR Filter Synchronization

The IIR filter is not synchronized to the external system directly, only indirectly through the synchronization of the SINC and FIR filters. Because IIR filters have 'infinite' memory, a discontinuity in the input data stream from a synchronization event can require significant time to settle out. The exact settling time depends on the size of the discontinuity and the filter coefficient characteristics.

IIR1 - Single stage, no decimation

1st order no decimation, 3 coefficients

Coefficient set 0: high-pass, corner 0.15% f_s (3 Hz at 2000 SPS)
Coefficient set 1: high-pass, corner 0.30% f_s (3 Hz at 1000 SPS)
Coefficient set 2: high-pass, corner 0.60% f_s (3 Hz at 500 SPS)
Coefficient set 3: high-pass, corner 0.90% f_s (3 Hz at 333 SPS)
Coefficient set 4: high-pass, corner 1.20% f_s (3 Hz at 250 SPS)

IIR2 - Single stage, no decimation

2nd order no decimation, 5 coefficients

Coefficient set 0: high-pass, corner 0.15% f_s (3 Hz at 2000 SPS)
Coefficient set 1: high-pass, corner 0.30% f_s (3 Hz at 1000 SPS)
Coefficient set 2: high-pass, corner 0.60% f_s (3 Hz at 500 SPS)
Coefficient set 3: high-pass, corner 0.90% f_s (3 Hz at 333 SPS)
Coefficient set 4: high-pass, corner 1.20% f_s (3 Hz at 250 SPS)

IIR3 - Two stage, no decimation

3rd order no decimation, 8 coefficients
(Combined IIR1 and IIR2 filter responses)

Coefficient set 0,0: high-pass, corner 0.20% f_s (4 Hz at 2000 SPS)
Coefficient set 1,1: high-pass, corner 0.41% f_s (4 Hz at 1000 SPS)
Coefficient set 2,2: high-pass, corner 0.82% f_s (4 Hz at 500 SPS)
Coefficient set 3,3: high-pass, corner 1.22% f_s (4 Hz at 333 SPS)
Coefficient set 4,4: high-pass, corner 1.63% f_s (4 Hz at 250 SPS)

Figure 29. IIR Filter Stages

IIR filters

IIR1 Coeff Selection	IIR1 Corner Frequency	IIR2 Coeff Selection	IIR2 Corner Frequency	IIR3 Coeff Selection	IIR3 Corner Frequency
0	0.15% f_s	0	0.15% f_s	0,0	0.2041% f_s
1	0.30% f_s	1	0.30% f_s	1,1	0.4074% f_s
2	0.60% f_s	2	0.60% f_s	2,2	0.8152% f_s
3	0.90% f_s	3	0.90% f_s	3,3	1.2222% f_s
4	1.20% f_s	4	1.20% f_s	4,4	1.6293% f_s

Table 17. IIR Filter Characteristics

Filter Type	System Function	Filter Coefficients (normalized 24-bit)
IIR1 (Coefficient set 0) 1st order, high pass Corner at 0.15% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8309916 b_{10} = 8349262 b_{11} = -8349262
IIR1 (Coefficient set 1) 1st order, high pass Corner at 0.30% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8231957 b_{10} = 8310282 b_{11} = -8310282
IIR1 (Coefficient set 2) 1st order, high pass Corner at 0.60% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8078179 b_{10} = 8233393 b_{11} = -8233393
IIR1 (Coefficient set 3) 1st order, high pass Corner at 0.90% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -7927166 b_{10} = 8157887 b_{11} = -8157887
IIR1 (Coefficient set 4) 1st order, high pass Corner at 1.20% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -7778820 b_{10} = 8083714 b_{11} = -8083714

Filter Type	System Function	Filter Coefficients (normalized 24-bit)
IIR2 (Coefficient set 0) 2nd order, high pass Corner at 0.15% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8332704 a_{22} = 4138771 b_{20} = 4166445 b_{21} = -8332890 b_{22} = 4166445
IIR2 (Coefficient set 1) 2nd order, high pass Corner at 0.30% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8276806 a_{22} = 4083972 b_{20} = 4138770 b_{21} = -8277540 b_{22} = 4138770
IIR2 (Coefficient set 2) 2nd order, high pass Corner at 0.60% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8165041 a_{22} = 3976543 b_{20} = 4083972 b_{21} = -8167944 b_{22} = 4083972
IIR2 (Coefficient set 3) 2nd Order, high pass Corner at 0.90% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8053350 a_{22} = 3871939 b_{20} = 4029898 b_{21} = -8059796 b_{22} = 4029898
IIR2 (Coefficient set 4) 2nd order, high pass Corner at 1.20% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -7941764 a_{22} = 3770088 b_{20} = 3976539 b_{21} = -7953078 b_{22} = 3976539

Table 18. IIR Filter Coefficients

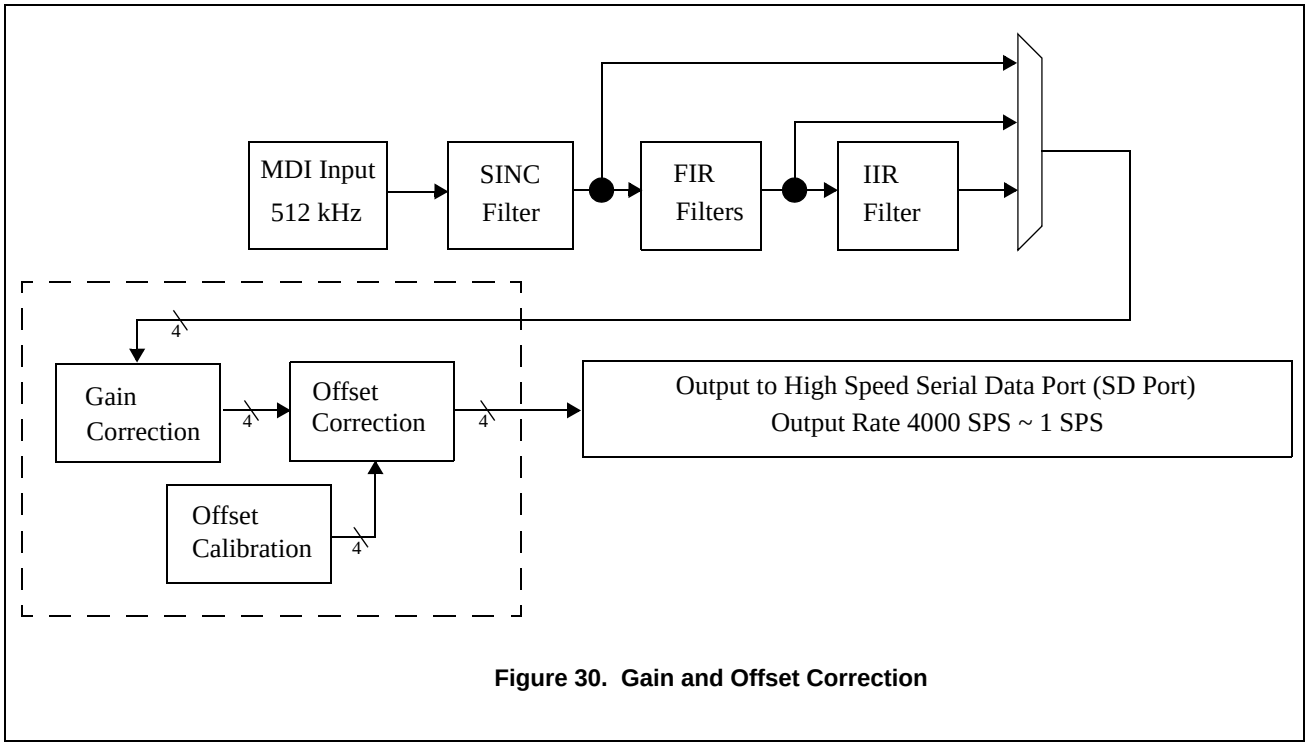


Figure 30. Gain and Offset Correction

15.GAIN AND OFFSET CORRECTION

The CS5376A digital filter can apply independent gain and offset corrections to the data of each measurement channel. Also, an offset calibration algorithm can automatically calculate offset correction values for each channel.

Gain correction values are written to the GAINx registers (0x21-0x24), while offset correction values are written to the OFFSETx registers (0x25-0x28). Gain and offset corrections are enabled by the USEGR and USEOR bits in the FILTCFG register (0x20).

When enabled, the offset calibration algorithm will automatically calculate offset correction values for each channel and write them into the OFFSETx registers. Offset calibration is enabled by writing the EXP and ORCAL bits in FILTCFG.

15.1 Gain Correction

Gain correction in the CS5376A normalizes sensor gains in multi-sensor networks. It requires externally calculated correction values to be written into the GAINx registers (0x21-0x24).

Gain correction values are 24-bit two's complement with unity gain defined as full scale, 0x7FFFFF. Gain correction always scales to a fractional value, and can never gain the digital filter data greater than one.

Output Value = Data * (GAIN / 0x7FFFFF)

Unity Gain: GAIN = 0x7FFFFF

50% Gain: GAIN = 0x3FFFFF

Zero Gain: GAIN = 0x000000

Once the GAIN registers are written, the USEGR bit in the FILTCFG register enables gain correction.

15.2 Offset Correction

Offset correction in the CS5376A cancels the DC bias of a measurement channel by subtracting the

value in the OFFSETx registers (0x25-0x28) from the digital filter output data word.

Offset correction values are 24-bit two's complement with a maximum positive value of 0x7FFFFF, and a maximum negative value of 0x800000. If applying an offset correction causes the final result to exceed a 24-bit two's complement maximum, the output data will saturate to that maximum value.

Output Data = Input Data - Offset Correction

Max Positive Output Value = 0x7FFFFF

Max Negative Output Value = 0x800000

Once the OFFSET registers are written, the USEOR bit in the FILTCFG register enables offset correction.

15.3 Offset Calibration

An offset calibration algorithm in the CS5376A can automatically calculate offset correction values. When using the offset calibration algorithm, background noise data should be used as the basis for calculating the offset value of each measurement channel.

The offset calibration algorithm is an exponential averaging function that places increased weight on more recent digital filter data. The exponential weighting factor is set by the EXP bits in the FILTCFG register, with larger exponent values producing a smoother averaging function that requires a longer settling time, and smaller values producing a noisier averaging function that requires a shorter settling time. Typical exponential values range from 0x05 to 0x0F, depending on the available settling time.

The characteristic equations of the offset calibration algorithm include an input value, X, an output value, Y, a summation value, YSUM, a sample index, n, and an exponential value, EXP.

$$Y(n) = X(n) - [YSUM(n-1) >> EXP]$$

$$YSUM(n) = Y(n) + YSUM(n-1)$$

$$\text{Offset Correction} = YSUM >> EXP$$

Once the EXP bits are written, the ORCAL bit in the FILTCFG register is set to enable offset calibration. When enabled, updated offset correction values are automatically written to the OFFSETx registers. When the offset calibration algorithm is fully settled, the ORCAL bit is cleared to maintain the final values in the OFFSETx registers.

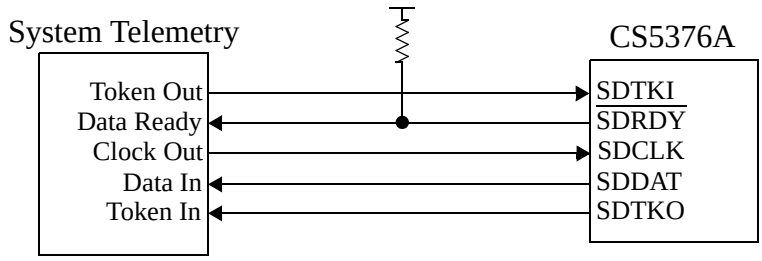


Figure 31. Serial Data Port Block Diagram

16.SERIAL DATA PORT

Once digital filtering is complete, each 24-bit output sample is combined with an 8-bit status byte. These 32-bit data words are written to an 8-deep FIFO buffer and then transmitted to the communications channel through a high speed serial data port (SD port).

16.1 Pin Descriptions

SDTKI - Pin 64

Token input, requests an SD port transaction.

$\overline{\text{SDRDY}}$ - Pin 61

Data ready output signal, active low. Open drain output requiring a 10 kΩ pull-up resistor.

SDCLK - Pin 62

Serial clock input.

SDDAT - Pin 60

Serial data output. Data valid on rising edge of SDCLK, transition on falling edge.

SDTKO - Pin 63

Token output, ends an SD port transaction. Passes through the SDTKI signal when no data is available in the SD port output FIFO.

16.2 SD Port Data Format

Serial data transactions transfer 32-bit words. Each word consists of an 8-bit status byte followed by a 24-bit output sample. The status byte, shown in Figure 32, has an MFLAG bit, channel bits, a time break bit, and a FIFO overflow bit.

MFLAG Bit - MFLAG

The MFLAG bit is set when an MFLAG signal is received on the MFLAG1-MFLAG4 pins. When received, that channel MFLAG bit is set in the next output word. See “Modulator Interface” on page 39 for more information about MFLAG.

Channel Bits - CH[1:0]

Channel bits indicate from which conversion channel the data word is from. The channel number, CH[1:0], is zero based.

CH[1:0] = 00 = Channel 1

CH[1:0] = 01 = Channel 2

CH[1:0] = 10 = Channel 3

CH[1:0] = 11 = Channel 4

Time Break Bit - TB

The time break bit marks a timing reference based on a rising edge into the TIMEB pin. After a programmed delay, the TB bit in the status byte is set for one output sample in all channels. The TIME-

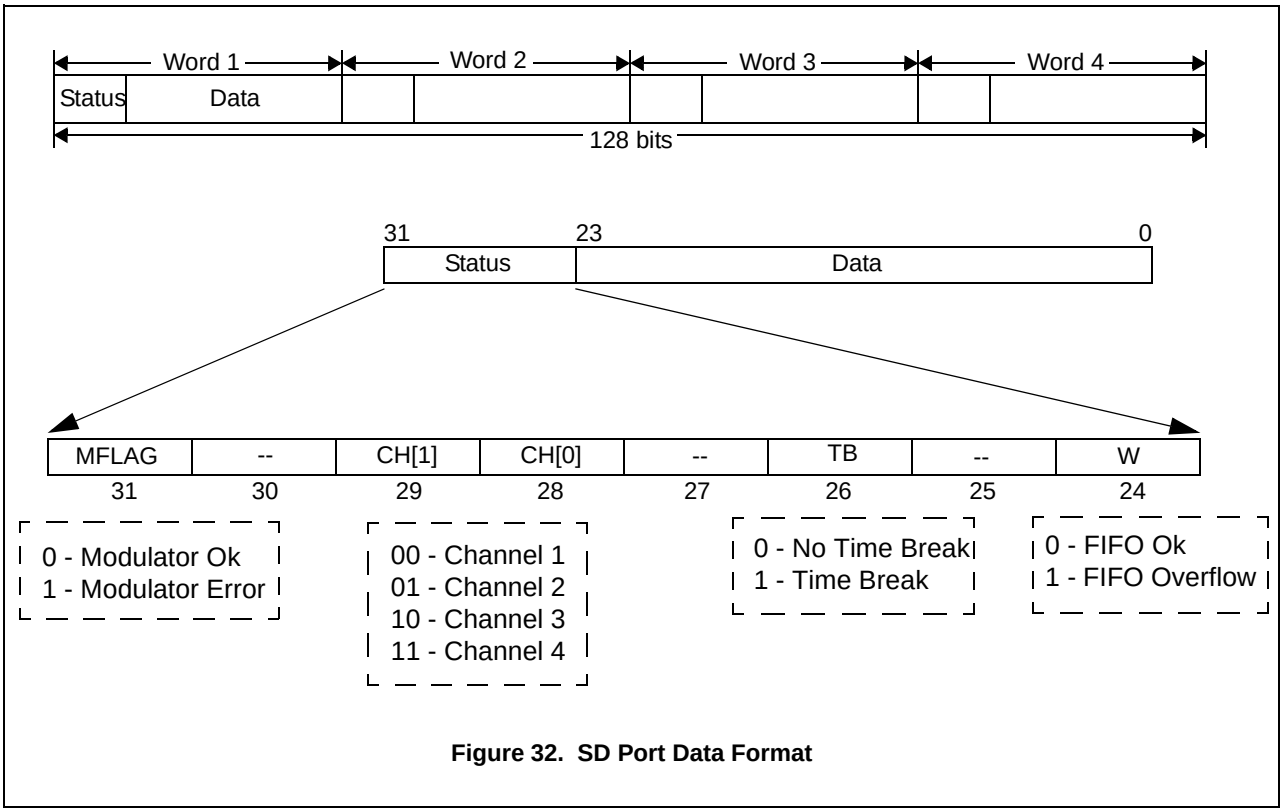


Figure 32. SD Port Data Format

BRK digital filter register (0x29) programs the sample delay for the TB bit output. See "Time Break Controller" on page 68 for more information about time break.

FIFO Overflow Bit - W

The FIFO overflow bit indicates an error condition in the SD port data FIFO, and is set if new digital filter data overwrites a FIFO location containing data which has not yet been sent.

The W bit is sticky, meaning it persists indefinitely once set. Clearing the W bit requires sending the 'Filter Stop' and 'Filter Start' configuration commands to reinitialize the data FIFO.

Conversion Data Word

The lower 24-bits of the SD port output data word is the conversion sample for the specified channel. Conversion data is 24-bit two's complement format.

16.3 SD Port Transactions

The SD port can operate in two modes depending how the SDTKI pin is connected: request mode where data is output when requested by the communications channel, or continuous mode where data is output immediately when ready.

16.3.1 Request Mode

To initiate SD port transactions on request, SDTKI is connected to an active high polling signal from the communications channel. A rising edge into SDTKI when new data is available in the SD port FIFO causes the CS5376A to initiate an SD port transaction by driving $\overline{\text{SDRDY}}$ low. If data is not yet available in the SD port FIFO, the SDTKI signal is passed through to the SDTKO output.

Once an SD port transaction is initiated, serial clocks into SDCLK cause data to be output to SDDAT, as shown in Figure 33. When all available

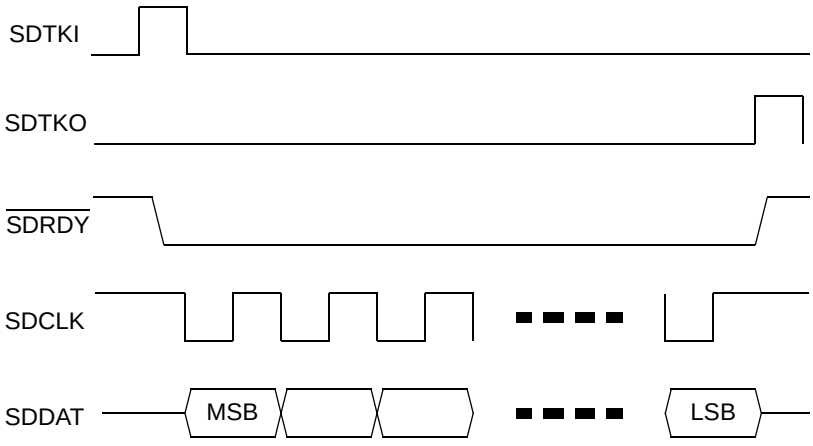


Figure 33. SD Port Transaction

data is read from the SD port data FIFO, $\overline{\text{SDRDY}}$ is released and SDTKO is pulsed high for 100 nS.

16.3.2 Continuous Mode

To have the CS5376A automatically initiate SD port transactions whenever data becomes available, connect SDTKI to a 4 MHz or slower clock source such as MCLK/2. The first rising edge into SDTKI after data becomes available in the SD port FIFO causes the CS5376A to initiate an SD port transaction by driving $\overline{\text{SDRDY}}$ low. If data is not available in the SD port FIFO, the SDTKI signal is passed through to the SDTKO output.

Once an SD port transaction is initiated, serial clocks into SDCLK cause data to be output to SDDAT, as shown in Figure 33. When all available data is read from the SD port data FIFO, $\overline{\text{SDRDY}}$ is released and SDTKO is pulsed high for 100 nS.

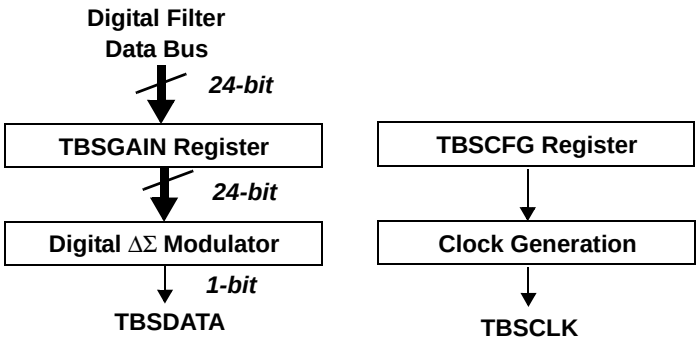


Figure 34. Test Bit Stream Generator Block Diagram

17. TEST BIT STREAM GENERATOR

The CS5376A test bit stream (TBS) generator creates sine wave or impulse ΔΣ bit stream data to drive an external test DAC. The TBS digital output can also be internally connected to the MDATA inputs for loopback testing of the digital filter.

17.1 Pin Descriptions

TBSDATA - Pin 9

Test bit stream 1-bit ΔΣ data output.

TBSCLK - Pin 8

Test bit stream clock output. Not used by the CS4373A test DAC.

17.2 TBS Architecture

The test bit stream generator consists of a data interpolator and a digital ΔΣ modulator. It receives periodic 24-bit data from the digital filter to create a 1-bit ΔΣ data output on the TBSDATA pin. It also creates a clock signal at the data rate, output to the TBSCLK pin.

The TBS input data from the digital filter is scaled by the TBSGAIN register (0x2B). Maximum stable amplitude is 0x04FFFF, with 0x04B8F2 approximately full scale for the CS4373A test DAC. The full scale 1-bit ΔΣ output from the TBS generator is defined as 25% minimum and 75% maximum one's density.

17.3 TBS Configuration

Configuration options for the TBS generator are set through the TBSCFG register (0x2A). Gain scaling of the TBS generator output is set by the TBSGAIN register (0x2B).

Interpolation Factor - INTP[7:0]

Selects how many times the interpolator uses a data point when generating the output bit stream. Interpolation is zero based and represents one greater than the programmed register value.

Operational Mode - TMODE

Selects between sine wave or impulse output mode.

Clock Rate - RATE[2:0]

Selects the TBSDATA and TBSCLK output rate.

Synchronization - TSYNC

Enables synchronization of the TBS output phase to the MSYNC signal.

Clock Delay - CDLY[2:0]

Programs a fractional delay for TBSCLK with a 1/8 clock period resolution.

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 19. TBS Configurations Using On-chip Data

Loopback - LOOP

Enables digital loopback from the TBS output to the MDATA inputs.

Run - RUN

Enables the test bit stream generator.

Data Delay - DDLY[5:0]

Programs full period delays for TBSDATA, up to a maximum of 63 bits.

Gain - TBSGAIN[23:0]

Scales the amplitude of the sine wave output and generated impulse. Maximum 0x04FFFF, nominal 0x04B8F2.

17.4 TBS Data Source

Data to create test signals is loaded into digital filter memory by configuration commands. The on-chip sine wave data is suitable for most tests, though custom data is required to support custom signal frequencies. See “EEPROM Configuration Commands” on page 28 or “Microcontroller Configuration Commands” on page 35 for information about programming TBS data.

TBS ROM Data

An on-chip 24-bit 1024 point digital sine wave is stored on the CS5376A. When selected by the ‘Write TBS ROM Data’ configuration command, the TBS generator can produce the test signal frequencies listed in Table 19. Additional discrete test frequencies and output rates can be programmed with the on-chip data by varying the interpolation factor and output rate.

Test Bit Stream Impulse Characteristics:

Interpolation Selection (INTP)	Output Rate Selection (RATE)	Pulse Width from CS4373A	Gain Scale Factor (TBSGAIN)	Pulse Height from CS4373A
0xFF	0x5	500 µs	0x04B8F2	860 mV
0xFF	0x4	1 ms	0x04B8F2	820 mV
0xFF	0x3	2 ms	0x04B8F2	820 mV
0x7F	0x5	250 µs	0x04B8F2	820 mV
0x7F	0x4	500 µs	0x04B8F2	820 mV
0x7F	0x3	1 ms	0x04B8F2	820 mV

Table 20. TBS Impulse Characteristics

Custom TBS Data

If a required test frequency cannot be generated using the on-chip test bit stream data, a custom data set can be written into the CS5376A. The number of data points to write, up to a maximum of 1024, depends on the required test signal frequency, output rate, and available interpolation factors. Custom data sets must be continuous on the ends; i.e. when copied end-to-end the data set must produce a smooth curve.

17.5 TBS Sine Wave Output

When the TMODE bit in the TBSCFG register is low, the TBS generator operates in sine wave mode. In this mode, sine wave data from digital filter memory is used to create a sine wave test signal that can drive a test DAC. Sine wave frequency and output data rate are calculated as shown by the characteristic equation of Table 19.

The sine wave maximum ΔΣ one's density output from the TBS generator is set by the TBSGAIN register. TBSGAIN can be programmed up to a maximum of 0x04FFFF, with the TBS generator unstable for higher amplitudes. For the CS4373A test DAC, a gain value of 0x04B8F2 produces an approximately full scale sine wave output (5 V_{pp} differential).

17.6 TBS Impulse Output

If the TMODE bit in TBSCFG is set high, the TBS generator operates in impulse mode. In this mode, the value in TBSGAIN sets the amplitude of the generated impulse. Impulse amplitude and period are calculated as shown in Table 20.

To create a -20 dB impulse from the TBS generator, the TBSGAIN register should be set to maximum 0x0078E5, and the INTP bits in TBSCFG should also be set to maximum 0xFF. The RATE bits should be set to produce data at the correct rate for the test DAC.

A rising edge on the TIMEB pin triggers the impulse output. When impulse mode is enabled but no TIMEB input is received, the TBS generator uses a negated TBSGAIN register as a repetitive input value. When a rising edge is recognized on the TIMEB pin, a single positive TBSGAIN value is written to the TBS generator to create the impulse.

17.7 TBS Loopback Testing

Included as part of the CS5376A test bit stream generator is a feedback path to the digital filter MDATA inputs. This loopback mode provides a fully digital signal path to test the TBS generator, digital filter, and data collection interface. Digital

loopback testing expects 512 kHz ΔΣ data for the MDATA inputs.

A mismatch of the TBS generator full scale output and the MDATA full scale input results in an amplitude mismatch when testing in loopback mode. The TBS generator outputs a 75% maximum one's density, while the MDATA inputs expect an 86% maximum one's density from a ΔΣ modulator, resulting in a measured full scale error of -3.6 dB.

17.8 TBS Synchronization

When the TSYNC bit is set in the TBSCFG register, the MSYNC signal resets the sine wave data pointer and phase aligns the TBS signal output. Once the digital filter is settled, all CS5376A devices receiving the SYNC signal will have identical TBS signal phase. See "Synchronization" on page 25 for more information about the SYNC and MSYNC signals.

If TSYNC is clear, MSYNC has no effect on the TBS data pointer and no change in the TBS output phase will occur during synchronization.

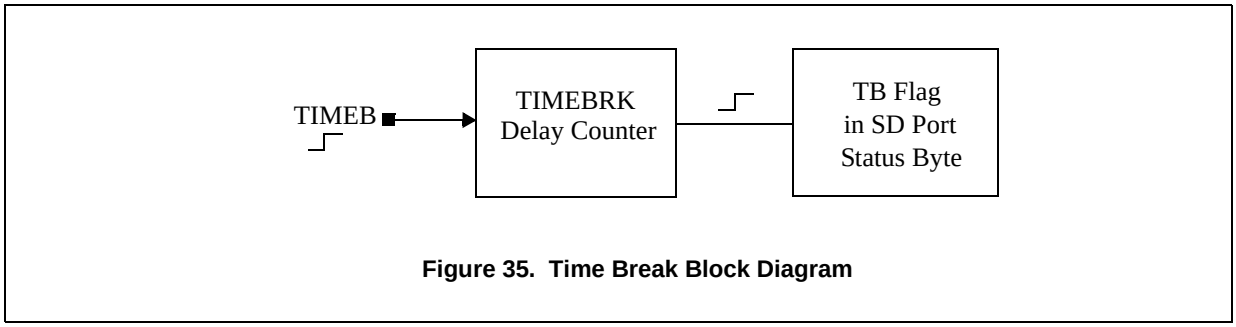


Figure 35. Time Break Block Diagram

18. TIME BREAK CONTROLLER

A time break signal is used to mark timing events that occur during measurement. An external signal sets a flag in the status byte of an output sample to mark when the external event occurred.

A rising edge input to the TIMEB pin causes the TB timing reference flag to be set in the SD port status byte. When set, the TB flag appears for only one output sample in the status byte of all enabled channels. The TB flag output can be delayed by programming a sample delay value into the TIMEBRK digital filter register.

18.1 Pin Description

TIMEB - Pin 57

Time break input pin, rising edge triggered.

18.2 Time Break Operation

An externally generated timing reference signal applied to the TIMEB pin initiates an internal sample counter. After a number of output samples have passed, programmed in the TIMEBRK digital filter register (0x29), the TB flag is set in the status byte of the SD port output word for all enabled channels. The TB flag is automatically cleared for subsequent data words, and appears for only one output sample in each channel.

18.3 Time Break Delay

The TIMEBRK register (0x29) sets a sample delay between a received rising edge on the TIMEB pin and writing the TB flag into the SD port status byte.

The programmable sample counter can compensate for group delay through the digital filters. When the proper group delay value is programmed into the TIMEBRK register, the TB flag will be set in the status byte of the measurement sample taken when the timing reference signal was received.

18.3.1 Step Input and Group Delay

A simple method to empirically measure the step response and group delay of a CS5376A measurement channel is to use the time break signal as both a timing reference input and an analog step input.

When a rising edge is received on the TIMEB pin with no delay programmed into the TIMEBRK register, the TB flag is set in the next SD port status byte. The same rising edge can act as a step input to the analog channel, propagating through the digital filter to appear as a rising edge in the measurement data. By comparing the timing of the TB status flag output and the rising edge in the measurement data, the measurement channel group delay can be determined.

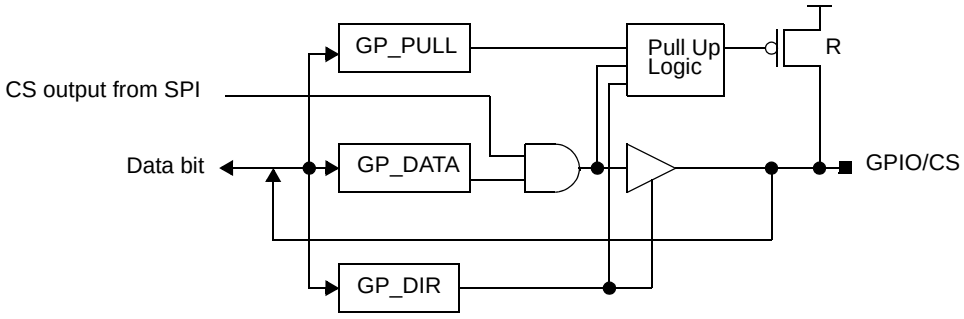


Figure 36. GPIO Bi-directional Structure

19. GENERAL PURPOSE I/O

The General Purpose I/O (GPIO) block provides 12 general purpose pins to interface with external hardware.

19.1 Pin Descriptions

GPIO[4:0]:CS[4:0] - Pins 32 - 36

Standard GPIO pins also used as SPI 2 chip selects.

GPIO[5:10] - Pins 37, 41 - 45

Standard GPIO pins.

GPIO11:EECS - Pin 46

Standard GPIO pin also used as an SPI 1 chip select when booting from an external EEPROM.

19.2 GPIO Architecture

Each GPIO pin can be configured as input or output, high or low, with a weak (~200 kΩ) internal pull-up resistor enabled or disabled. Several GPIO pins also double as chip selects for the SPI 1 and SPI 2 serial ports. Figure 36 shows the structure of a bi-directional GPIO pin with SPI chip select functionality.

When the CS5376A is used as an SPI master, either when booting from EEPROM using SPI 1 or performing master mode transactions using SPI 2, the chip select signals from SPI 1 and SPI 2 are logically AND-ed with the GPIO data bit. The corresponding GPIO pin should be initialized as output mode and logical 1 to produce the chip select falling edge.

19.3 GPIO Registers

When used as standard GPIO pins, settings are programmed in the GPCFG0 and GPCFG1 registers. GP_DIR bits set the input/output mode, GP_PULL bits enable/disable the internal pull-up resistor, and GP_DATA bits set the output data value. After reset, GPIO pins default as inputs with pull-up resistors enabled.

19.4 GPIO Input Mode

When reading a value from the GP_DATA bits, the returned data reports the current state of the pins. If a pin is externally driven high it reads a logical 1, if externally driven low it reads a logical 0. When a GPIO pin is used as an input, the pull-up resistor should be disabled to save power if it isn't required.

19.5 GPIO Output Mode

When a GPIO pin is programmed as an output with a data value of 0, the pin is driven low and the internal pull-up resistor is automatically disabled. When programmed as an output with a data value of 1, the pin is driven high and the pull-up resistor is inconsequential.

Any GPIO pin can be used as an open-drain output by setting the data value to 0, enabling the pull-up, and using the GP_DIR direction bits to control the pin value. This open-drain output configuration uses the internal pull-up resistor to hold the pin high when GP_DIR is set as an input, and drives the pin low when GP_DIR is set as an output.

19.5.1 GPIO Reads in Output Mode

When reading GPIO pins the GP_DATA register value always reports the current state of the pins, so a value written in output mode does not necessarily read back the same value. If a pin in output mode is written as a logical 1, the CS5376A attempts to drive the pin high. If an external device forces the pin low, the read value reflects the pin state and returns a logical 0. Similarly, if an output pin is written as a logical 0 but forced high externally, the read value reflects the pin state and returns a logical 1. In both cases the CS5376A is in contention with the external device resulting in increased power consumption.

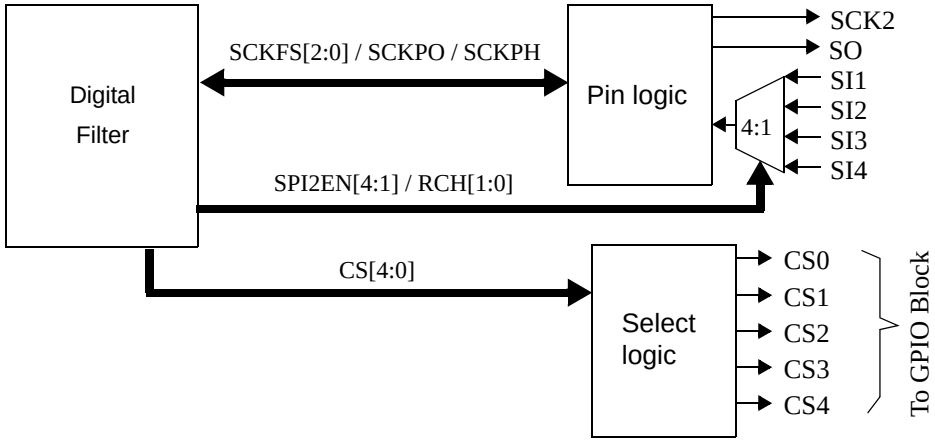


Figure 37. Serial Peripheral Interface 2 (SPI 2) Block Diagram

20.SERIAL PERIPHERAL INTERFACE 2

The Serial Peripheral Interface 2 (SPI 2) port is a master mode SPI port designed to interface with serial peripherals. By writing the SPI2 digital filter registers, multiple serial slave devices can be controlled through the CS5376A.

20.1 Pin Descriptions

CS[4:0] - Pins 32 - 36

Serial chip selects. Multiplexed with GPIO pins.

SCK2 - Pin 31

Serial clock output, common to all channels.

SO - Pin 30

Serial data output, common to all channels.

SI[4:1] - Pins 26 - 29

Serial data inputs.

20.2 SPI 2 Architecture

The SPI 2 pin interface has multiple chip selects and serial data inputs, but a common serial clock and serial data output. Which chip select and serial input to use for a particular slave serial transaction is selected by bits in the SPI2CTRL digital filter register.

SPI 2 chip select outputs are multiplexed with GPIO pins, which cannot perform both functions simultaneously. When used as a chip select, the GPIO output must be programmed high to permit the chip select to operate as an active low signal. See “General Purpose I/O” on page 69 for information about programming the GPIO pins.

The SPI 2 interface transfers data from the SPI 2 registers to a slave serial device and back through a bi-directional 8-bit shift register. Serial transactions are automatic once control, command, and data values are written into the SPI 2 digital filter registers.

20.3 SPI 2 Registers

SPI 2 transactions are initiated by first writing command, address, and data values to the SPI2CMD and SPI2DAT digital filter registers, and then writing the SPI2CTRL register to set the D2SREQ bit. The D2SREQ bit initiates a serial transaction using the programmed SPI2CTRL configuration.

20.3.1 SPI 2 Control Register

The SPI 2 hardware is configured by the SPI2CTRL digital filter register (0x10).

Bits in this register select the serial input pin and chip select pin used for a transaction, set the total number of bytes in a transaction, initiate a serial transaction, and report status information about a transaction. Other bits in SPI2CTRL set hardware configuration options such as the serial clock rate, the SPI mode, and the state of internal pull-up resistors.

Chip Select Enable - CS[4:0]

The chip select pin to use during a transaction is selected by the CS0, CS1, CS2, CS3, and CS4 bits. Multiple chip selects can be enabled to send a transaction to more than one serial peripheral.

Serial Input Select - SPI2EN[4:1], RCH[1:0]

Which serial input pin will receive data is selected using the SPI2EN bits and the RCH bits. The SPI2EN bits enable the serial input, while the RCH bits select it for the SPI 2 transaction.

A channel's SPI2EN bit should always be enabled, even when transactions do not expect to receive data from the slave device.

Transaction Bytes - DNUM[2:0]

DNUM bits specify the total number of bytes to transfer during a serial transaction, including command and address bytes. DNUM is zero based and represents one greater than the number programmed.

Serial Clock Rate - SCKFS[2:0]

The serial clock rate output from the SCK2 pin is selected by the SCKFS bits. Serial clock rates range from 32 kHz to 4.096 MHz.

SPI Mode - SCKPO, SCKPH

The serial mode used for a transaction depends on the SCKPO and SCKPH bits. The SPI 2 port supports all four SPI modes, with mode 0 and mode 3 the most commonly used. Supported modes are:

SPI Mode 0 (0,0): SCKPO = 0, SCKPH = 0

SPI Mode 1 (0,1): SCKPO = 0, SCKPH = 1

SPI Mode 2 (1,0): SCKPO = 1, SCKPH = 0

SPI Mode 3 (1,1): SCKPO = 1, SCKPH = 1

Wired-Or Mode - WOM

The SPI 2 pins can operate in two modes depending on the WOM bit. A default push-pull configuration drives output signals both high and low. Wired-Or mode only drives low, relying on a weak internal pull-up resistor to pull the output high. Wired-Or mode permits multiple serial controllers to access the same bus without contention.

Initiating Serial Transactions - D2SREQ

Writing the D2SREQ bit starts an SPI 2 serial transaction. When complete, the D2SREQ bit is automatically cleared by the SPI 2 hardware.

Status and Error Bits - D2SOP, SWEF, TM

Three bits in the SPI2CTRL register report status and error information.

D2SOP is set when the SPI 2 port is busy performing a transaction. It is automatically cleared when the transaction is completed.

SWEF is set if a request to initiate a new transaction occurs during the current transaction. This flag is latched and must be cleared manually.

TM is set to indicate the SPI 2 port timed out on the requested transaction. This flag is latched and must be cleared manually.

20.3.2 SPI 2 Command Register

The SPI2CMD register (0x11) is a 16-bit digital filter register with the high byte designated as an SPI command and the low byte designated as an address. The high byte holds an 8-bit SPI 'write' or 'read' opcode, as shown in Figure 38, and the low byte holds an 8-bit serial address.

During a transaction, bits in SPI2CMD are output MSB first, with data in SPI2DAT written or read following.

20.3.3 SPI 2 Data Register

The SPI2DAT register (0x12) is a 24-bit digital filter register containing three SPI data bytes. Data in SPI2DAT is always LSB aligned, with 1-byte data written or received using the low byte, 2-byte data written or received using the middle and low bytes, and 3-byte data written or received using all three bytes.

Data in SPI2DAT is written or read after writing the command and address bytes from the SPI2CMD register.

20.4 SPI 2 Transactions

The SPI 2 port operates as an SPI master to perform write and read transactions with serial slave peripherals. The exact format of the SPI transactions depends on the SPI mode, selected using the SCKPO and SCKPH bits in the SPI2CTRL register.

Write Transactions

Write transactions start by writing an SPI 'write' (0x02) opcode and an 8-bit destination address into the SPI2CMD register and the output data value to the SPI2DAT register. Writing the D2SREQ bit in the SPI2CTRL register initiates the SPI 2 transaction based on the SPI2CTRL configuration.

A write transaction outputs 1 or 2 bytes from the SPI2CMD register followed by 1, 2, or 3 bytes from the SPI2DAT register. Write transactions are therefore a minimum of 1 byte (DNUM = 0) and a maximum of 5 bytes (DNUM = 4). The SPI 2 port uses the DNUM bits in the SPI2CTRL register to determine the total number of bytes to send during a write transaction.

Write transactions are not required to use standard SPI commands. If serial peripherals use non-standard write commands they can be written into SPI2CMD and SPI2DAT as required.

Read Transactions

Read transactions start by writing an SPI 'read' (0x03) opcode and an 8-bit source address to the SPI2CMD register. Writing the D2SREQ bit in the SPI2CTRL register initiates the SPI 2 transaction based on the SPI2CTRL configuration, with the data value automatically received into the SPI2DAT register.

A read transaction outputs 2 bytes from the SPI2CMD register and can receive 1, 2, or 3 bytes into the SPI2DAT register. Read transactions are a minimum of 3 bytes (DNUM = 2) and a maximum of 5 bytes (DNUM = 4). The SPI 2 port uses the DNUM bits in the SPI2CTRL register to determine the total number of bytes to send and receive during a read transaction.

Read transactions are not required to use standard SPI commands. If serial peripherals use non-standard read commands they can be written to the SPI2CMD register, as long as they conform to the format of 2 bytes out with 1, 2, or 3 bytes in.

SPI Modes

The SPI mode for the SPI 2 port is selected in the SPI2CTRL register using the SCKPO and SCKPH bits. The most commonly used SPI modes are mode 0 and mode 3, both of which define the serial clock with data valid on rising edges and transitioning on falling edges.

In SPI mode 0, the SCK2 serial clock is defined initially in a low state. Output data on the SO pin is valid immediately after the chip select pin goes low, and the first rising edge of SCK2 latches valid data.

In SPI mode 3, the SCK2 serial clock is defined initially in a high state. Output data on the SO pin is invalid until the initial falling edge of SCK2, and the first rising edge of SCK2 latches valid data.

Instruction	Opcode	Address	Definition
Write	0x02	SPI2CMD[7:0]	Write serial peripheral beginning at the address given in SPI2CMD[7:0].
Read	0x03	SPI2CMD[7:0]	Read serial peripheral beginning at the address given in SPI2CMD[7:0].

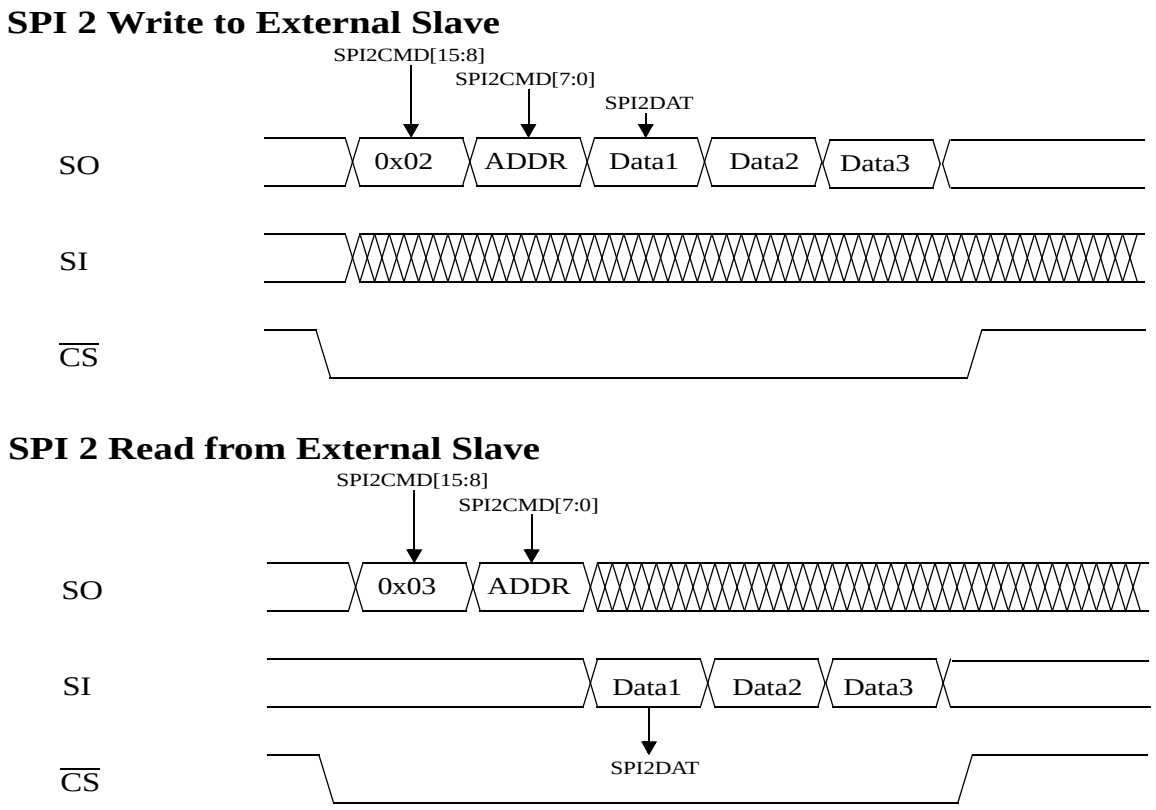
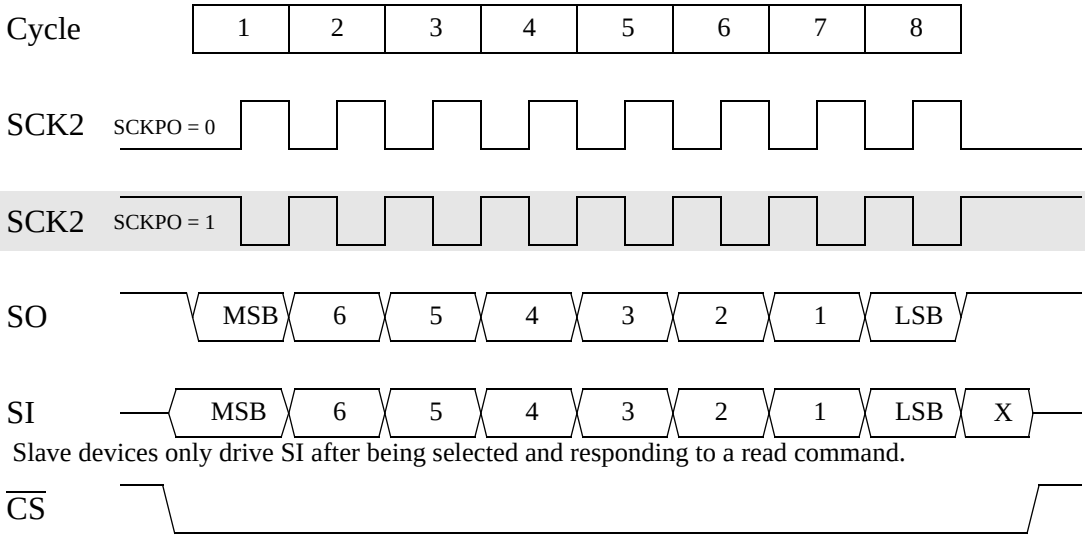


Figure 38. SPI 2 Master Mode Transactions

SPI modes 1 and 4 work similarly to modes 0 and 3, with the serial clock defined to have data valid on falling edges and transitioning on rising edges.

SPI 2 Transaction with SCKPH=0



SPI 2 Transaction with SCKPH=1

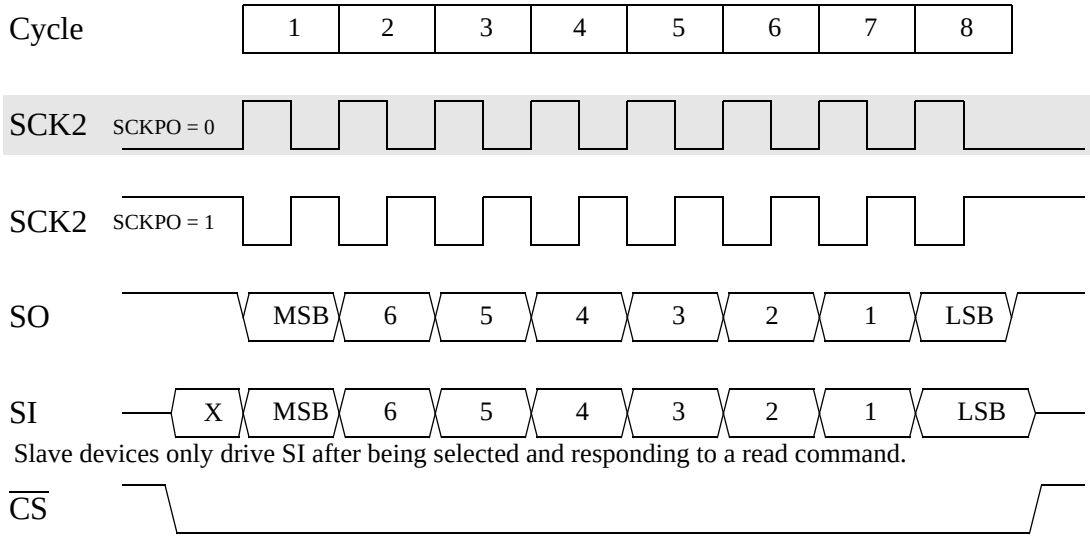


Figure 39. SPI 2 Transaction Details

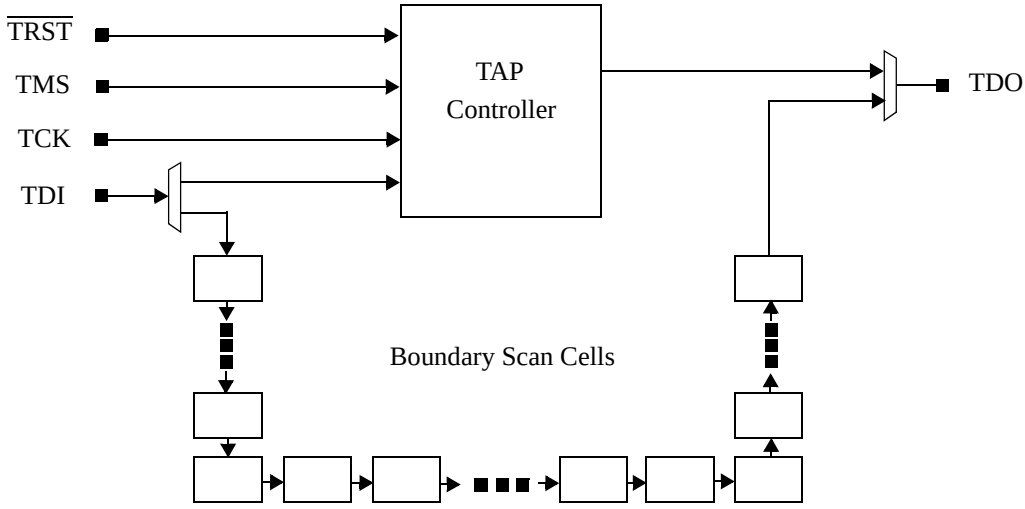


Figure 40. JTAG Block Diagram

21.BOUNDARY SCAN JTAG

The CS5376A includes an IEEE 1149.1 boundary scan JTAG port to test PCB interconnections. Refer to the IEEE 1149.1 specification for more information about boundary scan testing.

21.1 Pin Descriptions

$\overline{\text{TRST}}$ - Pin 1

Reset input for the test access port (TAP) controller and all boundary scan cells, active low. Connect to GND to disable the JTAG port.

TMS - Pin 2

Serial input to select the JTAG test mode.

TCK - Pin 3

Clock input to the TAP controller.

TDI - Pin 4

Serial input to the scan chain or TAP controller.

TDO - Pin 5

Serial output from the scan chain or TAP controller.

21.2 JTAG Architecture

The JTAG test circuitry consists of a test access port (TAP) controller and boundary scan cells connected to each pin. The boundary scan cells are linked together to create a scan chain around the CS5376A.

21.2.1 JTAG Reset

As required by the IEEE 1149.1 specification, the JTAG $\overline{\text{TRST}}$ signal is independent of the CS5376A $\overline{\text{RESET}}$ signal. In systems not using the JTAG port, $\overline{\text{TRST}}$ should be connected to ground. In systems using the JTAG port, $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ should be independently driven to provide reset capability during boundry scan.

21.2.2 TAP Controller

The test access port (TAP) controller manages commands and data through the boundary scan chain. It supports the four JTAG instructions and contains the IDCODE listed in Table 21.

The TAP controller also implements the 16 JTAG state assignments from the IEEE 1149.1 specification, which are sequenced using TMS and TCK.

JTAG Instructions	Encoding
BYPASS	11
EXTEST	00
IDCODE	01
SAMPLE / PRELOAD	10

JTAG IDCODE Components	Encoding
Revision	0x10000000
Device ID	0x05376000
Manufacturer ID	0x000000C9
CS5376A IDCODE	**0x153760C9**

Table 21. JTAG Instructions and IDCODE

21.2.3 Boundary Scan Cells

The CS5376A JTAG test port provides access to all device pins via internal boundary scan cells. When the JTAG port is disabled, boundary scan cells are transparent and do not affect CS5376A operation. When the JTAG port is enabled, boundary scan cells can write and read each pin independent of CS5376A operation.

Boundary scan cells are serially linked to create a scan chain around the CS5376A controlled by the TAP controller. Table 22 lists the scan cell mapping of the CS5376A.

BRC	Pin	Function	BRC	Pin	Function	BRC	Pin	Function
1	TBSCLK	data out	36	GPIO3	data in	68	GPIO11	data in
2	TBSDATA	data out	37		data out	69		data out
3	DNC	data out	38		output enable	70		output enable
4	MCLK/2	data out	39		pullup	71		pullup
5	MCLK	data out	40	GPIO4	data in	72	$\overline{SSO}$	data out
6	MSYNC	data out	41		data out	73		output enable
7	MDATA4	data in	42		output enable	74		WOM
8	MFLAG4	data in	43		pullup	75	SCK1	data in
9	MDATA3	data in	44	GPIO5	data in	76		data out
10	MFLAG3	data in	45		data out	77		output enable
11	MDATA2	data in	46		output enable	78		WOM
12	MFLAG2	data in	47		pullup	79		pullup
13	MDATA1	data in	48	GPIO6	data in	80	$\overline{SSI}$	data in
14	MFLAG1	data in	49		data out	81	MISO	data in
15	GND	data in	50		output enable	82		data out
16	SI4	data in	51		pullup	83		output enable
17	SI3	data in	52	GPIO7	data in	84		WOM
18	SI2	data in	53		data out	85		pullup
19	SI1	data in	54		output enable	86	MOSI	data in
20	SO	data out	55		pullup	87		data out
21		WOM	56	GPIO8	data in	88		output enable
22	SCK2	data out	57		data out	89		WOM
23		WOM	58		output enable	90		pullup
24	GPIO0	data in	59		pullup	91	$\overline{SINT}$	data out
25		data out	60	GPIO9	data in	92	$\overline{RESET}$	data in
26		output enable	61		data out	93	BOOT	data in
27		pullup	62		output enable	94	TIMEB	data in
28	GPIO1	data in	63		pullup	95	CLK	data in
29		data out	64	GPIO10	data in	96	SYNC	data in
30		output enable	65		data out	97	SDDAT	data out
31		pullup	66		output enable	98		output enable
32	GPIO2	data in	67		pullup	99	$\overline{SDRDY}$	data out
33		data out				100	SDCLK	data in
34		output enable				101	SDTKO	data out
35		pullup				102	SDTKI	data in

Table 22. JTAG Scan Cell Mapping

22.DEVICE REVISION HISTORY

The CS5376A is a pin compatible upgrade to the CS5376. The part family has had three revisions:

CS5376 rev A

CS5376 rev B

CS5376A rev A

The part number change for CS5376A reflects additional functionality built into the device.

22.1 Changes from CS5376 rev A to CS5376 rev B

New Sinc Filter, SINC3

Added a new sinc filter, SINC3, between the previous sinc filters and FIR1. Will permit higher decimation rates for seismology applications. Not used for 0.25 ms, 0.5 ms, 1 ms, or 2 ms output rates to maintain backward compatibility.

Added FIR1 Coefficients

Included an improved FIR1 filter to compensate for sinc filter droop. Previous filter had stop band frequency components up to -100 dB not removed by the FIR2 brick wall filter. Required stop band attenuation is 130 dB minimum. Previous FIR1 filter coefficients still included to maintain backwards compatibility.

Added IIR Coefficients

Included 3 Hz IIR1 and IIR2 filter coefficients for the 0.5 ms, 1 ms, 2 ms, 3 ms, and 4 ms configurations (5 sets IIR1, 5 sets IIR2). Previous 2 Hz @ 1 ms coefficient set was removed.

Modified Output Word Rate Selection

Changed the DEC bit settings in the FILTCFG register used to select an output word rate. Re-numbered to include the new 120 Hz, 60 Hz, 30 Hz, 15 Hz, and 7.5 Hz output rates. Other settings the same for backward compatibility.

Modified ROM Coefficient Selection Method

Changed the ROM coefficient selection routines (SPI and EEPROM) to require a 24 bit data word. Previously no data word was required, only the command byte. The data word is parsed to select the FIR1, FIR2, IIR1, and IIR2 coefficient sets.

Modified ROM TBS Data Selection Method

Changed the ROM test bit stream selection routine (SPI and EEPROM) to require a 24 bit data word. Previously no data word was required, only the command byte. The data word scales the ROM test bit stream data to a user selected amplitude.

Modified SPI port to strobe SINT pin

The SPI port now pulses the SINT pin whenever data is received. Can be used by a microcontroller to trigger additional data writes. Eliminates the need to poll the e2dreq bit.

Fixed continuous synchronization operation

The synchronization operation was modified to permit continuous re-sync. The SD port FIFO is no longer reset by the SYNC interrupt.

Corrected EEPROM loader bug

The EEPROM loader bug is fixed. A preamble to write required constants into memory is no longer required.

22.2 Changes from CS5376 rev B to CS5376A rev A

Fixed synchronization repeatability bug

Identical synchronization signals previously caused different impulse responses from multiple devices. Synchronization is now repeatable.

Modified SINC2 filter to correct gain and timing errors

Corrected SINC2 decimate by 2 gain error which affected 4000 SPS operation. Also modified SINC2 decimate by 16 output timing to match output of other SINC2 rates. Previous SINC2 decimate by 16 output was one sample later than expected.

Corrected gain error of 333 SPS output rate

SINC architecture was modified to correct gain error in SINC2 decimate by 12 by moving decimate by 3 stage into SINC3.

Modified SINC3 filter for new low bandwidth rates.

Newly supported output word rates are 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS. Older low bandwidth rates of 120, 60, 30, 15, 7.5 SPS were removed. No changes to 4000, 2000, 1000, 500, 333, 250 SPS rates for backwards compatibility to CS5376 revision A/B.

Added minimum phase FIR coefficients

Minimum phase FIR1 coefficient set 1 and FIR2 coefficient set 1 are newly available as selections for the SPI and EEPROM 'Write ROM Coefficients' command.

Corrected IIR2/IIR3 channels 2, 3, 4 bug

When selecting IIR2 or IIR3 output, data from channels 2, 3, and 4 were corrupted. IIR2 and IIR3 now operate correctly for these channels.

Corrected IIR2 coefficient DC offset

IIR2 coefficient sets 0, 1, and 3 did not perfectly cancel DC due to coefficient b20, b21, b22 mismatch. New b21 IIR2 coefficients correct this offset error.

Removed gain scale factor from 'Write TBS ROM' command

TBS data was previously scaled during configuration by a data word following the 'Write TBS ROM' command. Added a new TBSGAIN register (0x2B, replacing WD_CFG) that scales the TBS amplitude and can be modified during normal operation.

Removed watchdog timer

The watchdog timer was removed. Replaced WD_CFG register (0x2B) with TBSGAIN register.

Set GPIO11 as tri-state when EEPROM boot completed

After stand-alone boot from EEPROM, GPIO11 (acting as EEPROM chip select) was previously driven high. This pin now tri-states with an internal pull-up to hold it high.

Modified Test Bit Stream (TBS) to disable loopback when TBS disabled.

If TBS loopback mode was enabled, the external MDATA inputs were disconnected from the SINC filter even if the TBS was disabled. Now when the TBS is disabled, loopback mode is automatically disabled also.

Added Test Bit Stream (TBS) impulse mode.

TBS can now operate in sine wave or impulse mode, depending on bit 15 in the TBSCFG register. When impulse mode is enabled (TBSCFG bit 15 = 1), a rising edge on the TIMEB pin causes the TBS to output an impulse bitstream. When sine wave mode is enabled (TBSCFG bit 15 = 0), operation is identical to CS5376 revision A/B.

Added Test Bit Stream (TBS) synchronization in sine wave mode.

The TBS sine wave phase will reset if bit 11 of the TBSCFG register is set (TBSCFG bit 11 = 1) and a rising edge is received on the SYNC pin. When TBSCFG bit 11 is set low (TBSCFG bit 11 = 0), TBS phase is unaffected by the SYNC input similar to CS5376 revision A/B.

Modified Time Break delay function.

The timing delay between receiving a rising edge on the TIMEB pin and asserting the TIMEB flag in the output word status bits is corrected. In CS5376 revision A/B a '0' value in the TIMEBREAK register (0x29) disabled the TIMEB status bit write, and a '1' value set the status bit in the current output word. Now, a '0' value sets the TIMEB status bit in the current output word, and a '1' value delays until the following word.

23.REGISTER SUMMARY

23.1 SPI 1 Registers

The CS5376A SPI 1 registers interface the serial port to the digital filter.

Name	Addr.	Type	# Bits	Description
SPI1CTRLH	00	R/W	8	SPI 1 Control Register, High Byte
SPI1CTRLM	01	R/W	8	SPI 1 Control Register, Middle Byte
SPI1CTRLL	02	R/W	8	SPI 1 Control Register, Low Byte
SPI1CMDH	03	R/W	8	SPI 1 Command, High Byte
SPI1CMDM	04	R/W	8	SPI 1 Command, Middle Byte
SPI1CMDL	05	R/W	8	SPI 1 Command, Low Byte
SPI1DAT1H	06	R/W	8	SPI 1 Data 1, High Byte
SPI1DAT1M	07	R/W	8	SPI 1 Data 1, Middle Byte
SPI1DAT1L	08	R/W	8	SPI 1 Data 1, Low Byte
SPI1DAT2H	09	R/W	8	SPI 1 Data 2, High Byte
SPI1DAT2M	0A	R/W	8	SPI 1 Data 2, Middle Byte
SPI1DAT2L	0B	R/W	8	SPI 1 Data 2, Low Byte

23.1.1 SPI1CTRL : 0x00, 0x01, 0x02

Figure 41. SPI 1 Control Register SPI1CTRL

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	--	--	--	--
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	1

15	14	13	12	11	10	9	8
SMODF	--	--	EMOP	SWEF	--	--	E2DREQ
R	R/W	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	1	0

7	6	5	4	3	2	1	(LSB) 0
--	--	--	--	--	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	0	0	0	0

SPI 1 Address: 0x00 0x01 0x02

-- Not defined; read as 0
R Readable
W Writable
R/W Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	--	reserved	15	SMODF	SPI 1 mode fault flag	7:0	--	reserved
			14:13	--	reserved			
			12	EMOP	External master to SPI 1 operation in progress flag			
			11	SWEF	SPI 1 write collision error flag			
			10:9	--	reserved			
			8	E2DREQ	External master to digital filter request flag			

23.1.2 SPI1CMD : 0x03, 0x04, 0x05

Figure 42. SPI 1 Command Register SPI1CMD

(MSB) 23	22	21	20	19	18	17	16
S1CMD23	S1CMD22	S1CMD21	S1CMD20	S1CMD19	S1CMD18	S1CMD17	S1CMD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
S1CMD15	S1CMD14	S1CMD13	S1CMD12	S1CMD11	S1CMD10	S1CMD9	S1CMD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
S1CMD7	S1CMD6	S1CMD5	S1CMD4	S1CMD3	S1CMD2	S1CMD1	S1CMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI 1 Address: 0x03 0x04 0x05

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 S1CMD[23:16] SPI 1 Command High Byte	15:8 S1CMD[15:8] SPI 1 Command Middle Byte	15:8 S1CMD[7:0] SPI 1 Command Low Byte

23.1.3 SPI1DAT1 : 0x06, 0x07, 0x08

Figure 43. SPI 1 Data Register SPI1DAT1

(MSB) 23	22	21	20	19	18	17	16
S1DAT23	S1DAT22	S1DAT21	S1DAT20	S1DAT19	S1DAT18	S1DAT17	S1DAT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
S1DAT15	S1DAT14	S1DAT13	S1DAT12	S1DAT11	S1DAT10	S1DAT9	S1DAT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
S1DAT7	S1DAT6	S1DAT5	S1DAT4	S1DAT3	S1DAT2	S1DAT1	S1DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI 1 Address: 0x06 0x07 0x08

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 S1DAT[23:16] SPI 1 Data High Byte	15:8 S1DAT[15:8] SPI 1 Data Middle Byte	15:8 S1DAT[7:0] SPI 1 Data Low Byte

23.1.4 SPI1DAT2 : 0x09, 0x0A, 0x0B

Figure 44. SPI 1 Data Register SPI1DAT2

(MSB) 23	22	21	20	19	18	17	16
S1DAT23	S1DAT22	S1DAT21	S1DAT20	S1DAT19	S1DAT18	S1DAT17	S1DAT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
S1DAT15	S1DAT14	S1DAT13	S1DAT12	S1DAT11	S1DAT10	S1DAT9	S1DAT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
S1DAT7	S1DAT6	S1DAT5	S1DAT4	S1DAT3	S1DAT2	S1DAT1	S1DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI 1 Address: 0x09
0x0A
0x0B

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 S1DAT[23:16] SPI 1 Data High Byte	15:8 S1DAT[15:8] SPI 1 Data Middle Byte	15:8 S1DAT[7:0] SPI 1 Data Low Byte

23.2 Digital Filter Registers

The CS5376A digital filter registers control hardware peripherals and filtering functions.

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG0	0E	R/W	24	GPIO[7:0] Direction, Pull-Up Enable, and Data
GPCFG1	0F	R/W	24	GPIO[11:8] Direction, Pull-Up Enable, and Data
SPI2CTRL	10	R/W	24	SPI2 Control
SPI2CMD	11	R/W	16	SPI2 Command
SPI2DAT	12	R/W	24	SPI2 Data
RESERVED	13-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN1	21	R/W	24	Gain Correction Channel 1
GAIN2	22	R/W	24	Gain Correction Channel 2
GAIN3	23	R/W	24	Gain Correction Channel 3
GAIN4	24	R/W	24	Gain Correction Channel 4
OFFSET1	25	R/W	24	Offset Correction Channel 1
OFFSET2	26	R/W	24	Offset Correction Channel 2
OFFSET3	27	R/W	24	Offset Correction Channel 3
OFFSET4	28	R/W	24	Offset Correction Channel 4
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

23.2.1 CONFIG : 0x00

Figure 45. Hardware Configuration Register CONFIG

(MSB)23	22	21	20	19	18	17	16
--	--	--	--	--	DFS2	DFS1	DFS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	1

15	14	13	12	11	10	9	8
--	--	--	--	--	MCKFS2	MCKFS1	MCKFS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

7	6	5	4	3	2	1	(LSB)0
--	--	MCKEN2	MCKEN	MDIFS	--	BOOT	MSEN
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	0	0	1

DF Address: 0x00

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:19	--	reserved
18:16	DFS [2:0]	Digital filter frequency select 111: 16.384 MHz 110: 8.192 MHz 101: 4.096 MHz 100: 2.048 MHz 011: 1.024 MHz 010: 512 kHz 001: 256 kHz 000: 32 kHz

15:11	--	reserved
10:8	MCKFS [2:0]	MCLK frequency select 111: reserved 110: reserved 101: 4.096 MHz 100: 2.048 MHz 011: 1.024 MHz 010: 512 kHz 001: reserved 000: reserved

7:6	--	reserved
5	MCKEN2	MCLK/2 output enable 1: Enabled 0: Disabled
4	MCKEN	MCLK output enable 1: Enabled 0: Disabled
3	MDIFS	MDATA input frequency select 1: 256 kHz 0: 512 kHz
2	--	reserved
1	BOOT	Boot source indicator 1: Booted from EEPROM 0: Booted from Micro
0	MSEN	MSYNC enable 1: MSYNC generated 0: MSYNC remains low

23.2.2 GPCFG0 : 0x0E

Figure 46. GPIO Configuration Register GPCFG0

(MSB) 23	22	21	20	19	18	17	16
GP_DIR7	GP_DIR6	GP_DIR5	GP_DIR4	GP_DIR3	GP_DIR2	GP_DIR1	GP_DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
GP_PULL7	GP_PULL6	GP_PULL5	GP_PULL4	GP_PULL3	GP_PULL2	GP_PULL1	GP_PULL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

7	6	5	4	3	2	1	(LSB) 0
GP_DATA7	GP_DATA6	GP_DATA5	GP_DATA4	GP_DATA3	GP_DATA2	GP_DATA1	GP_DATA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

DF Address: 0x0E

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	GP_DIR [7:0]	GPIO pin direction 1: Output 0: Input	15:8	GP_PULL [7:0]	GPIO pullup resistor 1: Enabled 0: Disabled	7:0	GP_DATA [7:0]	GPIO data value 1: VDD 0: GND

Note: GPIO[4:0] also used as SPI 2 chip selects CS[4:0].

23.2.3 GPCFG1 : 0x0F

Figure 47. GPIO Configuration Register GPCFG1

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	GP_DIR11	GP_DIR10	GP_DIR9	GP_DIR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
--	--	--	--	GP_PULL11	GP_PULL10	GP_PULL9	GP_PULL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	1	1

7	6	5	4	3	2	1	(LSB) 0
--	--	--	--	GP_DATA11	GP_DATA10	GP_DATA9	GP_DATA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	1	1

DF Address: 0x0F

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:20	--	reserved	15:12	--	reserved	7:4	--	reserved
19:16	GP_DIR [11:8]	GPIO pin direction 1: Output 0: Input	11:8	GP_PULL [11:8]	GPIO pullup resistor 1: Enabled 0: Disabled	3:0	GP_DATA [11:8]	GPIO data value 1: VDD 0: GND

Note: GPIO11 also used as boot EEPROM chip select EECS.

23.2.4 SPI2CTRL : 0x10

Figure 48. SPI 2 Control Register SPI2CTRL

(MSB) 23	22	21	20	19	18	17	16
WOM	SCKFS2	SCKFS1	SCKFS0	SPI2EN3	SPI2EN2	SPI2EN1	SPI2EN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1

15	14	13	12	11	10	9	8
RCH1	RCH0	D2SOP	SCKPH	SWEF	SCKPO	TM	D2SREQ
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
DNUM2	DNUM1	DNUM0	CS4	CS3	CS2	CS1	CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	0	0	0	0	0

DF Address: 0x10

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition.

Bit definitions:

23	WOM	Wired-or mode 1: Enabled (open drain) 0: Disabled (push-pull)	15:14	RCH [1:0]	Read channel 11: SI4 10: SI3 01: SI2 00: SI1	7:5	DNUM [2:0]	Number of bytes in serial transaction
22:20	SCKFS [2:0]	SCK2 frequency select 111: reserved 110: reserved 101: 4.096 MHz 100: 2.048 MHz 011: 1.024 MHz 010: 512 kHz 001: 128 kHz 000: 32 kHz	13	D2SOP	Digital filter to SPI2 operation in progress flag	4	CS4	Chip Select 4 Enable
			12	SCKPH	SO output timing 1: Data becomes valid on first SCK2 edge 0: Data becomes valid before first SCK2 edge	3	CS3	Chip Select 3 Enable
						2	CS2	Chip Select 2 Enable
			11	SWEF	SPI2 write collision flag	1	CS1	Chip Select 1 Enable
19:16	SPI2EN [3:0]	SI[4:1] input enable 1111: All enabled 0000: All disabled	10	SCKPO	SCK2 data polarity 1: Valid on falling edge, transition on rising edge 0: Valid on rising edge, transition on falling edge	0	CS0	Chip Select 0 Enable
			9	TM	SPI2 timeout flag 1: SPI2 timed out 0: not timed out			
			8	D2SREQ	Digital filter to SPI2 serial transaction request 1: Request operation 0: Operation complete (cleared by hardware)			

23.2.5 SPI2CMD : 0x11

Figure 49. SPI 2 Command Register SPI2CMD

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	--	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SCMD15	SCMD14	SCMD13	SCMD12	SCMD11	SCMD10	SCMD9	SCMD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SCMD7	SCMD6	SCMD5	SCMD4	SCMD3	SCMD2	SCMD1	SCMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x11

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 -- reserved	15:8 SCMD[15:8] SPI2 Upper Command Byte	15:8 SCMD[7:0] SPI2 Lower Command Byte

23.2.6 SPI2DAT : 0x12

Figure 50. SPI 2 Data Register SPI2DAT

(MSB) 23	22	21	20	19	18	17	16
SDAT23	SDAT22	SDAT21	SDAT20	SDAT19	SDAT18	SDAT17	SDAT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SDAT15	SDAT14	SDAT13	SDAT12	SDAT11	SDAT10	SDAT9	SDAT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x12

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 SDAT[23:16] SPI2 Upper Data Byte	15:8 SDAT[15:8] SPI2 Middle Data Byte	15:8 SDAT[7:0] SPI2 Lower Data Byte

23.2.7 FILTCFG : 0x20

Figure 51. Filter Configuration Register FILTCFG

(MSB) 23	22	21	20	19	18	17	16
--	--	--	EXP4	EXP3	EXP2	EXP1	EXP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
--	ORCAL	USEOR	USEGR	--	FSEL2	FSEL1	FSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
DEC3	DEC2	DEC1	DEC0	--	--	CH1	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x20

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:21	--	reserved	15	--	reserved	7:4	DEC[3:0]	Decimation selection (Output word rate)
20:16	EXP[4:0]	OFFSET calibration exponent	14	ORCAL	Run OFFSET calibration 1: Enable 0: Disable			0111: 4000 SPS 0110: 2000 SPS 0101: 1000 SPS 0100: 500 SPS 0011: 333 SPS
			13	USEOR	Use OFFSET correction 1: Enable 0: Disable			0010: 250 SPS 0001: 200 SPS 0000: 125 SPS 1111: 100 SPS 1110: 50 SPS
			12	USEGR	Use GAIN correction 1: Enable 0: Disable			1101: 40 SPS 1100: 25 SPS 1011: 20 SPS 1010: 10 SPS 1001: 5 SPS 1000: 1 SPS
			11	--	reserved	3:2	--	reserved
			10:8	FSEL[2:0]	Output filter stage select 111: reserved 110: reserved 101: IIR 3rd Order 100: IIR 2nd Order 011: IIR 1st Order 010: FIR2 Output 001: FIR1 Output 000: SINC Output	1:0	CH[1:0]	Channel Enable 11: 3 Channel (1, 2, 3) 10: 2 Channel (1, 2) 01: 1 Channel (1 only) 00: 4 Channel (1, 2, 3, 4)

23.2.8 GAIN1 - GAIN4 : 0x21 - 0x24

Figure 52. Gain Correction Register GAIN1

(MSB) 23	22	21	20	19	18	17	16
GAIN23	GAIN22	GAIN21	GAIN20	GAIN19	GAIN18	GAIN17	GAIN16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
GAIN15	GAIN14	GAIN13	GAIN12	GAIN11	GAIN10	GAIN9	GAIN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x21

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 GAIN[23:16] Gain Correction Upper Byte	15:8 GAIN[15:8] Gain Correction Middle Byte	15:8 GAIN[7:0] Gain Correction Lower Byte

23.2.9 OFFSET1 - OFFSET4 : 0x25 - 0x28

Figure 53. Offset Correction Register OFFSET1

(MSB) 23	22	21	20	19	18	17	16
OFST23	OFST22	OFST21	OFST20	OFST19	OFST18	OFST17	OFST16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
OFST15	OFST14	OFST13	OFST12	OFST11	OFST10	OFST9	OFST8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
OFST7	OFST6	OFST5	OFST4	OFST3	OFST2	OFST1	OFST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x25

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 OFST[23:16] Offset Correction Upper Byte	15:8 OFST[15:8] Offset Correction Middle Byte	15:8 OFST[7:0] Offset Correction Lower Byte

23.2.10 TIMEBRK : 0x29

Figure 54. Time Break Counter Register TIMEBRK

(MSB) 23	22	21	20	19	18	17	16
TBRK23	TBRK22	TBRK21	TBRK20	TBRK19	TBRK18	TBRK17	TBRK16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
TBRK15	TBRK14	TBRK13	TBRK12	TBRK11	TBRK10	TBRK9	TBRK8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
TBRK7	TBRK6	TBRK5	TBRK4	TBRK3	TBRK2	TBRK1	TBRK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x29

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	TBRK[23:16]	Time Break Counter Upper Byte	15:8	TBRK[15:8]	Time Break Counter Middle Byte	15:8	TBRK[7:0]	Time Break Counter Lower Byte

23.2.11 TBSCFG : 0x2A

Figure 55. Test Bit Stream Configuration Register TBSCFG

(MSB) 23	22	21	20	19	18	17	16
INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
TMODE	RATE2	RATE1	RATE0	TSYNC	CDLY2	CDLY1	CDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
LOOP	RUN	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2A

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	INTP[7:0]	Interpolation factor 0xFF: 256 0xFE: 255 ... 0x01: 2 0x00: 1 (use once)	15	TMODE	Operational mode 1: Impulse mode 0: Sine Mode	7	LOOP	Loopback TBSDATA output to MDATA inputs 1: Enabled 0: Disabled
			14:12	RATE[2:0]	TBSDATA and TBSCLK output rate. 111: 2.048 MHz 110: 1.024 MHz 101: 512 kHz 100: 256 kHz 011: 128 kHz 010: 64 kHz 001: 32 kHz 000: 4 kHz	6	RUN	Run Test Bit Stream 1: Enabled 0: Disabled
			11	TSYNC	Synchronization 1: Sync enabled 0: No sync			
			10:8	CDLY[2:0]	TBSCLK output phase delay 111: 7/8 period 110: 3/4 period 101: 5/8 period 100: 1/2 period 011: 3/8 period 010: 1/4 period 001: 1/8 period 000: none	5:0	DDLY[5:0]	TBSDATA output delay 0x3F: 63 bits 0x3E: 62 bits ... 0x01: 1 bit 0x00: 0 bits (no delay)

23.2.12 TBSGAIN : 0x2B

Figure 56. Test Bit Stream Gain Register TBSGAIN

(MSB) 23	22	21	20	19	18	17	16
TGAIN23	TGAIN22	TGAIN21	TGAIN20	TGAIN19	TGAIN18	TGAIN17	TGAIN16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
TGAIN15	TGAIN14	TGAIN13	TGAIN12	TGAIN11	TGAIN10	TGAIN9	TGAIN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
TGAIN7	TGAIN6	TGAIN5	TGAIN4	TGAIN3	TGAIN2	TGAIN1	TGAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2B

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 TGAIN[23:16] Test Bit Stream Gain Upper Byte	15:8 TGAIN[15:8] Test Bit Stream Gain Middle Byte	15:8 TGAIN[7:0] Test Bit Stream Gain Lower Byte

23.2.13 SYSTEM1, SYSTEM2 : 0x2C, 0x2D

Figure 57. User Defined System Register SYSTEM1

(MSB) 23	22	21	20	19	18	17	16
SYS23	SYS22	SYS21	SYS20	SYS19	SYS18	SYS17	SYS16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SYS15	SYS14	SYS13	SYS12	SYS11	SYS10	SYS9	SYS8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SYS7	SYS6	SYS5	SYS4	SYS3	SYS2	SYS1	SYS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2C

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	SYS[23:16]	System Register Upper Byte		15:8	SYS[15:8]	System Register Middle Byte		15:8	SYS[7:0]	System Register Lower Byte

23.2.14 VERSION : 0x2E

Figure 58. Hardware Version ID Register VERSION

(MSB) 23	22	21	20	19	18	17	16
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	1	0	1	1	0

15	14	13	12	11	10	9	8
HW7	HW6	HW5	HW4	HW3	HW2	HW1	HW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

7	6	5	4	3	2	1	(LSB) 0
ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

DF Address: 0x2E

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	TYPE [7:0]	Chip Type 76 - CS5376, CS5376A	15:8	HW [7:0]	Hardware Revision 01 - CS5376 Rev A 02 - CS5376 Rev B 03 - CS5376A Rev A	7:4	ROM [7:0]	ROM Version 01 - Ver 1.0 02 - Ver 2.0 03 - Ver 3.0

23.2.15 SELFTEST : 0x2F

Figure 59. Self Test Result Register SELFTEST

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	EU3	EU2	EU1	EU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	0

15	14	13	12	11	10	9	8
DRAM3	DRAM2	DRAM1	DRAM0	PRAM3	PRAM2	PRAM1	PRAM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

7	6	5	4	3	2	1	(LSB) 0
DROM3	DROM2	DROM1	DROM0	PROM3	PROM2	PROM1	PROM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

DF Address: 0x2F

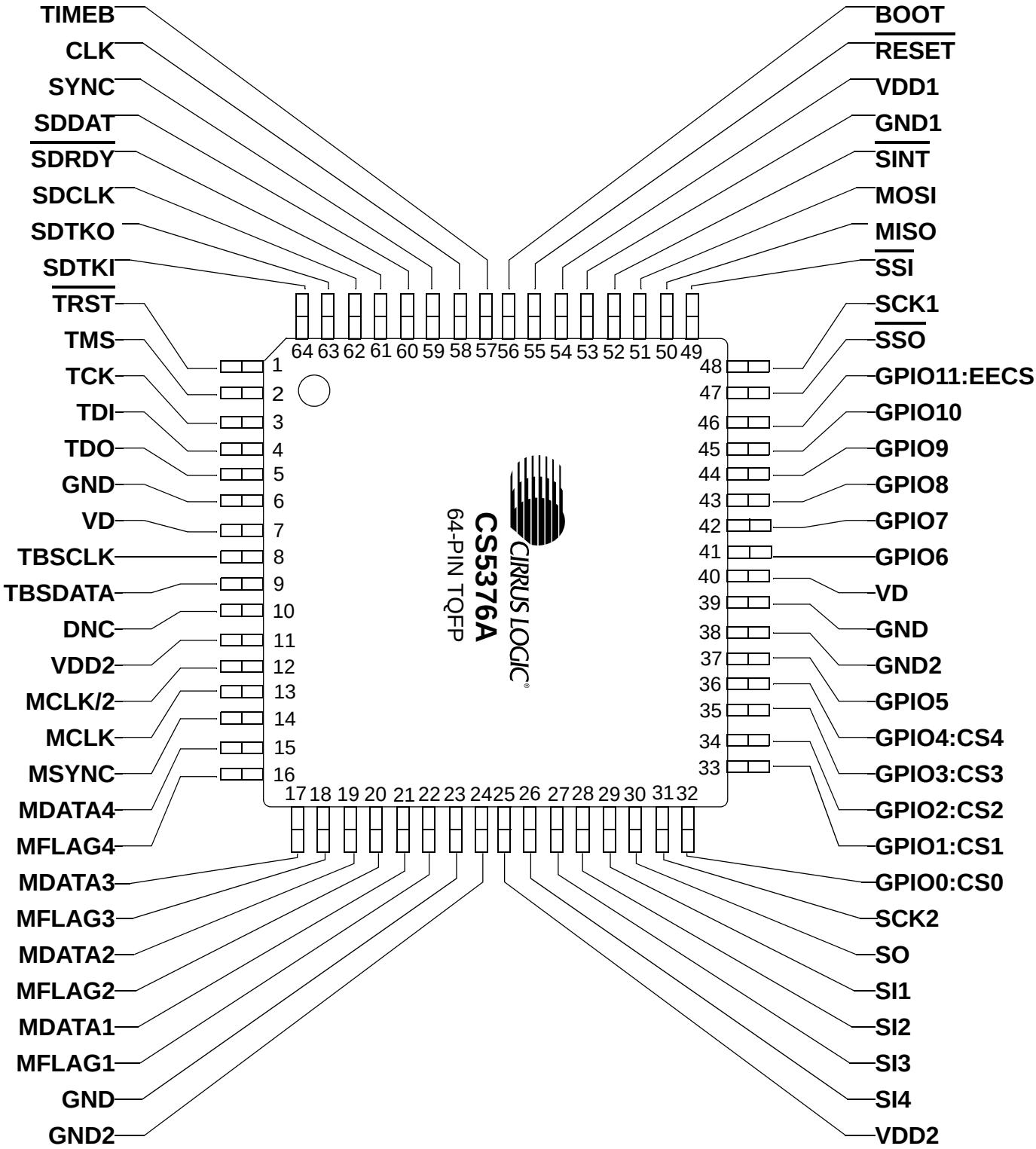
--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:20	--	reserved	15:12	DRAM [3:0]	Data RAM Test 'A': Pass 'F': Fail	7:4	DROM [3:0]	Data ROM Test 'A': Pass 'F': Fail
19:16	EU [3:0]	Execution Unit Test 'A': Pass 'F': Fail	11:8	PRAM [3:0]	Program RAM Test 'A': Pass 'F': Fail	3:0	PROM [3:0]	Program ROM Test 'A': Pass 'F': Fail

24.PIN DESCRIPTIONS

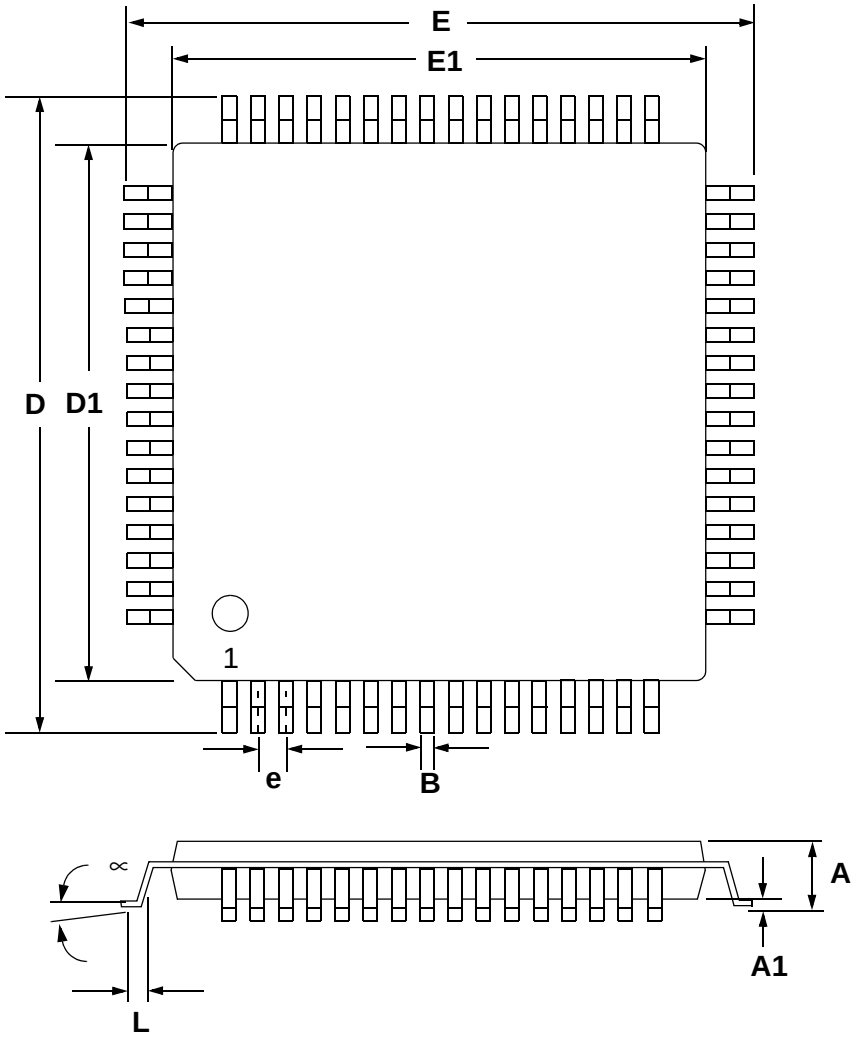


Pin Name	Pin Number	Pin Type	Pin Description
JTAG port			
$\overline{\text{TRST}}$	1	Input	JTAG reset, active low. Connect to GND if JTAG is not used.
TMS	2	Input	JTAG test mode select.
TCK	3	Input	JTAG clock input.
TDI	4	Input	JTAG data input.
TDO	5	Output	JTAG data output.
Test Bit Stream			
TBSCLK	8	Output	Test bit stream clock output.
TBSDATA	9	Output	Test bit stream data output.
No Connect			
DNC	10	N/A	Do not connect.
Modulator Interface			
MCLK/2	12	Output	Modulator clock output, half rate.
MCLK	13	Output	Modulator clock output, full rate.
MSYNC	14	Output	Modulator sync output.
MDATA[4:1]	15, 17, 19, 21	Input	Modulator data inputs.
MFLAG[4:1]	16, 18, 20, 22	Input	Modulator flag inputs.
Serial Peripheral Interface 2			
SI[4:1]	26, 27, 28, 29	Input	SPI 2 data inputs.
SO	30	Output	SPI 2 data output.
SCK2	31	Output	SPI 2 clock output.
General Purpose Input / Output			
GPIO[0:4]:CS[0:4]	32, 33, 34, 35, 36	Input / Output	General Purpose I/O with SPI 2 chip selects.
GPIO[5:10]	37, 41, 42, 43, 44, 45	Input / Output	General Purpose I/O.
GPIO11:EECS	46	Input / Output	General Purpose I/O with boot EEPROM chip select.
Serial Peripheral Interface 1			
$\overline{\text{SSO}}$	47	Output	SPI 1 slave select output, active low.
SCK1	48	Input / Output	SPI 1 serial clock input / output.
$\overline{\text{SSI}}$	49	Input	SPI 1 slave select input, active low.
MISO	50	Input / Output	SPI 1 data, master in / slave out. Open drain output requiring a 10 kΩ pull-up.
MOSI	51	Input / Output	SPI 1 data, master out / slave in.
$\overline{\text{SINT}}$	52	Output	SPI 1 serial interrupt output, active low.
Reset Control			
$\overline{\text{RESET}}$	55	Input	Reset, active low.
BOOT	56	Input	Boot mode select.
Time Break			
TIMEB	57	Input	Time break input.

Pin Name	Pin Number	Pin Type	Pin Description
Clock and Synchronization			
CLK	58	Input	Clock input, nominal 32.768 MHz.
SYNC	59	Input	Sync input.
Serial Data Port			
SDDAT	60	Output	SD port data output.
$\overline{\text{SDRDY}}$	61	Output	SD port data ready, active low. Open drain output requiring a 10 kΩ pull-up.
SDCLK	62	Input	SD port clock input.
SDTKO	63	Output	SD port token output.
SDTKI	64	Input	SD port token input.
Power Supplies			
VDD1	54	Supply	Pin power supply for pins 1 - 5 and 41 - 64.
VDD2	11, 25	Supply	Pin power supplies for pins 8 - 37.
VD	7, 40	Supply	Logic core power supplies.
GND1, GND2, GND	6, 23, 24, 38, 39, 53	Supply	Digital grounds.

25.PACKAGE DIMENSIONS

64L TQFP PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.063	---	1.60
A1	0.002	0.006	0.05	0.15
B	0.007	0.011	0.17	0.27
D	0.461	0.484	11.70	12.30
D1	0.390	0.398	9.90	10.10
E	0.461	0.484	11.70	12.30
E1	0.390	0.398	9.90	10.10
e*	0.016	0.024	0.40	0.60
L	0.018	0.030	0.45	0.75
µ	0.000°	7.000°	0.00°	7.00°

* Nominal pin pitch is 0.50 mm
Controlling dimension is mm.
JEDEC Designation: MS026

26.ORDERING INFORMATION

Model	Temperature	Package
CS5376A-IQ	-40 to +85 °C	64-pin TQFP
CS5376A-IQZ Lead Free		

27.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5376A-IQ	240 °C	3	7 Days
CS5376A-IQZ Lead Free	250 °C		

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

28.REVISION HISTORY

Revision	Date	Changes
PP1	SEP 2003	Initial “Preliminary Product” release.
F1	FEB 2004	Update group delay on page 50, power consumption on page 14 and MISO read timing on page 15. Add TBS impulse data on page 66 and MOSI pull-up on page 32.
F2	AUG 2005	Updated ordering information. Added MSL data.
F3	SEP 2005	Added lead-free device ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com